SYNERGY SEMICONDUCTOR

QUAD OC-3 SONET/SDH/ATM CLOCK RECOVERING TRANSCEIVER

PRELIMINARY INFORMATION
SY69743

FEATURES

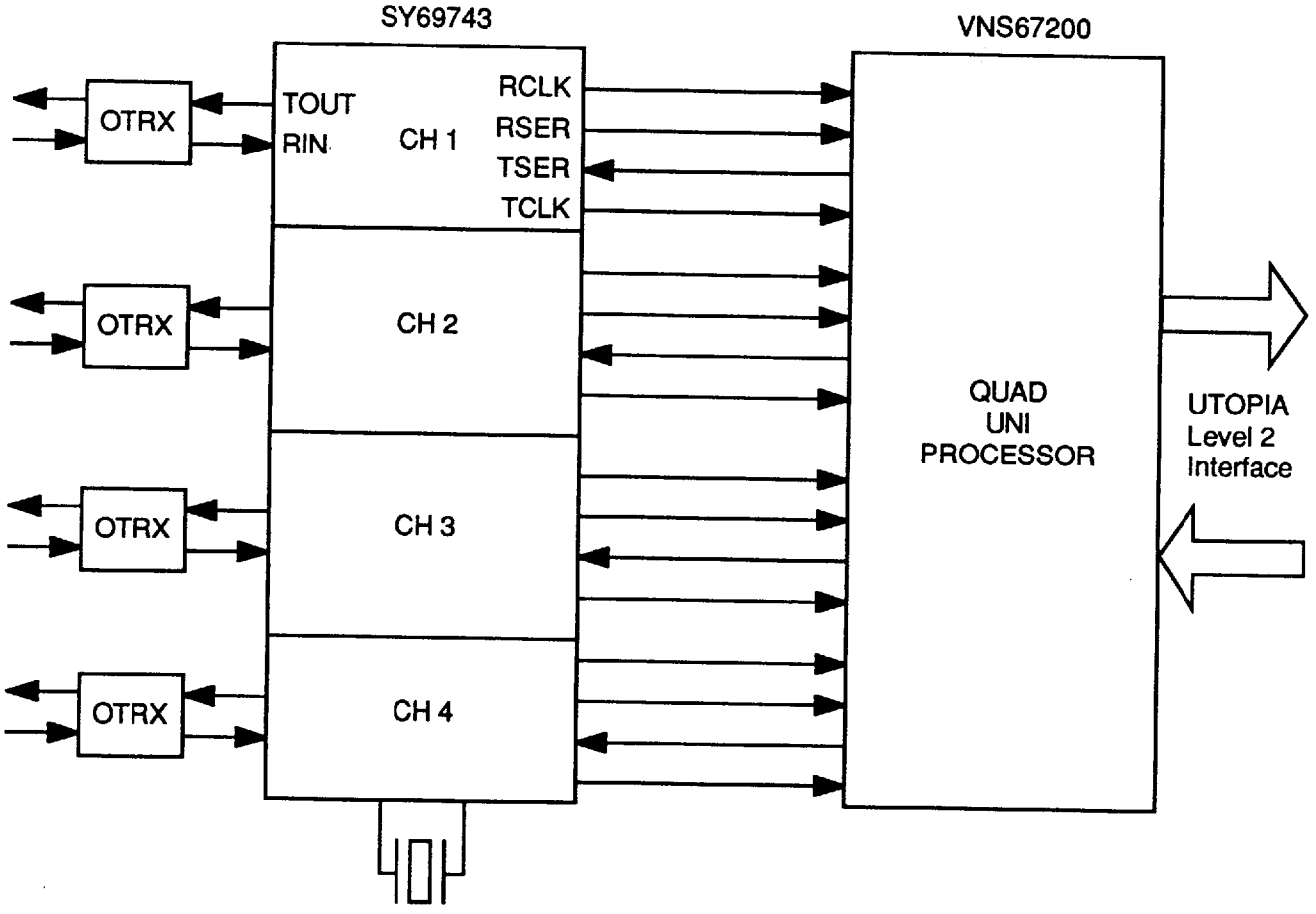
- A complete single-chip 4 Channel Transmitter & Receiver
- Complies with Bellcore, CCITT and ANSI Specifications
- Compatible with VTI VNS67200 Quad UNI Processor and PMC-Sierra PM5345 SUNI and IgT WAC-013-B ATM UNI Processor
- Supports clock recovery for 51.84 Mbit/s or 155.52 Mbit/s NRZ or NRZI data stream
- Supports clock generation for 51.84 Mbit/s OC/STS-1 or 155.52 Mbit/s OC/STS-3 SONET/SDH and ATM applications
- Operates from a single 12.96MHz crystal
- 100K ECL compatible I/O
- Single +5 volt power supply
- 128-pin PowerQuad2 package
- Typical power dissipation of only 1.8 watts

DESCRIPTION

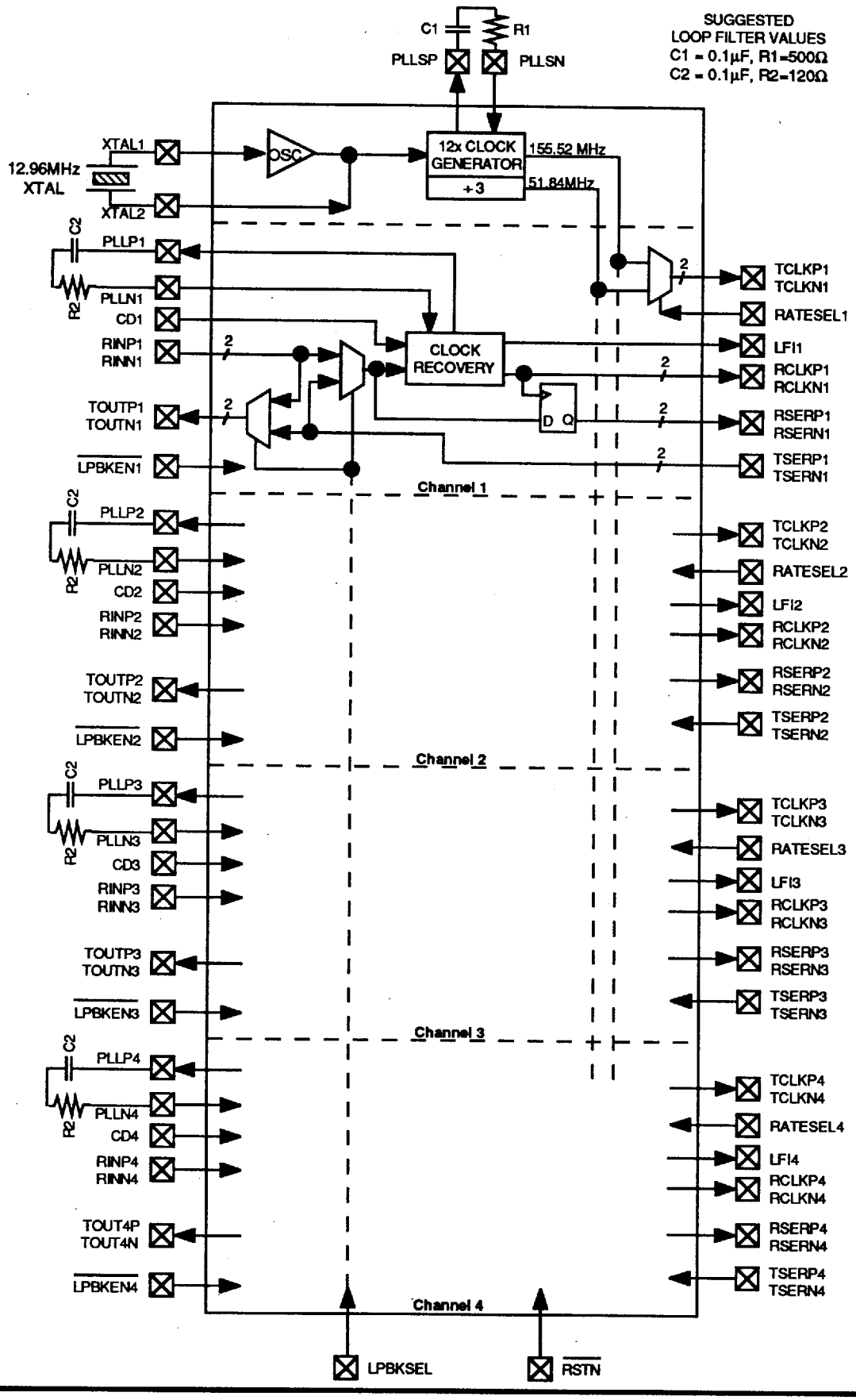
Synergy's SY69743 is designed to provide high performance clock recovery and generation for either 51.84 Mbit/s OC/STS-1 or 155.52 Mbit/s OC/STS-3 SONET/SDH and ATM applications. The SY69743 is ideally suited for SONET -based ATM applications, and is fabricated in Synergy's proprietary ASSET bipolar process.

The SY69743 recovers clock and data information from a 51.84 Mbit/s or 155.52, NRZ or NRZI, Mbit/s serial data stream. It also provides differential buffering for the transmit data.

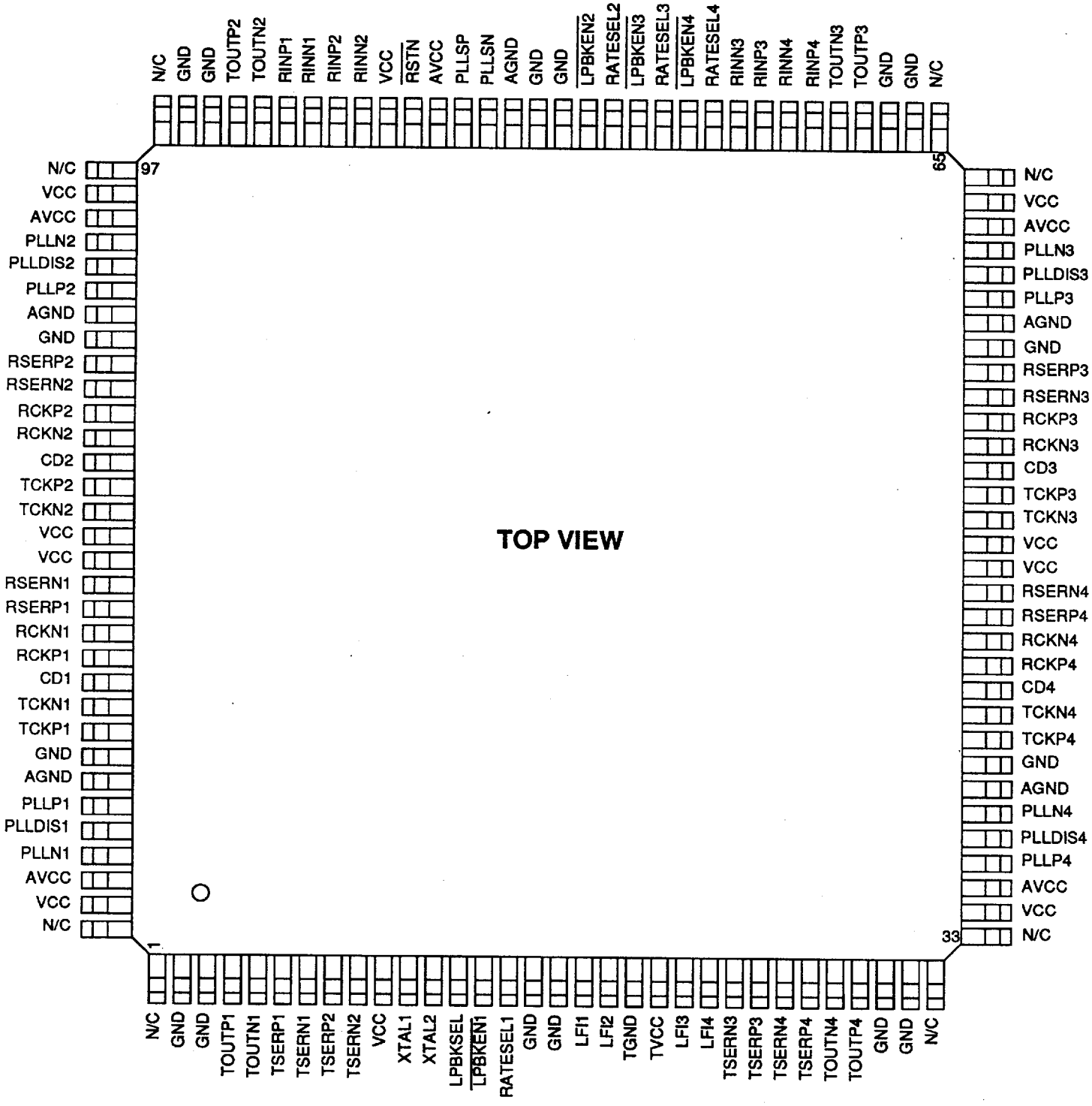
SONET/SDH and ATM Interface



FUNCTIONAL BLOCK DIAGRAM



PINOUT


TOP VIEW
1
33
65
97
N/C
GND
GND
TOUTP2
TOUTN2
RINP1
RINN1
RINP2
RINN2
VCC
RSTN
AVCC
PLLSP
PLLSN
AGND
GND
GND
LPBKEN2
RATESEL2
LPBKEN3
RATESEL3
LPBKEN4
RATESEL4
RINN3
RINP3
RINN4
RINP4
TOUTN3
TOUTP3
GND
GND
N/C
N/C
VCC
AVCC
PLLN2
PLLDIS2
PLLP2
AGND
GND
RSERP2
RSERN2
RCKP2
RCKN2
CD2
TCKP2
TCKN2
VCC
VCC
RSERN1
RSERP1
RCKN1
RCKP1
CD1
TCKN1
TCKP1
GND
AGND
PLLP1
PLLDIS1
PLLN1
AVCC
VCC
N/C
N/C
VCC
AVCC
PLLN3
PLLDIS3
PLLP3
AGND
GND
RSERP3
RSERN3
RCKP3
RCKN3
CD3
TCKP3
TCKN3
VCC
VCC
RSERN4
RSERP4
RCKN4
RCKP4
CD4
TCKN4
TCKP4
GND
AGND
PLLN4
PLLDIS4
PLLP4
AVCC
VCC
N/C
N/C
GND
GND
TOUTP1
TOUTN1
TSERP1
TSERN1
TSERP2
TSERN2
VCC
XTAL1
XTAL2
LPBKSEL
LPBKEN1
RATESEL1
GND
GND
LFI1
LFI2
TGND
TVCC
LFI3
LFI4
TSERN3
TSERP3
TSERN4
TSERP4
TOUTN4
TOUTP4
GND
GND
N/C

PIN NAMES

INPUTS

RINP1/RINN1, ..., RINP4/RINN4 - Receive Input.
Differential PECL.
These are the differential receive serial inputswith built-in line receiver for each of the four channels. Clock is recovered from the transitions on these inputs.

TSERP1/TSERN1, ..., TSERP4/TSERN4 - Transmit Serial Data.
Differential PECL.
These are differential receive inputs with built-in line receiver for each of the four channels. The serial data to be transmitted is presented on these line receiver pins.

LPBKSEL - Loopback Select. TTL.
This input selects the loop path of either the receive data stream or the transmit data stream for the respective channel. It is used in conjunction with the LPBKEN (Loopback Enable) pins. When HIGH, the receive data stream is looped back out through the respective TOUTP/TOUTN (Transmit Output) pins. When LOW, the data presented on the TSERP/TSERN(Transmit Serial Data) pins is looped back through the clock recovery circuit and is presented on the RSERP/RSERN (Recovered Serial Data) pins along with the recovered clock on the RCLKP/ RCLKN (Recovered Clock) pins.

$\overline{\text{LPBKEN1}}$, ..., $\overline{\text{LPBKEN4}}$ - Loopback Enable. TTL.- ACTIVE LOW
These active LOW inputs enable the loopback mode for the respective channels. The loopback path is selected by the state of the LPBKSEL (Loopback Select) pin. When HIGH, the device is in normal receive/transmit mode.

CD1, ..., CD4 - Carrier Detect. PECL.- ACTIVE HIGH
These inputs controls the recovery function of the receive PLL for each channel and can be driven by the carrier detect output from optical modules. When HIGH, the data on RINP,RINN (Receive Input) pins is recovered normally. When LOW, the internal transition detect circuitry and the clock recovery is disabled. When LOW, the Clock Recovery PLL no longer aligns to the RINP/RINN, but instead aligns with the internal equivalent of TCLKP/TCLKN. The LFI for the respective channel will transition LOW, and the RSERP (Recovered Serial Data) will remain LOW regardless of the signal level on the RINP/RINN (Receive Input) pins.

RATESEL1, ..., RATESEL4 - Rate Select. TTL.
These pins select the bit clock rate for the respective channel. When HIGH, a bit rate of 155.52MHz is selected and when LOW, a bit rate of 51.84MHz is selected.

$\overline{\text{RSTN}}$ - Master Reset. TTL. - ACTIVE LOW
This input should be used to initialize all internal circuitry upon power-up. Upon power-up this pin must held LOW for 1 millisecond to properly initialize the device.

OUTPUTS

TOUTP1/TOUTN1, ..., TOUTP4,TOUTN4 - Transmit Output.
Differential PECL.
These pins are normally connected to the optical transmitter module of the respective channel. These represent the buffered version of the Transmit Serial Data.

TCLKP1/TCLKN1,..., TCLKP4,TCLKN4 - Transmit Clock.
Differential PECL.
These pins provide the reference bit rate clock for the transmit processing device. The frequency of the output depends on the state of the RATESEL (Rate Select) pin.

LFI - Link Fault Indicator. TTL.
This output indicated the status of the input data stream. It is controlled by three functions; the Carrier Detect input, the internal transition detection circuitry, and the Out of Lock detector. The transition detector determines if RINP/RINN has enough transitions to be accurately recovered by the clock recovery PLL. The Out of Lock detector determines if RINP/RINN is within the frequency range of the clock recovery PLL. When CD is HIGH and RINP/RINN has sufficient transitions and is within the frequency range of the clock recovery PLL, the LFI output will be HIGH. Otherwise the LFI will be LOW.

RCLKP1/RCLKN1, ..., RCLKP4/RCLKN4 - Recovered Clock.
PECL.
These outputs represent the recovered clock from the RINP/RINN (Receive Input) for the respective channel. It is used to sample the RSERP/RSERN (Recovered Serial Data).

RSERP1/RSERN1, ..., RSERP4/RSERN4 - Recovered Serial Data. PECL.
These outputs represent the recovered data from the input data stream. The recovered data is aligned with the Recovered Clock.

OTHER

XTAL1, XTAL2.
Positive and negative reference crystal inputs. A 12.96 MHz crystal with the associated capacitors connected to these pins provides the necessary 51.84MHz or 155.52MHz TCLKP/TCLKN (Transmit clock) depending on the state of the RATESEL (Rate Select) pin for each channel.

PLLP1/PLLN1, ..., PLLP4/PLLN4 - Clock Recovery PLL Loop Filter.
External loop filter connections for the clock recovery PLLs of the respective channels. A 0.1µf capacitor and a 120Ω resistor in series are recommended between these pins.

PLLSP/PLLSN - Clock Synthesis PLL Loop Filter.
External loop filter connections for the clock synthesis PLL. A 0.1µf capacitor and a 500Ω resistor in series are recommended between these pins.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter		Rating	Unit
V_{CC}, TV_{CC}, AV_{CC}	Power Supply (GND, TGND, AGND = 0V)		0 to +7	VDC
V_I	Input Voltage (GND, TGND, AGND = 0V)		0 to V_{EE}	VDC
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range		0 to +75	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS — PECL

V_{CC}, TV_{CC}, AV_{CC} = +5V ±10%; GND, TGND, AGND = 0V, T_A = 0°C to +75°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	3.975	4.120	3.975	4.120	3.975	4.120	V
V_{OL}	Output LOW Voltage	3.190	3.380	3.190	3.380	3.190	3.380	V
V_{IH}	Input HIGH Voltage	3.835	4.120	3.835	4.120	3.835	4.120	V
V_{IL}	Input LOW Voltage	3.190	3.525	3.190	3.525	3.190	3.525	V
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA
I_{EE}	Total Power Supply Current	—	360	—	360	—	360	mA

DC ELECTRICAL CHARACTERISTICS — TTL

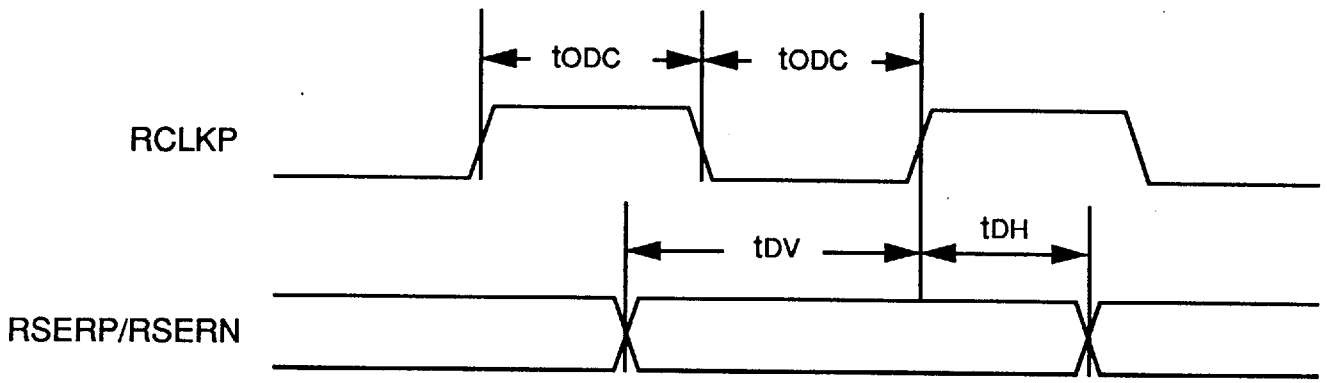
V_{CC}, TV_{CC}, AV_{CC} = +5V ±10%; GND, TGND, AGND = 0V, T_A = 0°C to +75°C

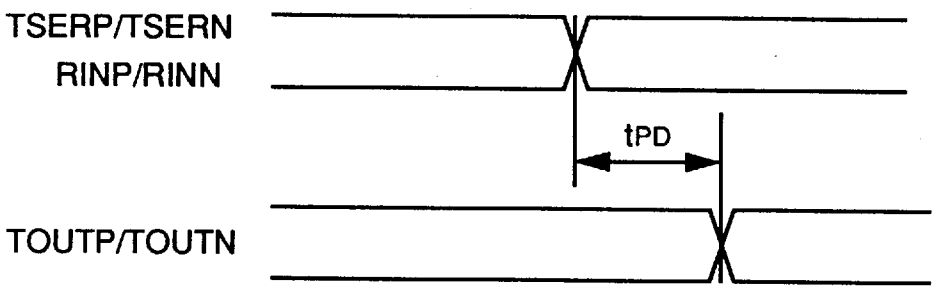
Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	—	V	I_{OH} = –2mA
V_{OL}	Output LOW Voltage	—	0.5	V	I_{OL} = 8mA
I_{OS}	Output Short Circuit Current	–150	–60	mA	V_{OUT} = Vcc
I_{EE}	Total Power Supply Current	—	360	mA	—

AC ELECTRICAL CHARACTERISTICS

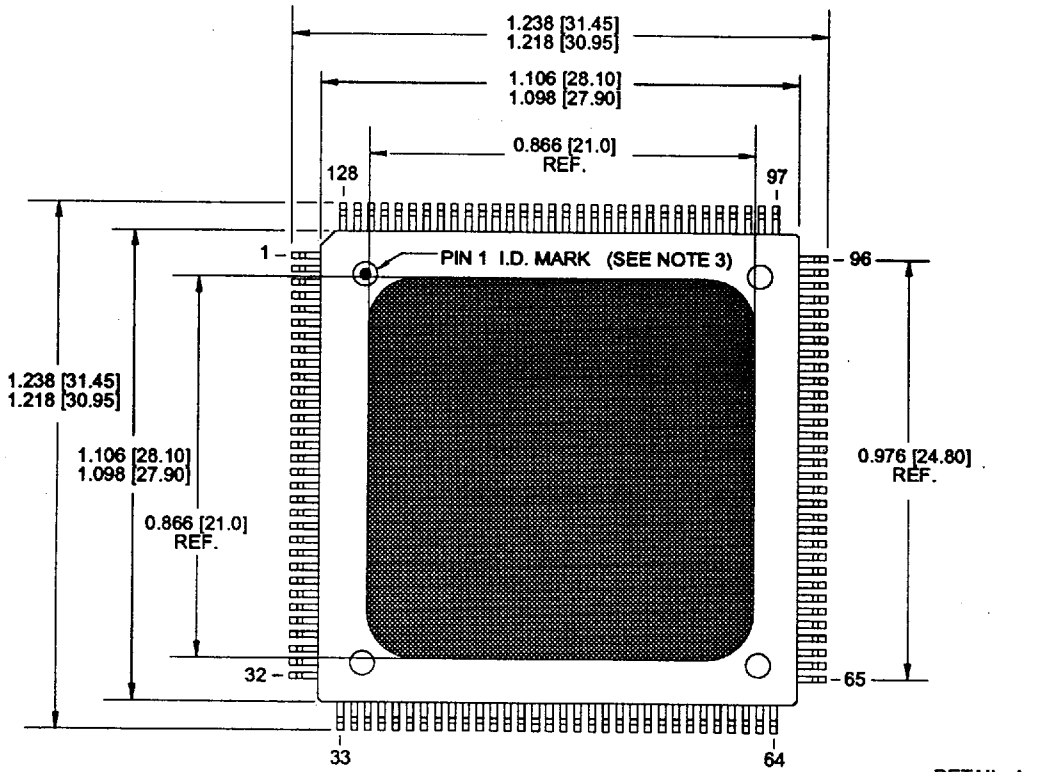
Parameter	Min.	Typ.	Max.	Units	Condition
VCO Center Frequency		155.52 ±2%		MHz	Nominal
Acquisition Lock Time			15	µsec	
TTL Output Rise/Fall Time			1.2	ns	10% t0 90% of amplitude, 30pF load
PECL Output Rise/Fall Time			500	ps	10% to 90%, 50Ω load, 5pF cap
tDV - Data Valid	3			ns	30pF load
tDH - Data Hold	1			ns	30pF load
tODC - Output Clock Duty Cycle (TCLKP/N, RCLKP/N)	45		55	% OF UI	
TPD - Prop Delay (TSER to TOUT, RIN, TOUT)	10.00			ns	

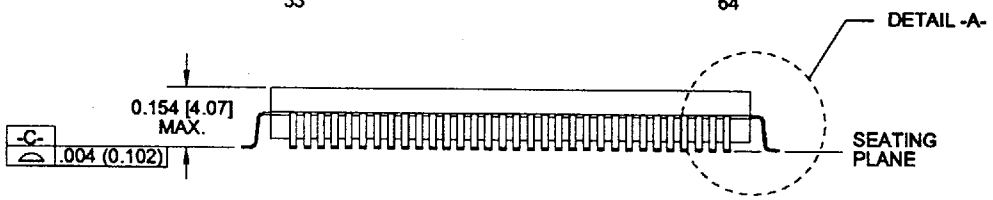
TIMING WAVEFORMS



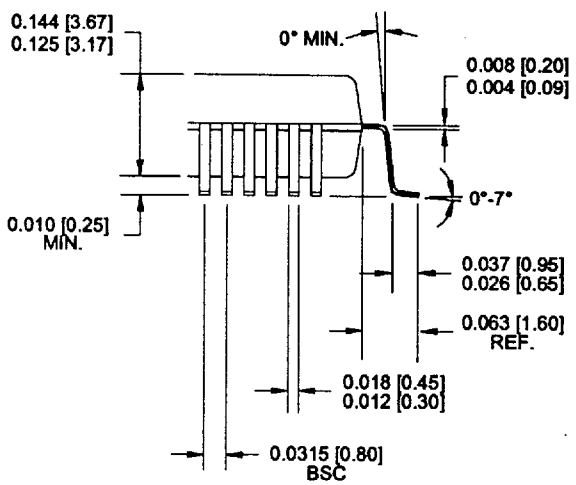


128 LEAD PLASTIC QUAD FLATPACK WITH HEAT SPREADER - DIE DOWN (R128-1)





DETAIL -A-



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. CONTROLLING DIMENSION: [MILLIMETERS].
3. THE PIN 1 ID MARK IS ROUNDED AT THE BOTTOM.
   THE REMAINING MARKS ARE FLAT AT THE BOTTOM.