

## 1 Megabit Module

## XM28C010

128K x 8 Bit

### 5 Volt, Byte Alterable E<sup>2</sup>PROM

#### TYPICAL FEATURES

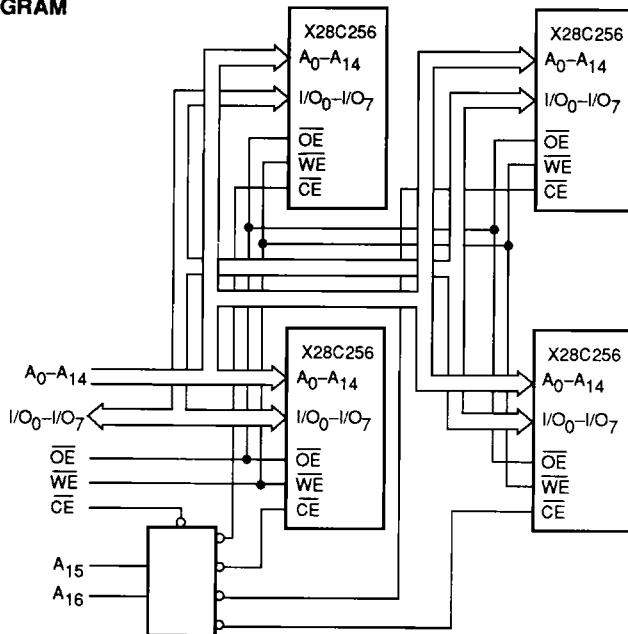
- High Density 1 Megabit (128K x 8) E<sup>2</sup>PROM Module
- Access Time of 120 ns at -55°C to +125°C
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>PP</sub> Control Circuits
  - Self Timed
    - No Erase Before Write
    - No Complex Programming Algorithms
    - No Overerase Problem
- Base Memory Component: Xicor CMOS X28C256
- JEDEC Standard 32-Pin 600 Mil Wide Ceramic Side Braze Package
- Pin Compatible with the X28C010 1Megabit Monolithic CMOS E<sup>2</sup>PROM

- Fast Write Cycle Times Supported by:
  - Internal Program Cycle 10 ms Max.
  - 64-byte Page
  - DATA Polling
  - Toggle Status Bit
- High Rel Module Available with:
  - 100% MIL-STD-883 Compliant Components
- Software Data Protection

#### DESCRIPTION

The XM28C010 is a high density 1 Megabit E<sup>2</sup>PROM comprised of four X28C256 32K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. The XM28C010 is configured 128K x 8 bit and features the JEDEC approved pinout for byte-wide memories, compatible with the monolithic X28C010.

#### FUNCTIONAL DIAGRAM



3871 FHD F01

# XM28C010

## DESCRIPTION (Cont.)

The XM28C010 is available in commercial, industrial, and military temperature ranges. The High Rel module is built with MIL-STD-883 Class B microcircuit components. In addition, after being assembled all High Rel modules undergo 100% screening.

The XM28C010 supports a 64-byte page write operation, this, combined with  $\overline{\text{DATA}}$  Polling or Toggle Bit testing, effectively provides a 78 $\mu\text{s}$ /byte write cycle, enabling the module memory array to be rewritten in 10 seconds.

The XM28C010 will also support Software Data Protection, a user-optional method of protecting data during power transitions.

The XM28C010 provides the same high endurance and data retention as the base memory components.

## PIN DESCRIPTIONS

### Addresses ( $A_0$ – $A_{16}$ )

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced (see Note 4).

### Output Enable ( $\overline{\text{OE}}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

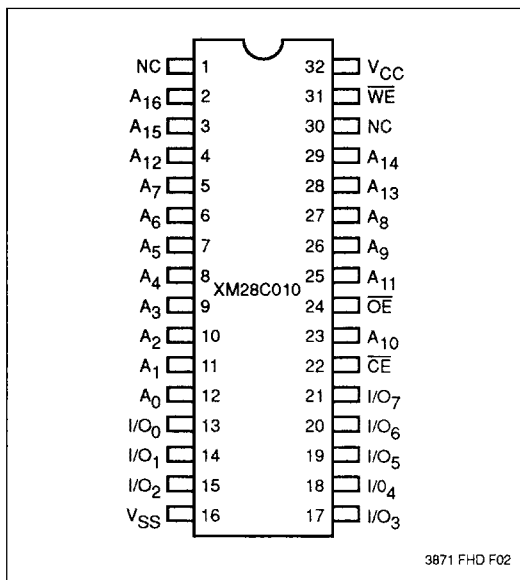
### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the XM28C010 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

The Write Enable input controls the writing of data to the XM28C010.

## PIN CONFIGURATION



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## PIN NAMES

Symbol	Description
$A_0$ – $A_{16}$	Address Inputs
$I/O_0$ – $I/O_7$	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
Vcc	+5V
Vss	Ground
NC	No Connect

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## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The XM28C010 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms (see Note 4).

### Page Write Operation

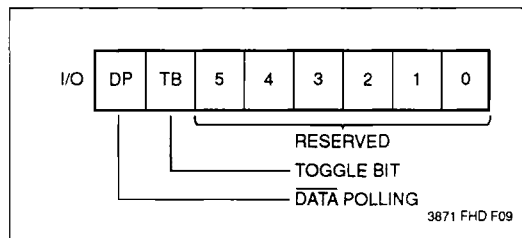
The page write feature of the XM28C010 allows the entire memory to be written in 10 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the XM28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{16}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

## Write Operation Status Bits

The XM28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



### DATA Polling (I/O<sub>7</sub>)

The XM28C010 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the XM28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data. Note: If the XM28C010 is in the protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### Toggle Bit (I/O<sub>6</sub>)

The XM28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

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## DATA POLLING I/O<sub>7</sub>

Figure 2. DATA Polling Bus Sequence

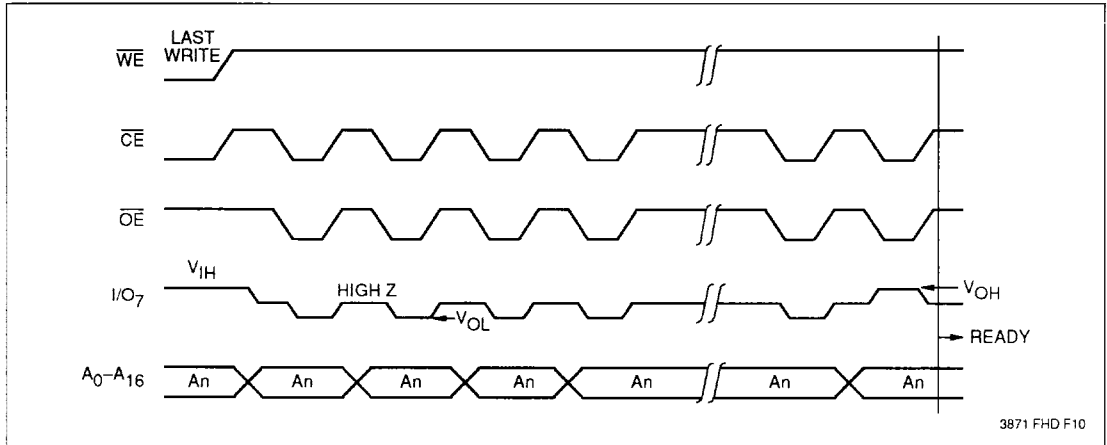
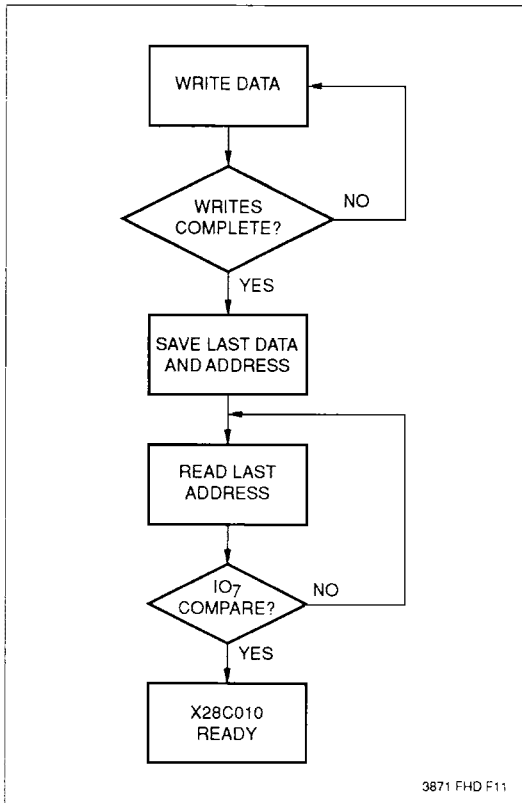


Figure 3. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the XM28C010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

# XM28C010

## THE TOGGLE BIT I/O<sub>6</sub>

Figure 4. Toggle Bit Bus Sequence

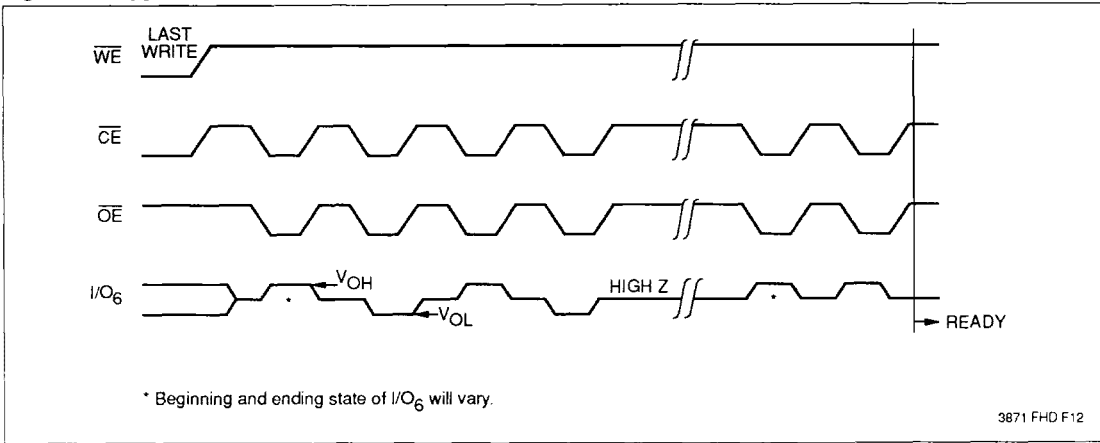
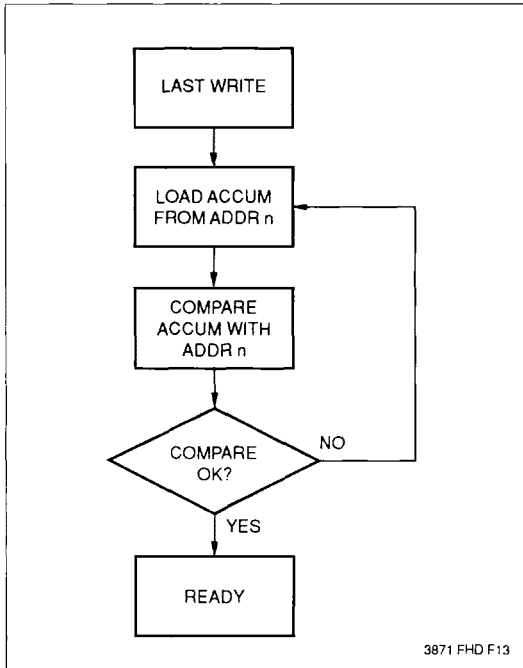


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple XM28C010 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## XM28C010

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### HARDWARE DATA PROTECTION

The XM28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse less than 10 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3V$ .
- Write Inhibit—Holding  $\overline{OE}$  LOW will prevent an inadvertent write cycle during power-on and power-off.

### SOFTWARE DATA PROTECTION

The XM28C010 does provide the Software Data Protection (SDP) feature. Because the module is comprised of four discrete X28C256 LCCs, the algorithm will differ from the algorithm employed for the monolithic 1 Mega-bit X28C010.

The module is shipped from Xicor with the Software Data Protection NOT ENABLED; that is, the module will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once  $V_{CC}$  is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Func-

tional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described in the next section.

### SOFTWARE COMMAND SEQUENCE

$A_{15}$  and  $A_{16}$  are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 6 and 7. Because this involves writing to a nonvolatile bit the device will become protected after  $t_{WC}$  has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 8 and 9. This is a nonvolatile operation, and the host will have to wait a minimum  $t_{WC}$  before attempting to write new data.

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## SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

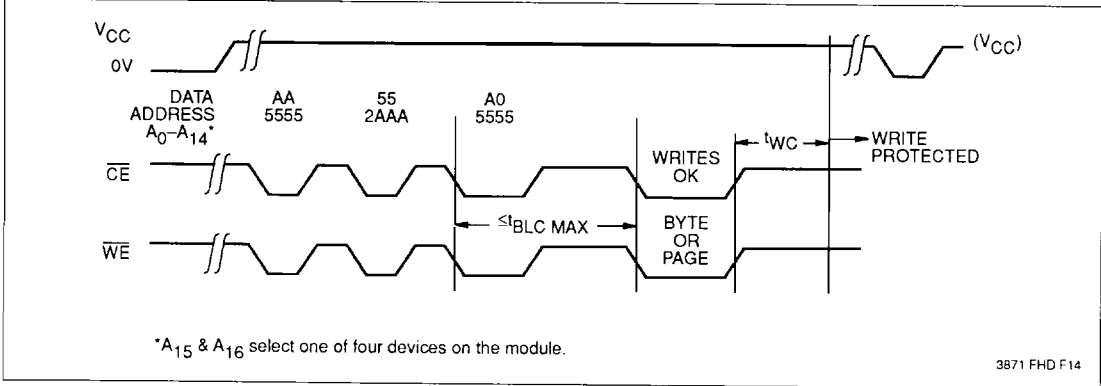
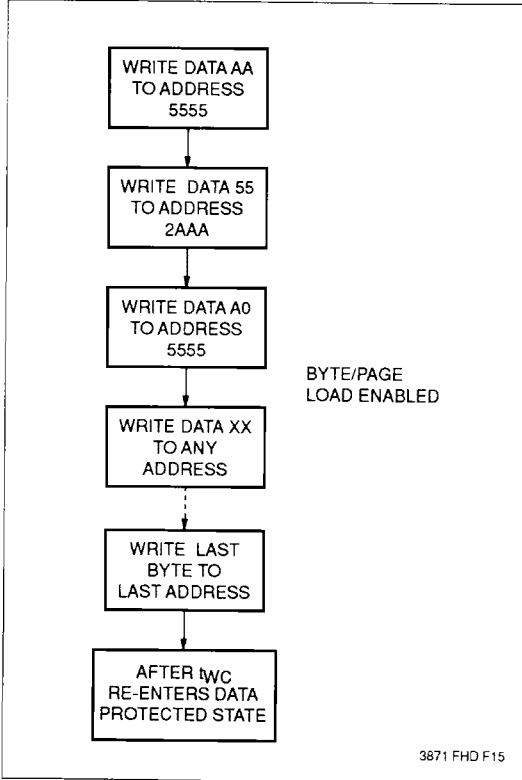


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.

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## RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

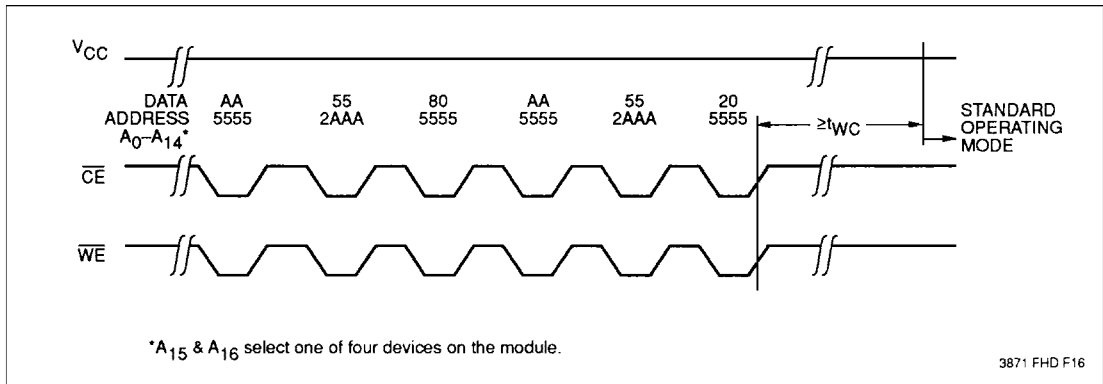
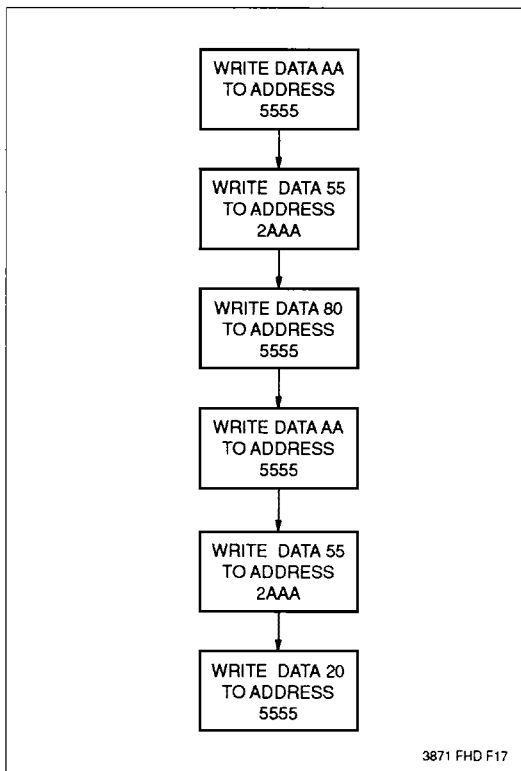


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the device will be in standard operating mode.

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## SYSTEM CONSIDERATIONS

Because the XM28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C010 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

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## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground .....	-1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. OPERATING CHARACTERISTICS

XM28C010  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

XM28C010I  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

XM28C010M  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) XM28C010-20-25		70	mA	CE = OE = V <sub>IL</sub> , WE = V <sub>IH</sub> , All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ f = 5MHz
	XM28C010-12-15		90		
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby) (TTL Inputs)		15	mA	CE = V <sub>IH</sub> , OE = V <sub>IL</sub> All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Current (Standby) -20-25 (CMOS Inputs) -12-15		800 2		
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , CE = V <sub>IH</sub>
V <sub>IL</sub>	Input Low Voltage	-1.0	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA

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## POWER-UP TIMING

Symbol	Parameter	Typ. <sup>(1)</sup>	Units
t <sub>PUR</sub> <sup>(2)</sup>	Power-up to Read Operation	100	μs
t <sub>PUW</sub> <sup>(2)</sup>	Power-up to Write Operation	5	ms

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**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = 5V$

Symbol	Test	Max.	Units	Test Conditions
C <sub>I/O</sub> <sup>(2)</sup>	Input/Output Capacitance	40	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance	24	pF	V <sub>IN</sub> = 0V

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**Notes:** (1) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

(2) This parameter is periodically sampled and not 100% tested.

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## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

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## MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	DOUT	Active
L	H	L	Write	DIN	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3871 PGM T06

## A.C. CHARACTERISTICS

XM28C010  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

XM28C010I  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

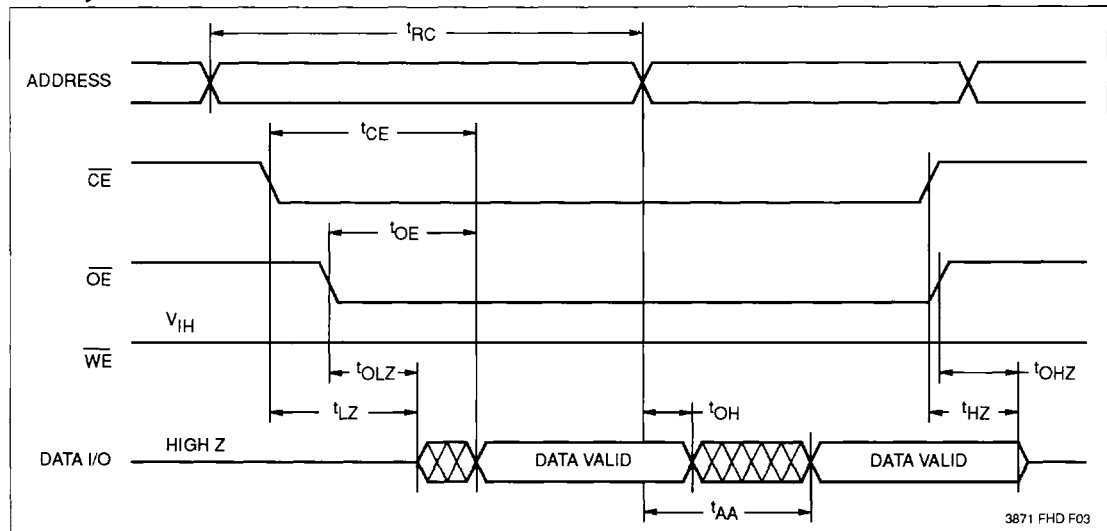
XM28C010M  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

### Read Cycle Limits

Symbol	Parameter	XM28C010-12		'-15		'-20		'-25		XM28C010		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	120		150		200		250		300		ns
$t_{CE}$	Chip Enable Access Time		120		150		200		250		300	ns
$t_{AA}$	Address Access Time		120		150		200		250		300	ns
$t_{OE}$	Output Enable Access Time		50		50		80		100		100	ns
$t_{LZ}^{(3)}$	CE Low to Active Output	0		0		0		0		0		ns
$t_{OLZ}^{(3)}$	OE Low to Active Output	0		0		0		0		0		ns
$t_{HZ}^{(4)}$	CE High to High Z Output		50		50		50		100		100	ns
$t_{OHZ}^{(4)}$	OE High to High Z Output		50		50		50		100		100	ns
$t_{OH}$	Output Hold from Address	0		0		0		0		0		ns

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### Read Cycle



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Note: (3)  $t_{LZ}$  and  $t_{OLZ}$  are shown for reference only, they are periodically characterized and are not 100% tested.

(4)  $t_{HZ}$  and  $t_{OHZ}$  are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven.

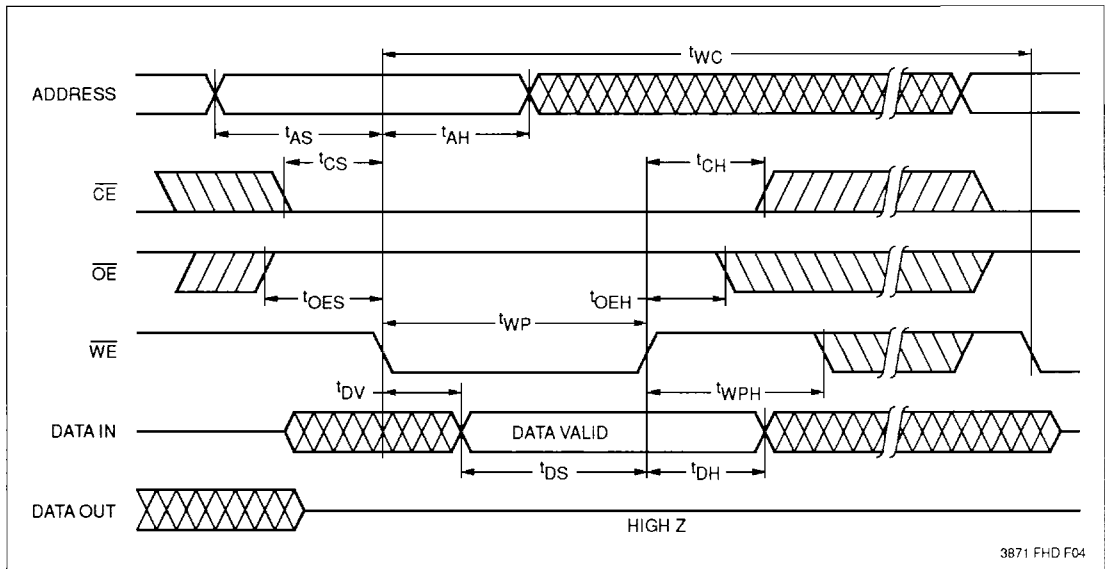
# XM28C010

## Write Cycle Limits

Symbol	Parameter	WE Controlled Write		CE Controlled Write <sup>(5)</sup>		Units
		Min.	Max.	Min.	Max.	
$t_{WC}^{(6)}$	Write Cycle Time		10		10	ms
$t_{AS}$	Address Setup Time	0		0		ns
$t_{AH}$	Address Hold Time	150		175		ns
$t_{CS}$	Write Setup Time	25		0		ns
$t_{CH}$	Write Hold Time	0		25		ns
$t_{CW}$	CE Pulse Width	125		100		ns
$t_{OES}$	OE High Setup Time	10		10		ns
$t_{OEH}$	OE High Hold Time	10		35		ns
$t_{WP}$	WE Pulse Width	100		125		ns
$t_{WPH}$	WE High Recovery	1		1		$\mu$ S
$t_{DV}$	Data Valid		1		1	$\mu$ S
$t_{DS}$	Data Setup	50		50		ns
$t_{DH}$	Data Hold	10		35		ns
$t_{DW}$	Delay to Next Write	10		10		$\mu$ S
$t_{BLC}$	Byte Load Cycle	1	100	1	100	$\mu$ S

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## WE Controlled Write Cycle

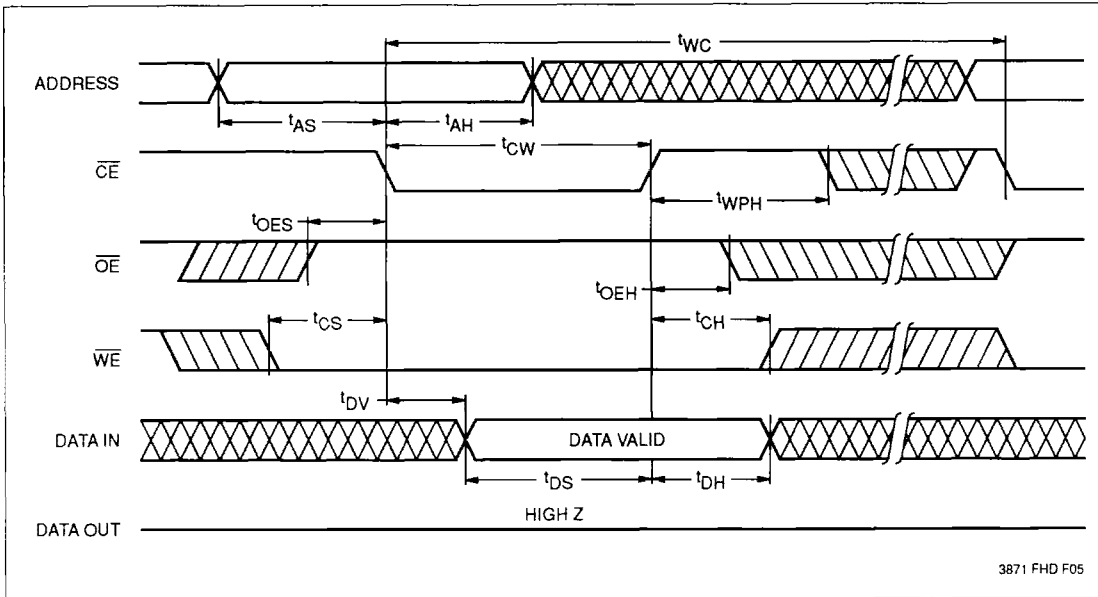


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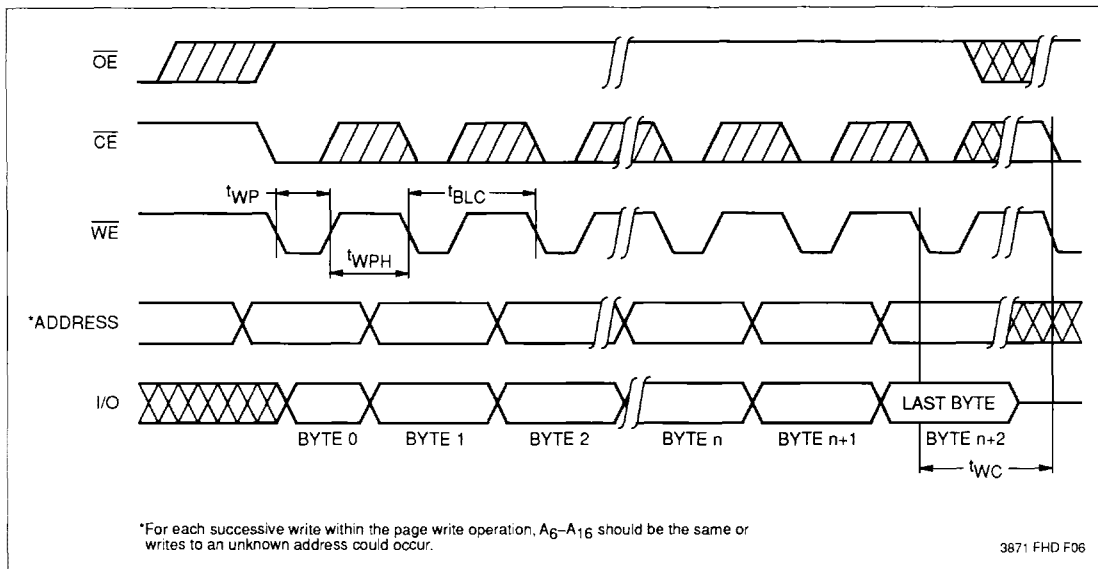
- Note:** (5) Due to the inclusion of the decoder IC on board the module the  $\overline{WE}$  and  $\overline{CE}$  write controlled timings will vary. When utilizing the  $\overline{CE}$  controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a  $\overline{WE}$  controlled write operation  $\overline{CE}$  must be a minimum 125 ns to accommodate the additional setup time required.
- (6)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the interval write operation.

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## $\overline{CE}$ Controlled Write Cycle

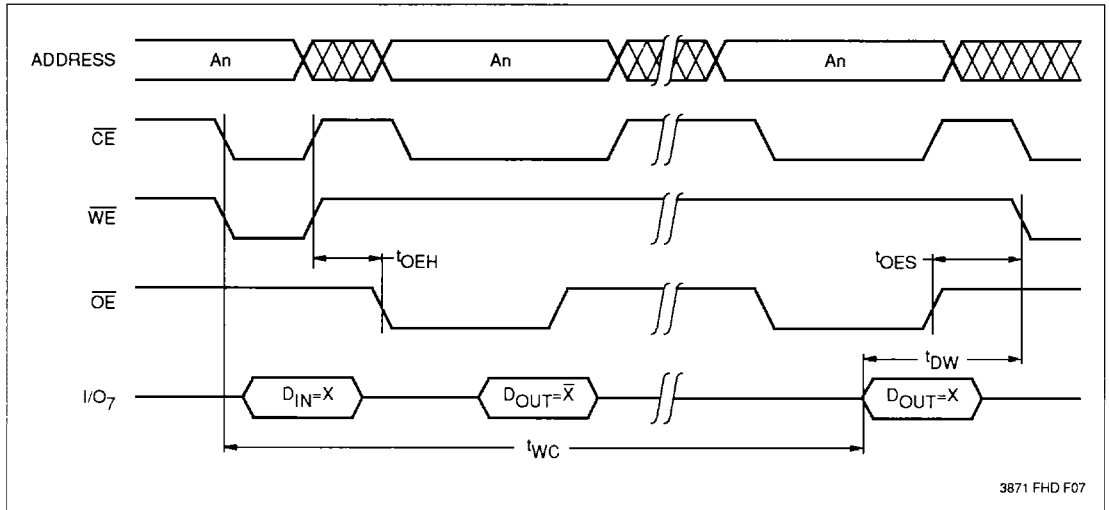


## Page Write Cycle

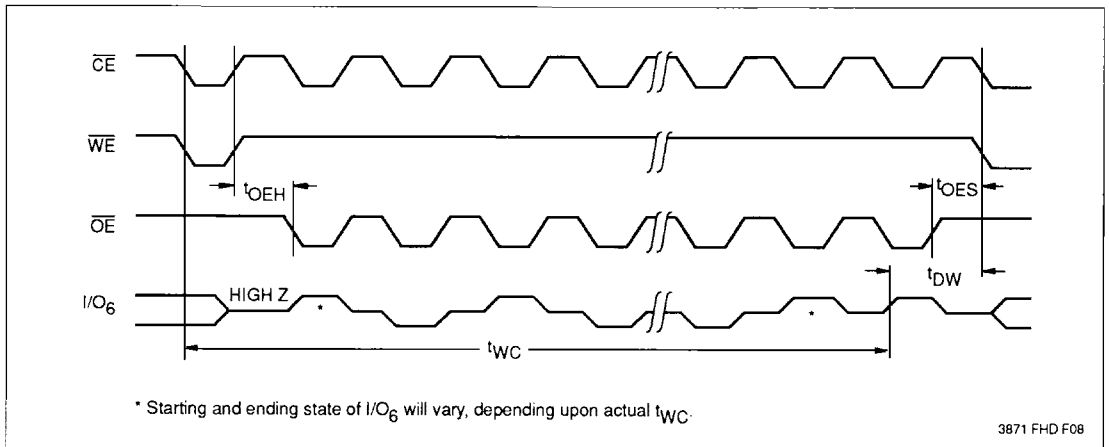


# XM28C010

## DATA Polling Timing Diagram








## Toggle Bit Timing Diagram



# XM28C010

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## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**XM28C010**

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**NOTES**