6 Operating Conditions

Table 10
Operating Conditions

Symbol	Parameter	min	max	Unit
V_{DD}	Supply voltage	3.0	4.6	V
T_{OP}	Operating temperature	-25 [1)]	70	°C

1) -25 °C is the technological limit. For consumer applications it is recommended to use a higher limit of 0 °C.

6.1 DC Parameters

Table 11
Electrical Parameters

Symbol	Parameter	min	max	Unit
I_{DD}	Supply current		t.b.d.	mA
C_I	Input capacitance of CLK, TCLK		200	fF
C_I	Input capacitance of all other inputs		15	fF
C_O	Output capacitance of DO, TDO		t.b.d.	fF

6.2 AC Parameters

The following table contains all timing parameters of the timing diagrams in the next chapters. The given values are pre-silicon and based on simulations with a high production yield as main design target.

Table 12
Timing Parameters

Symbol	Parameter	min	max	Unit	Notes
t_{CLL}	Clock low time	4		ns	
t_{CLH}	Clock high time	4		ns	
t_{CLR}	Clock rise time		1	ns	
t_{CLF}	Clock fall time		1	ns	
t_{SU}	Setup time	2		ns	
t_{HO}	Hold time	0		ns	

Symbol	Parameter	min	max	Unit	Notes
t_{SUL}	Setup time for LATENCY	2		clocks	
t_{HOL}	Hold time for LATENCY	2		clocks	
t_{ZHL}	Delay time, buffer tri-state to buffer active		3	ns	
t_{HLZ}	Delay time, buffer active to buffer tri-state		3	ns	
t_{RLO}	Reset low time with inactive memory	200		ns	
t_{RVV}	Delay time from RESET inactive to first ACTIVATE	200		ns	
t_{APD}	Delay time between ACTIVATE and PRECHARGE	30		ns	
$t_{PAD\ (1)}$	Delay time between PRECHARGE and ACTIVATE of same row	30	see t_{PAD} (2)	ns	1)
$t_{PAD\ (2)}$	Refresh period for one memory row	see t_{PAD} (1)	64	ms	2)
t_{ACD}	Delay time between ACTIVATE and COLUMN operation to the same bank	25		ns	
t_{CL1}	Clock period for LATENCY 1	19+n		ns	3)
t_{AA1}	Address access time for LATENCY 1	44+n		ns	3)
t_{CO1}	Clock to valid output delay at LATENCY 1		19+n	ns	3),4)
t_{DH1}	Clock to output hold at LATENCY 1	2		ns	
t_{MO1}	Modify time: t_{CL1} - t_{CO1} - t_{SU}				
t_{CL2}	Clock period for LATENCY 2	15+n		ns	3)
t_{AA2}	Address access time for LATENCY 2	42+n		ns	3)
t_{CO2}	Clock to valid output delay for LATENCY 2 and LATENCY 3		4	ns	4)
t_{DH2}	Clock to output hold at LATENCY 2	2		ns	
t_{MO2}	Modify time: t_{CL2} - t_{CO2} - t_{SU}				
t_{CL3}	Clock period for LATENCY 3	12+n		ns	3)
t_{AA3}	Address access time for LATENCY 3	42+n		ns	3)

Symbol	Parameter	min	max	Unit	Notes
t_{CP3}	Delay between COLUMN operation and PRECHARGE to the same bank, LATENCY 3	2 * t_{CL3}			5)
t_{MO3}	Modify time: t_{CL3} - t_{CO2} - t_{SU}				

1) The same parameter is relevant for the refresh period.

2) During the refresh period all 256 rows of one memory block must be activated and precharged.

3) If the number of memory blocks in a memory stripe is less or equal than 4 then n = 0. For all other values *n = (number of blocks in stripe) - 4.*

4) Output load 1 pF

5) Due to LATENCY 3 a rising clock edge is required during t_{CP3}.

7 Maximum Ratings

Stresses above those listed in the table below may cause permanent damage to the device. Exposure to conditions beyond those indicated below may affect device reliability.

This is a stress rating only and functional operation of the device under these conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied. It is not implied, that more than one of these conditions can be applied simultaneously.

Table 13
Maximum Ratings

Parameter	Limit Values		Unit
	min.	max.	
positive Supply Voltage	3.0	4.6	V
Voltage applied at any input	tbd	tbd	V

8 Environmental Requirements

8.1 Storage and Transportation

The rated (limited capability) storage and transportation temperature range prior to printed board assembly shall be - 50 to +150°C (without supply voltage)

8.2 Operating Ambient

The operating ambient temperature shall be within 0 °C to +70 °C