Z86C40

CMOS Z8® 4K ROM CCP™ CONSUMER CONTROLLER PROCESSOR

FEATURES

- 8-Bit, CMOS MCU with 4 Kbytes of ROM and 256 Bytes of RAM (236 Bytes for General Purpose)
- Package Styles: 40-Pin DIP, 44-Pin PLCC, 44-Pin QFP
- Software Programmable Low EMI Modes
- Programmable Open-Drain Mode on Port 0, Port1, and Port 2
- Low-Power Consumption: 40 mW (Typical @ 5.0V)
- Fast Instruction Pointer: 750 ns @ 16 MHz
- Two Standby Modes: STOP and HALT
- 32 Input/Output Lines (Three with Comparator Inputs)
- 25 Digital CMOS Level, Schmitt-Triggered Inputs
- Three Digital CMOS Level Inputs
- Three Expanded Register File Control Registers
- Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speeds up to 12 MHz and 16 MHz
- Low Voltage Protection
- Watch-Dog/Power-On Reset Timers
- Permanently Enabled WDT Option
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- RAM and ROM Protect
- Programmable Interrupt Polarity
- Auto Latches

GENERAL DESCRIPTION

The Z86C40 CCP™ (Consumer Controller Processor) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 4 Kbytes of ROM and 236 bytes of general-purpose RAM, this low cost, low power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C40 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File (ERF) to allow access to register mapped peripheral and I/O circuits. The Z86C40 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial, automotive, computer peripherals, and consumer applications.

With ROM/ROMless selectivity, the Z86C40 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

GENERAL DESCRIPTION (Continued)

For applications demanding powerful I/O capabilities, the Z86C40 provides 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each, and are configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory (Figure 1).

Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File (ERF). The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The Expanded Register File consists of two control registers.

To unburden the system from coping with the real-time tasks, such as counting/timing and data communication, the Z86C40 offers two on-chip counter/timers with a large number of user-selectable modes. Additionally, two on-board comparators allow analog signals to be processed using a common reference voltage.

Note: All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

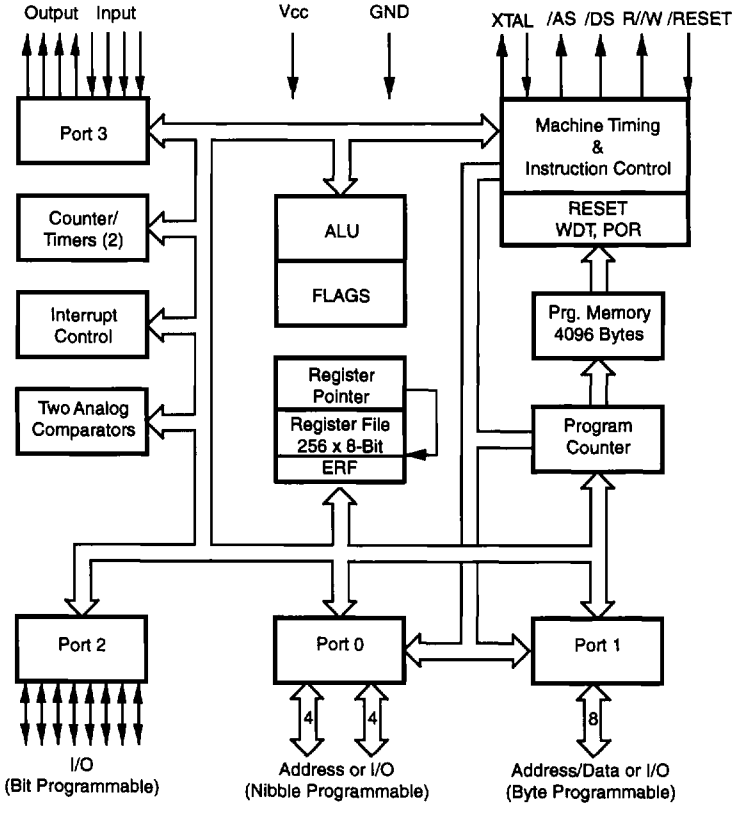


Figure 1. Functional Block Diagram

PIN DESCRIPTION

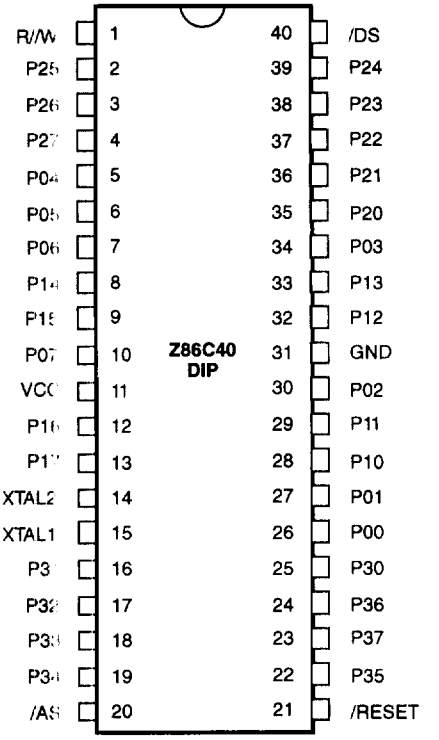


Figure 2. 40-Pin DIP Pin Configuration

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	R/W	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	In/Output
5-7	P04-P06	Port 0, Pins 4,5,6	In/Output
8-9	P14-P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	In/Output
28-29	P10-P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

PIN DESCRIPTION (Continued)

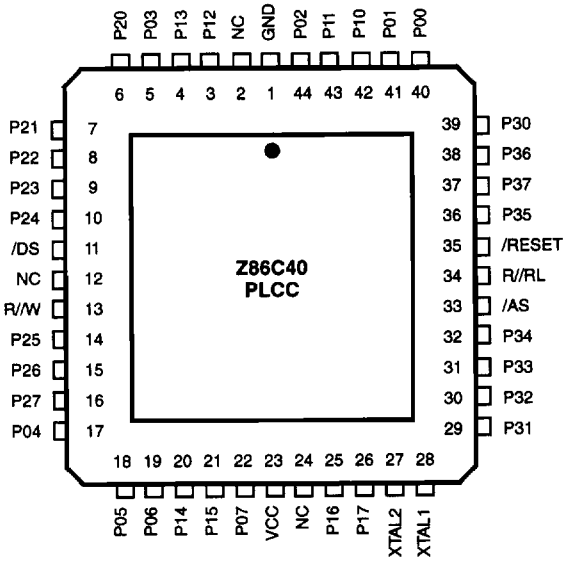


Figure 3. 44-Pin PLCC Pin Configuration

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	GND	Ground	
2	NC	Not Connected	
3-4	P12-P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	NC	Not Connected	
13	R/W	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	In/Output
17-19	P04-P06	Port 0, Pins 4,5,6	In/Output
20-21	P14-P05	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23	V_{CC}	Power Supply	
24	NC	Not Connected	
25-26	P16-P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless select	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	In/Output
42-43	P10-P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

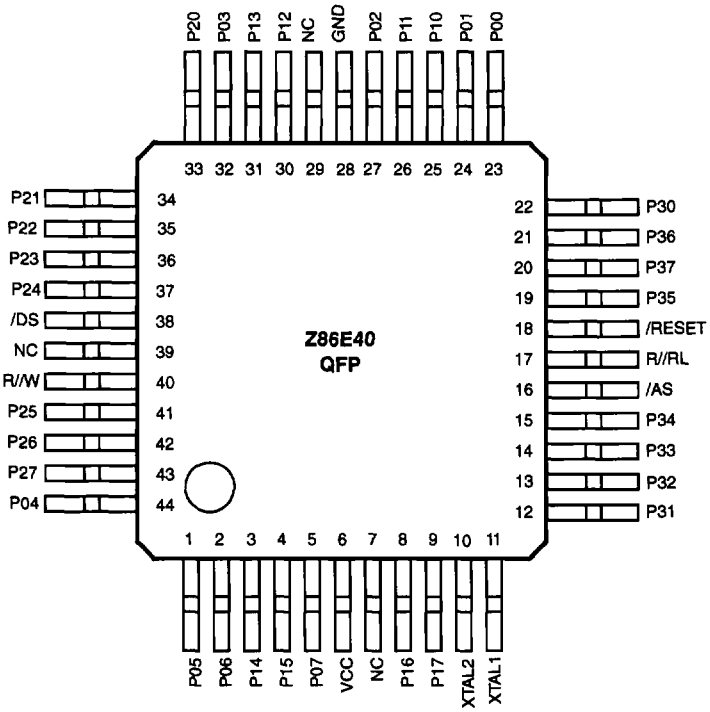


Figure 4. 44-Pin QFP Pin Configuration

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	In/Output
3-4	P14-P05	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6	V_{CC}	Power Supply	
7	NC	Not Connected	
8-9	P16-P17	Port 1, Pins 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output

Pin #	Symbol	Function	Direction
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pin 0,1	In/Output
25-26	P10-P11	Port 1, Pins 0,1	In/Output
27	P02	Port 0, Pin 2	In/Output
28	GND	Ground	
29	NC	Not Connected	
30-31	P12-P13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	NC	Not Connected	
40	R/W	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

PIN FUNCTIONS

/ROMless (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90/C89 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions normally as a Z8 ROM version).

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network, or an external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/W (output, write Low). Read/Write, the R/W signal is Low when the Z86C40 is writing to the external program or data memory.

Port 0 (P00-P07). Port 0 is an 8-bit, bidirectional, CMOS compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03-P00 input/output and P07-P04 input/output), or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 is set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R/W (Figure 5).

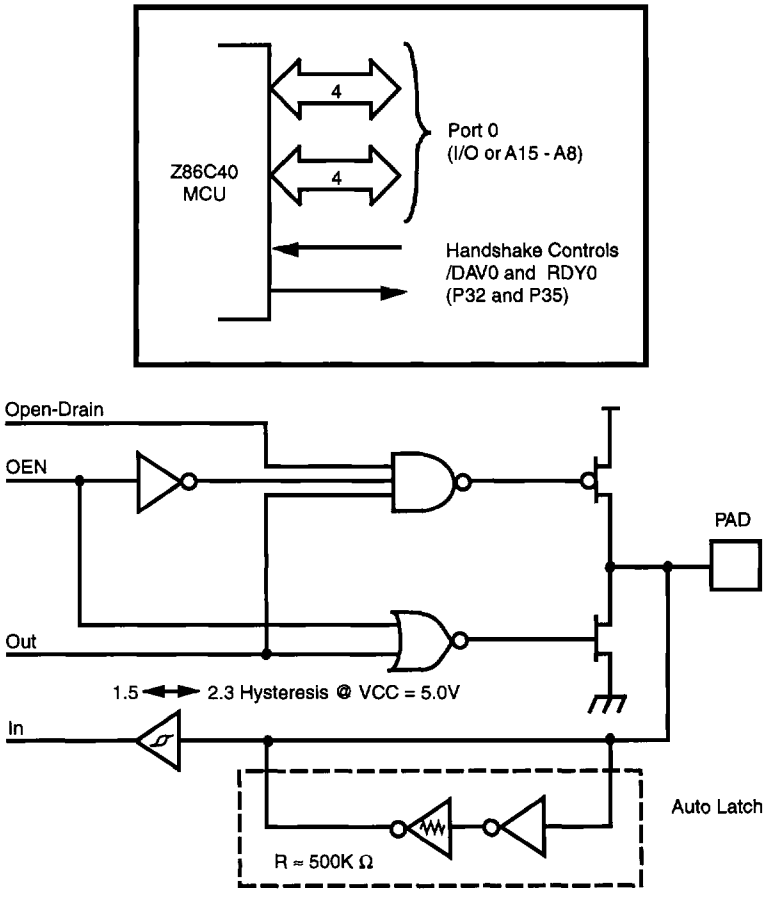


Figure 5. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P10-P17). Port 1 is an 8-bit, bidirectional, CMOS compatible port (Figure 6), with multiplexed Address (A7-A0) and Data (D7-D0) ports. For the Z86C40 ROM device, these eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and byte-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software.

Port 1 may be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). Memory locations greater than 4095 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the Z86C40 to share common resources in multiprocessor and DMA applications.

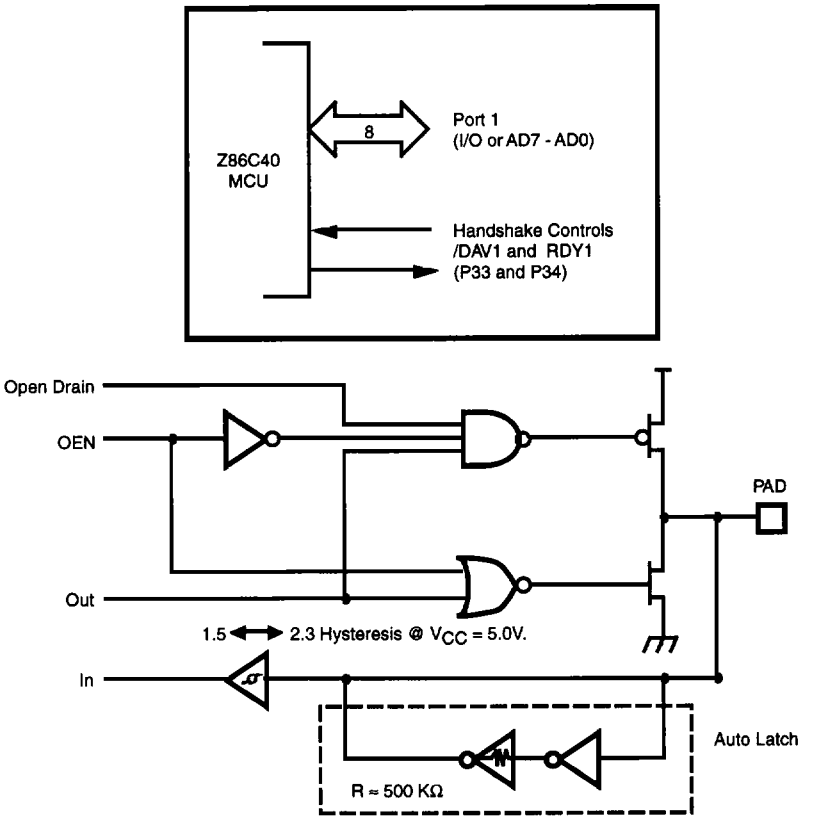


Figure 6. Port 1 Configuration

Port 2 (P20-P27). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software.

Port 2 may be placed under handshake control. In this Handshake Mode, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 7).

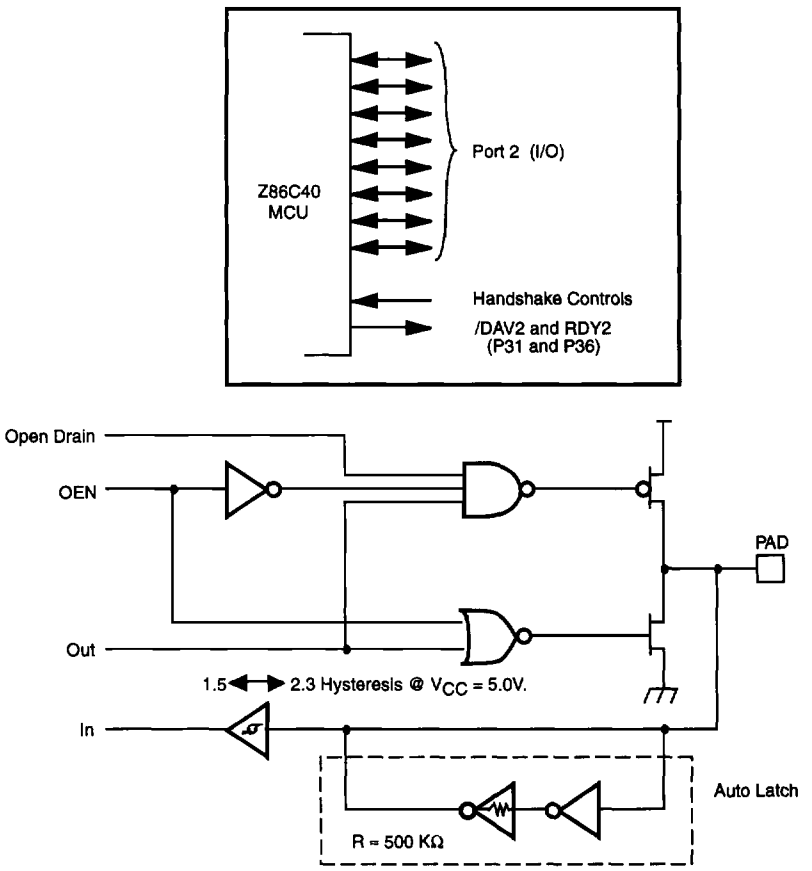


Figure 7. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P30-P37). Port 3 is an 8-bit, CMOS compatible, four fixed inputs (P30-P33) and four fixed outputs (P34-P37), and is configured under software control for Input/Output, Counter/Timers, interrupt, port handshake, and Data Memory functions. Port 3, pin 0 input is Schmitt-triggered, and pins P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, P36, P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, pin 0 and pin 3 are falling edge interrupt inputs. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7). P33 is the comparator reference voltage input when in Analog Mode. Access to Counter/Timers 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}); Data Memory Select (/DM, see Table 4, Figure 37).

P34 output can be software-programmed to function as a Data Memory Select (DM). The Port 3 mode register (P3M) bit D3, D4 selects this function. When accessing external Data Memory, the P34 goes active Low; when accessing external program memory, the P34 goes High.

Table 4. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-OUT			R/D		/DM
P35	OUT				R/D			
P36	OUT	T_{OUT}					R/D	
P37	OUT		AN2-OUT					

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Auto Latch. The Auto-Latch instruction puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Note: Deletion of all Port Auto Latches is available as a ROM Mask option. The Auto Latch Delete option is selected by the customer when the ROM code is submitted.

Comparator Inputs. Port 3, Pins P31 and P32 each have a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source. P34 and P37 outputs the comparator outputs by software-programming the PCON Reg. bit D0 to 1.

/RESET (input, active Low). Initializes the MCU. Reset is accomplished either through Power-On Reset, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Reset, the internally generated reset is driving the reset pin Low for the POR time. ***Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions.*** Pull-up is provided internally.

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86C40 is equipped with a reset filter of four external clocks (4 TpC). If the external reset signal is less than 4 TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000C (HEX), 5-10 TpC cycles after the RST is released. For Power-On Reset, the reset output time is T_{POR} ms.

Once program execution begins, /AS and /DS toggles only for external memory accesses. The Z86C40 does not reset WDTMR, SMR, P2M, PCON, and P3M registers on a STOP-Mode Recovery operation.

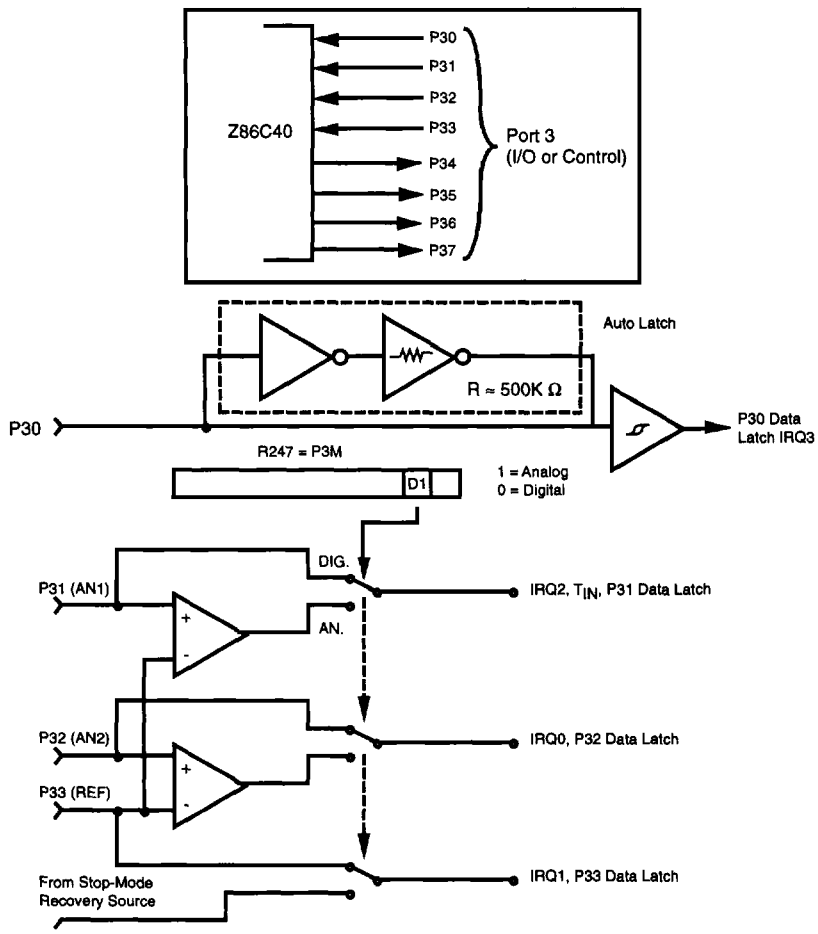


Figure 8a. Port 3 Configuration

PIN FUNCTIONS (Continued)

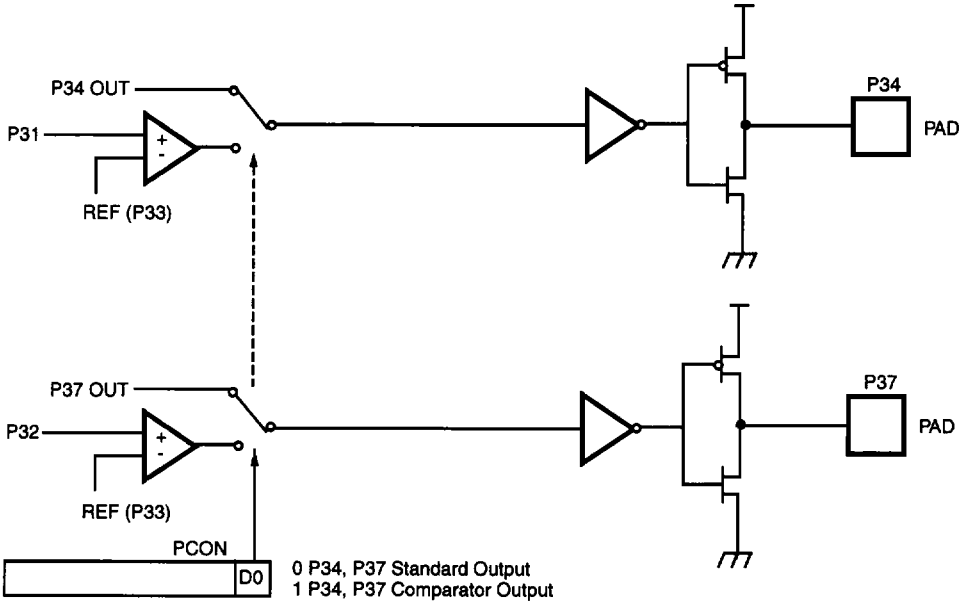


Figure 8b. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z86C40 MCU incorporates the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset
- Low Voltage Recovery

Auto Power-On Reset circuitry is built into the Z86C40, eliminating the need for an external reset circuit to reset upon power-up. The internal pull-up resistor is on the Reset pin, so a pull-up resistor is not required; however, in high EMI (noisy) environment, it is recommended that a small value pull-up resistor be used.

Program Memory. The Z86C40 addresses up to 4 Kbytes of internal program memory and 60 Kbytes of external memory (Figure 9). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, address 12 to address 4095 consists of on-chip mask-programmed ROM. At addresses 4096 and greater, the Z86C40 executes external program memory fetches through Port 0 and Port 1 in Address/Data mode.

The 4 Kbyte program memory is mask programmable. ***A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to Program Memory in all modes. ROM look-up tables cannot be used with this feature.***

The ROM Protect option is mask-programmable, to be selected by the customer when the ROM code is submitted.

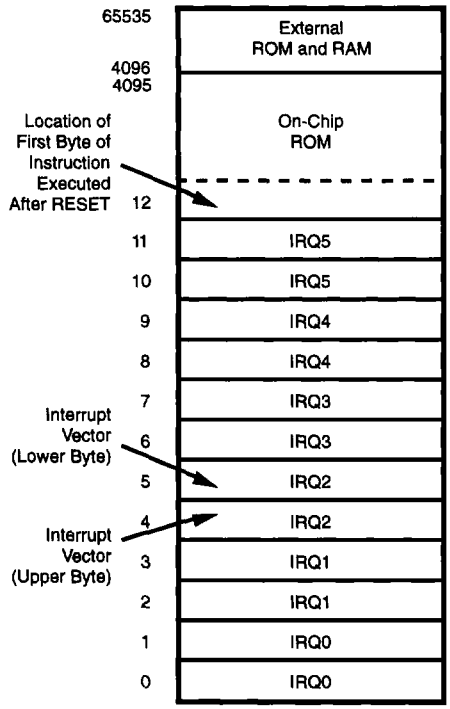


Figure 9. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Data Memory (/DM). The Z86C40 ROM version can address up to 60 Kbytes of external data memory beginning at location 4096. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 10). The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode.

Expanded Register File (ERF). The Z86C40 register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group (Figure 11). These register groups are known as the Expanded Register File (ERF). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 12). Three system configuration registers reside in the Expanded Register File at Bank F (PCON, SMR, WDTMR). The rest of the Expanded Register is not physically implemented, and is open for future expansion.

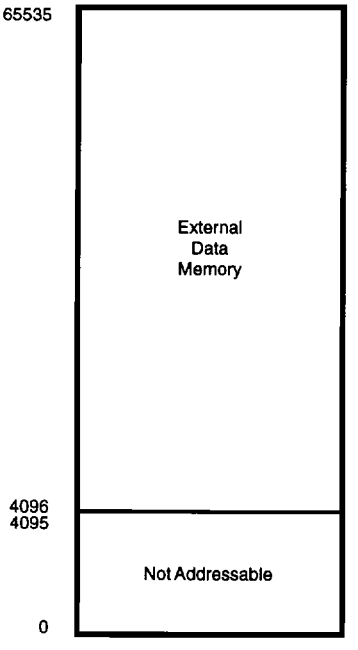


Figure 10. Data Memory Map

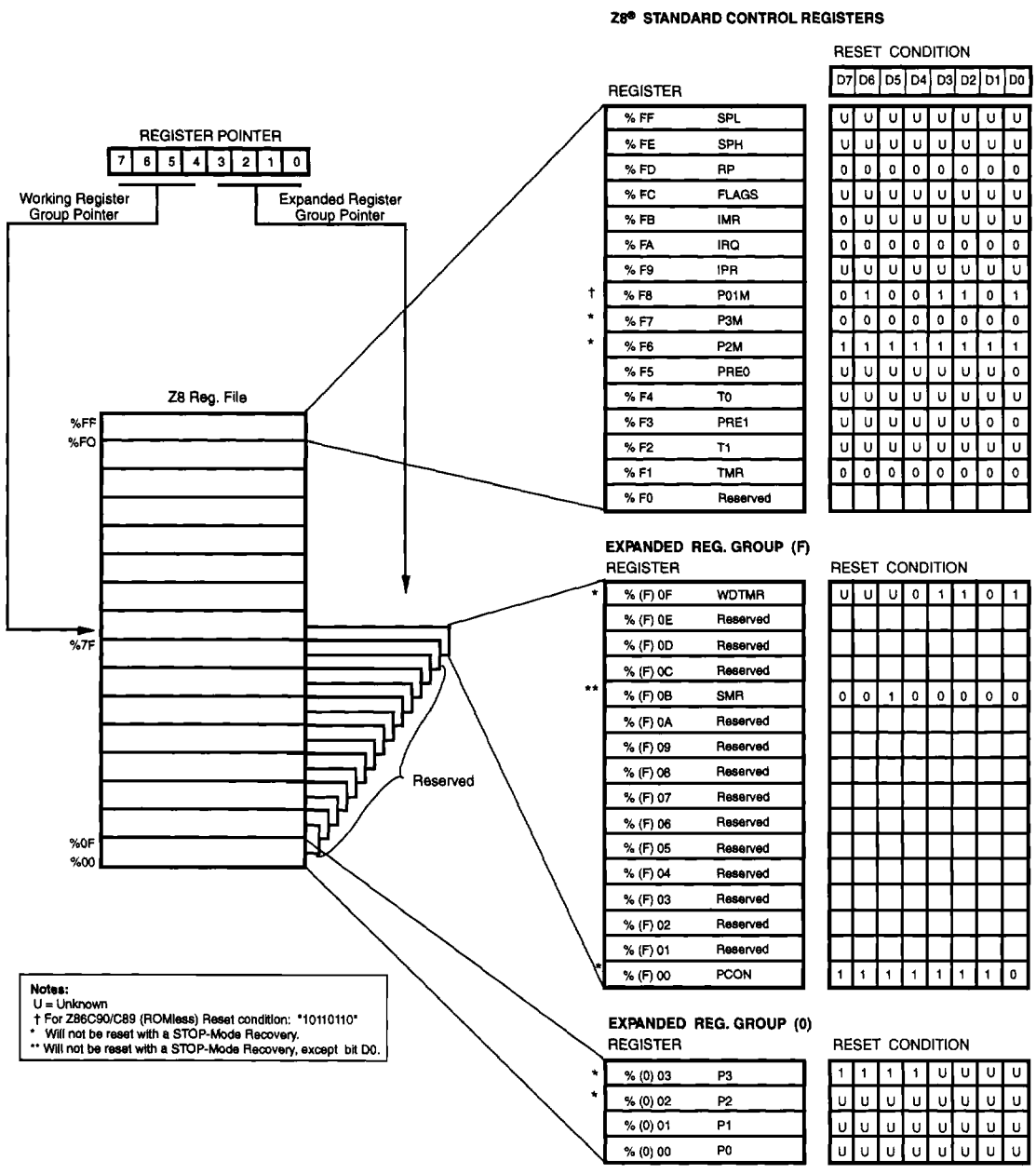


Figure 11. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

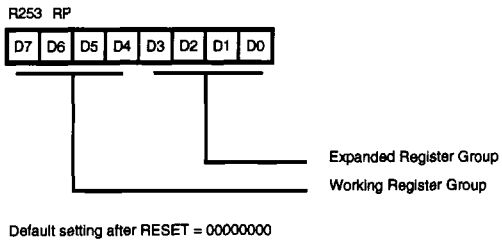


Figure 12. Register Pointer Register

Register File. The register file consists of four I/O port registers, 236 general-purpose registers and 15 control and status registers (R0-R3, R4-239 and R240-R255, respectively), plus three system configuration registers in the expanded register group. The instructions access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 13). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

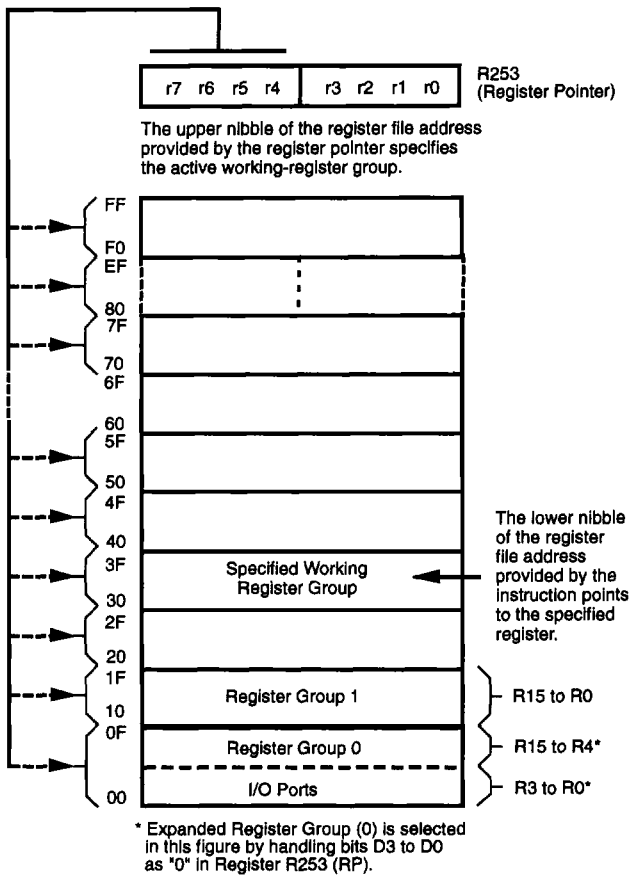


Figure 13. Register Pointer

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V.

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the IMR register, bit D6. A 1 in D6 enables RAM Protect.

Stack. The Z86C40 external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). SPH is used as a general-purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 14).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, ***but not the prescalers***, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

FUNCTIONAL DESCRIPTION (Continued)

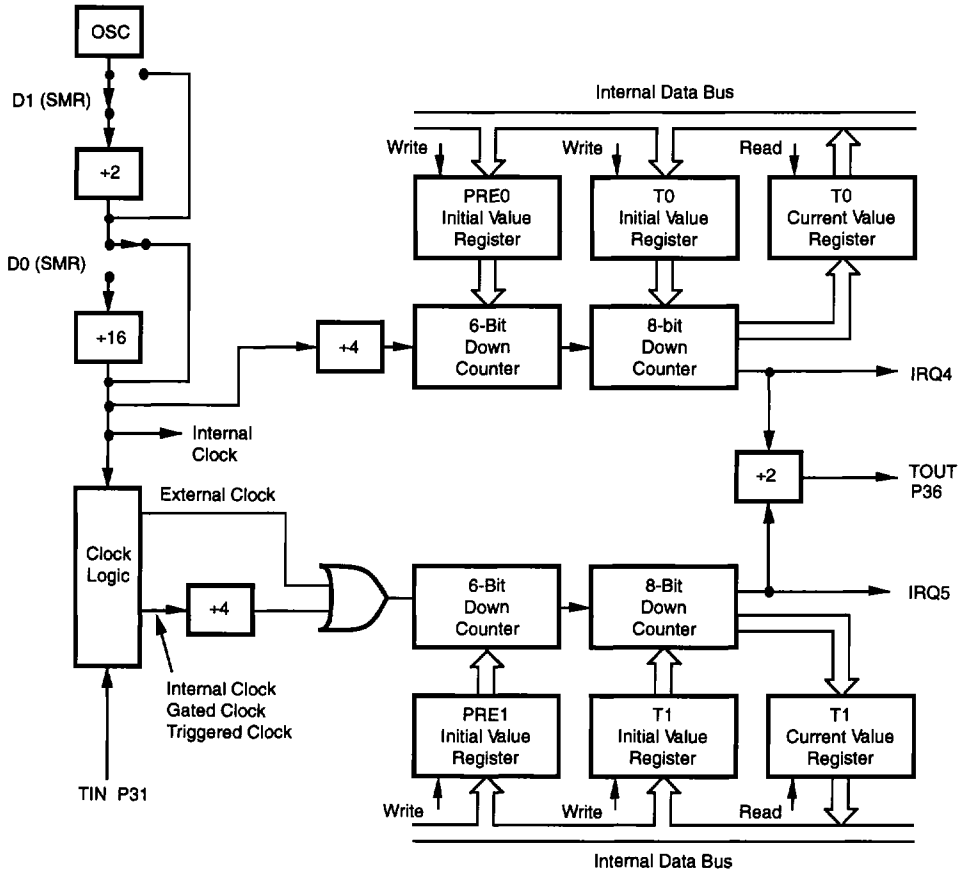


Figure 14. Counter/Timer Block Diagram

Interrupts. The Z86C40 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 15) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 5). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

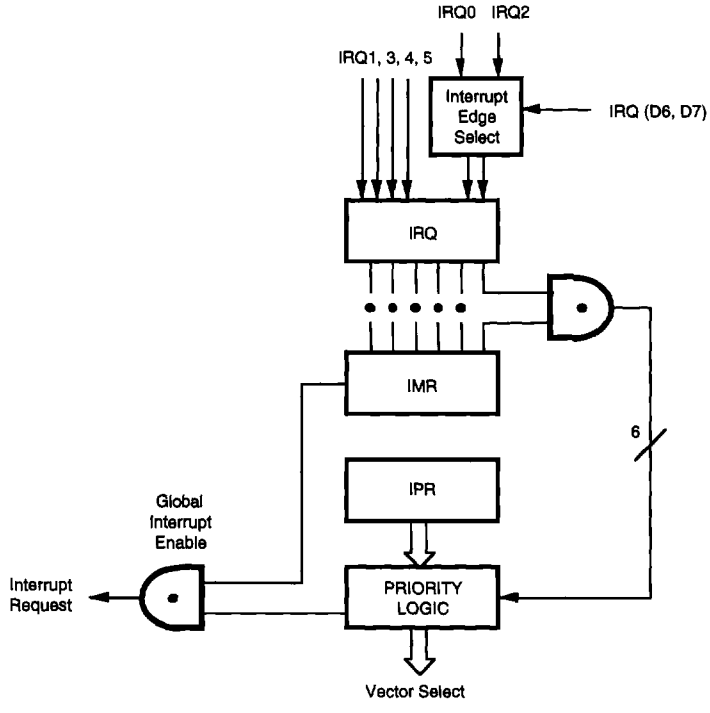


Figure 15. Interrupt Block Diagram

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

FUNCTIONAL DESCRIPTION (Continued)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z86C40 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6 . The configuration is shown in Table 6.

Table 6. IRQ Register

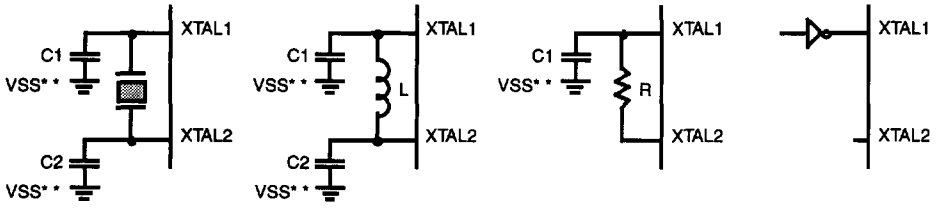
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86C40 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator. The RC oscillator option is mask-programmable on the Z86C40 and is selected by the customer at the time when the ROM code is submitted. (Note that the RC option is available up to 8 MHz.) The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 16).

Note: For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

LC
C1, C2 = 22 pF

L = 130 uH *
f = 3 MHz *

RC
@ 5V VCC (TYP)

C1 = 33 pF *
R = 1K *
f = 6 MHz *

External Clock

* Preliminary value including pin parasitics
* * Device ground pin

Figure 16. Oscillator Configuration

Power-On-Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. STOP-Mode Recovery (if D5 of SMR=1).
3. WDT timeout.

The POR time is a specified as T_{POR}. Bit 5 of the STOP-Mode Register determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be enabled and executed to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
          or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation. It also reduces the standby current to 10 µA or less. The STOP mode is terminated by a reset only, either by WDT timeout, POR, SMR recovery, or external reset. This causes the processor to restart the application program at address 000C (HEX).

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2, and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 17).

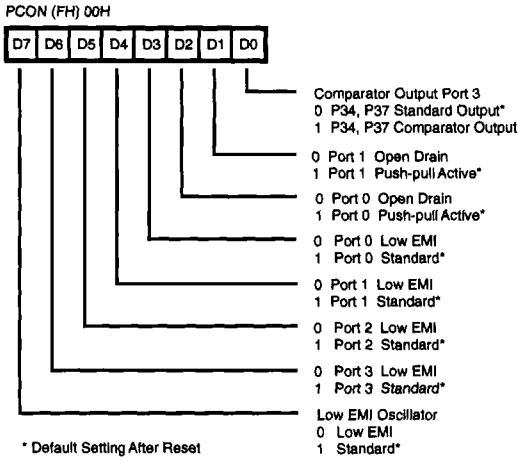


Figure 17. Port Configuration Register (PCON) (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** Maximum external clock frequency of 4 MHz when running in the low EMI oscillator mode.

Low EMI Emission. The Z86C40 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Figure 18). All bits are Write Only, except bit 7 which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the STOP-Mode Recovery signal. Bits 0 and 1 determine the timeout period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

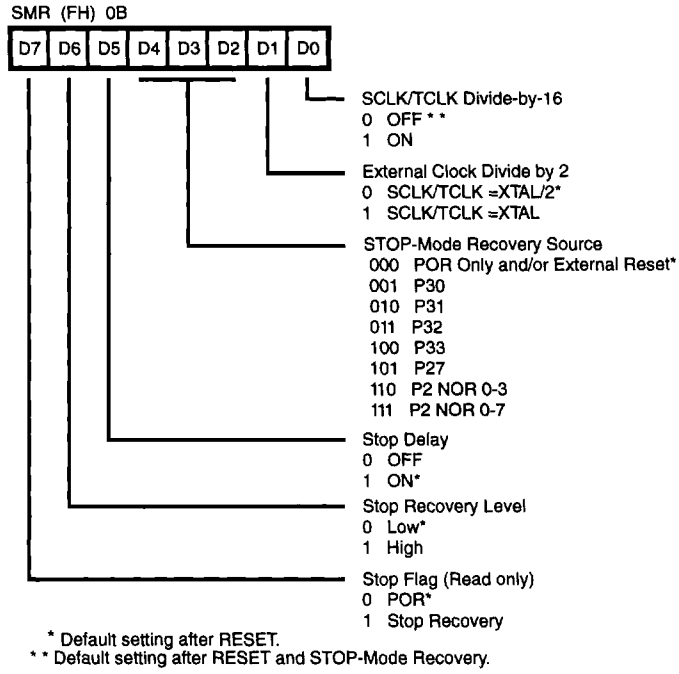


Figure 18. STOP-Mode Recovery Register (Write Only Except Bit D7, Which Is Read Only)

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero. Maximum external clock frequency is 4 MHz when SMR Bit D1 = 1 where SCLK/TCLK = XTAL.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 19 and Table 7).

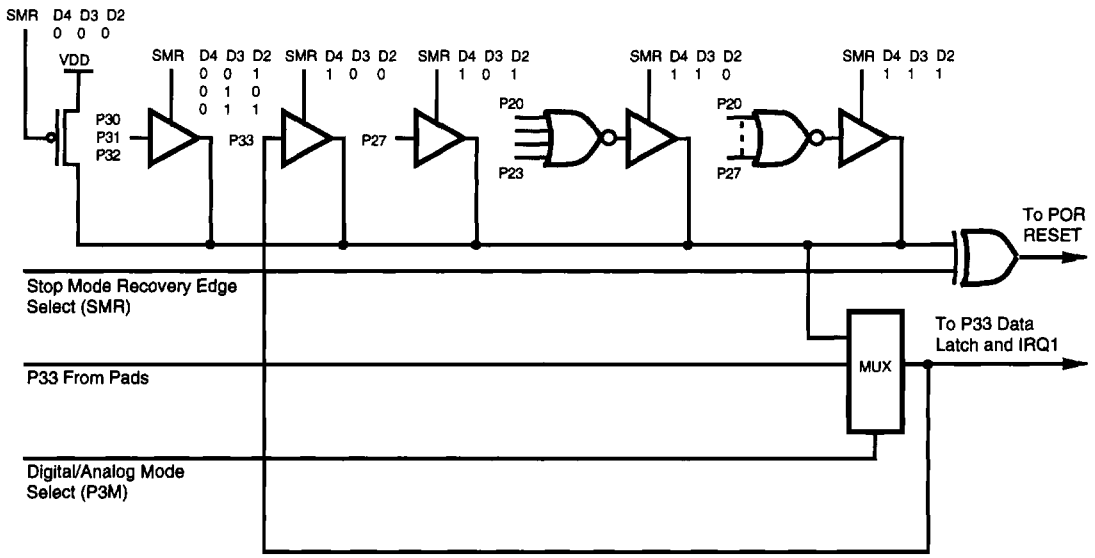


Figure 19. STOP-Mode Recovery Source

Table 7. STOP-Mode Recovery Source

SMR:432 D4	D3	D2	Operation Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

STOP-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR}/RESET delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source is kept active for at least 5 TpC.

STOP-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z86C40 from STOP mode. A 0 indicates low-level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 20).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

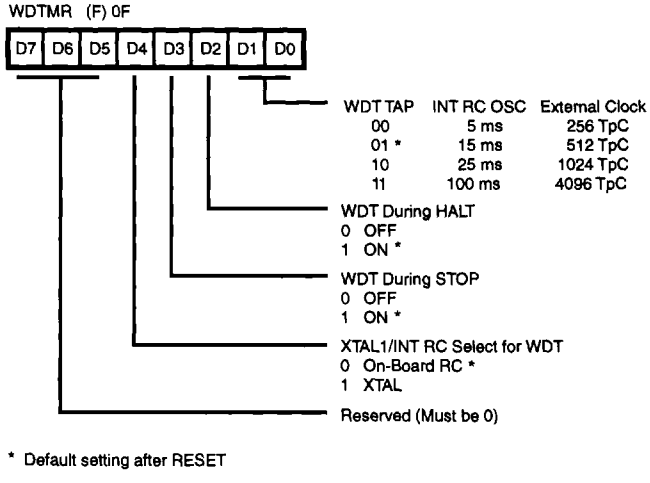


Figure 20. Watch-Dog Timer Mode Register (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

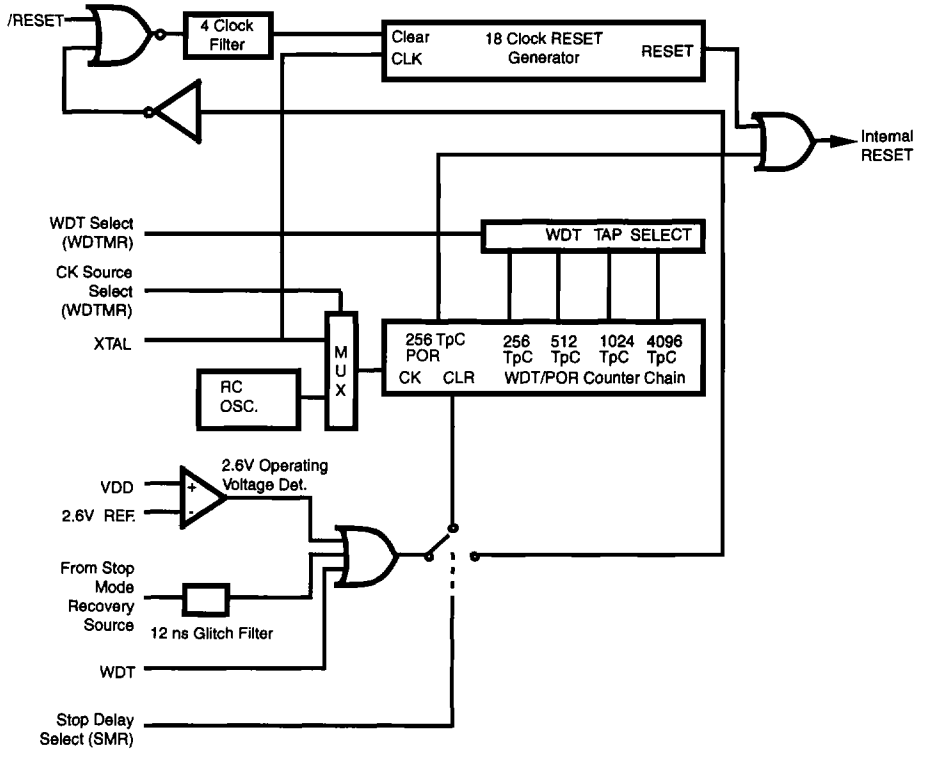


Figure 21. Resets and WDT

WDT Time Select. (D0,D1). Selects the WDT time period and is configured as shown in Table 8.

Table 8. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of XTAL Clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms.
Values given are for V_{CC} = 5.0V.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the Internal RC oscillator.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 64 internal system clock cycles from the execution of the first instruction after Power-On Reset, watch dog reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH (Figure 20).

Note: The WDT can be permanently enabled through a mask programming option. The option is selected by the customer at the time of ROM code submittal. In this mode, WDT is always activated when the device comes out of reset. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP modes is controlled by WDTMR programming. If this mask option is not selected at the time of ROM code submission, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

FUNCTIONAL DESCRIPTION (Continued)

Low Voltage Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage (Low Voltage Protection voltage). The minimum operating voltage is varying with the temperature and operating frequency, while the Low Voltage Protection voltage (V_{LV}) varies with temperature only.

The Low Voltage Protection trip voltage (V_{LV}) is less than 3V and above 1.4V under the following conditions.

Maximum (V_{LV}) Conditions:

Case 1: T_A = –40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

Case 2: T_A = –40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency is one-half the external clock frequency (SMR D1 = 0).

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies in Case 1 and Case 2, above. The device is guaranteed to function normally at supply voltages above the Low Voltage Protection trip point. The actual Low Voltage Protection trip point is a function of temperature and process parameters (Figure 22).

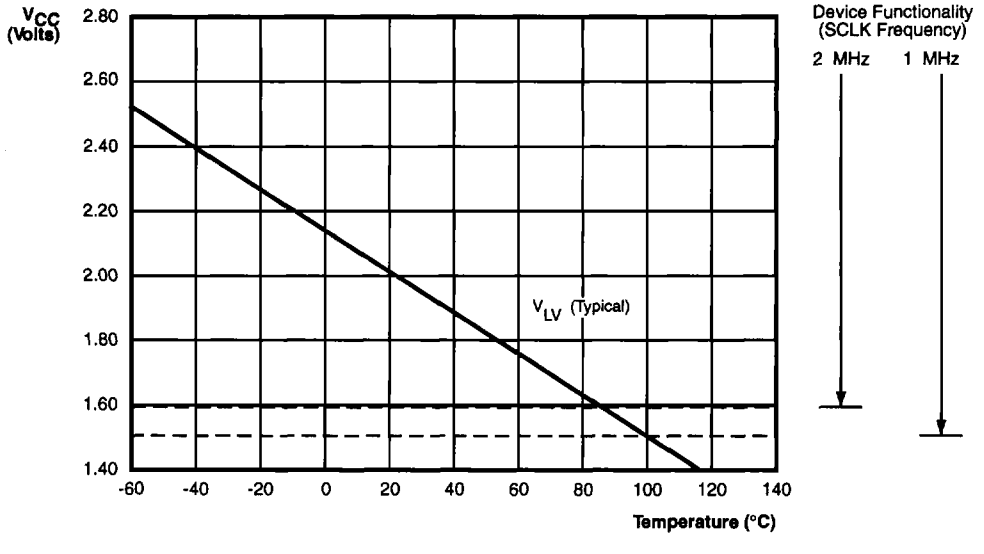


Figure 22. Typical Z86C40 Low Voltage Protection Voltage vs Temperature

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	-40	+105	C
Storage Temperature	-65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	-0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7	V
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS} [Note 2]	-0.6	V_{DD}+1	V
Total Power Dissipation		770	mW
Maximum Current out of V_{SS}		140	mA
Maximum Current into V_{DD}		125	mA
Maximum Current into an Input Pin [Note 3]	-600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	-600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		25	mA
Maximum Output Current Sourced by Any I/O Pin		25	mA

Notes:
[1] This applies to all pins except XTAL pins and where otherwise noted.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes XTAL pins.
[4] Device pin is not at an output Low state.

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 770 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH}) \,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH} \,] + \text{sum of } (V_{OL} \times I_{OL})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 23).

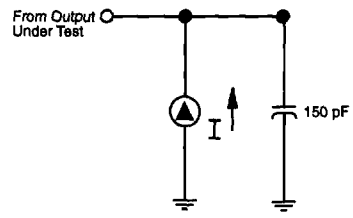


Figure 23. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	[8]
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	[8]
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	[8]
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	[8]
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	[8]
		5.5V		1.2		1.2	0.3	V	I_{OL} = +12 mA	[8]
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset	3.0V		25		25	10	mV		[10]
	Voltage	5.5V		25		25	10	mV		[10]
I_{IL}	Input Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V		-130		-130	-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	[4,5]
		5.5V		25		25	12	mA	@ 16 MHz	[4,5]
		3.0V		15		15	5	mA	@ 12 MHz	[4,5]
		5.5V		20		20	15	mA	@ 12 MHz	[4,5]
I_{CC1}	Standby Current	3.0V		4.5		4.5	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 16 MHz	[4,5]
		5.5V		8		8	3.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 16 MHz	[4,5]
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	[4,5]
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	[4,5]
I_{CC2}	Standby Current	3.0V		8		15	1	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6,11]
		5.5V		10		20	2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6,11]
		3.0V		500		600	310	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6,11,14]
		5.5V		800		1000	600	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6,11,14]

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
V^{ICR}	Input Common Mode Voltage Range	3.0	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		[10]
		5.5	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		[10]
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V		15		20	11	µA	$0V < V_{IN} < V_{CC}$	[9]
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V		-8		-10	-6	µA	$0V < V_{IN} < V_{CC}$	[9]
T_{POR}	Power On Reset	3.0V	7	24	7	25	8.5	mS		
		5.5V	3	13	3	14	5.0	mS		
V_{LV}	V_{CC} Low Voltage Protection Voltage		1.7	2.95	1.7	3.3	2.6	V	2 MHz max Int. CLK Freq.	[7]
V_{OH}	Output High Voltage (Low EMI Mode)	3.3V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -0.5mA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -0.5mA	
V_{OL}	Output Low Voltage (Low EMI Mode)	3.3V		0.6		0.6	0.2	V	I_{OL} = 1.0mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = 1.0mA	

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock-Driven	0.3 mA	5	mA	8 MHz
Resonator or Crystal	3.0 mA	5	mA	8 MHz

[2] GND = 0V.
[3] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF.
[6] Same as note [4] except inputs at V_{CC}.
[7] The V_{LV} increases as the temperature decreases.
[8] Standard Mode (not Low EMI).
[9] Auto Latch (Mask Option) selected.
[10] For analog comparator, inputs when analog comparators are enabled.
[11] Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
[12] Excludes clock pins.
[13] Typicals are at V_{CC} = 5.0V and 3.3V.
[14] Internal RC selected.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

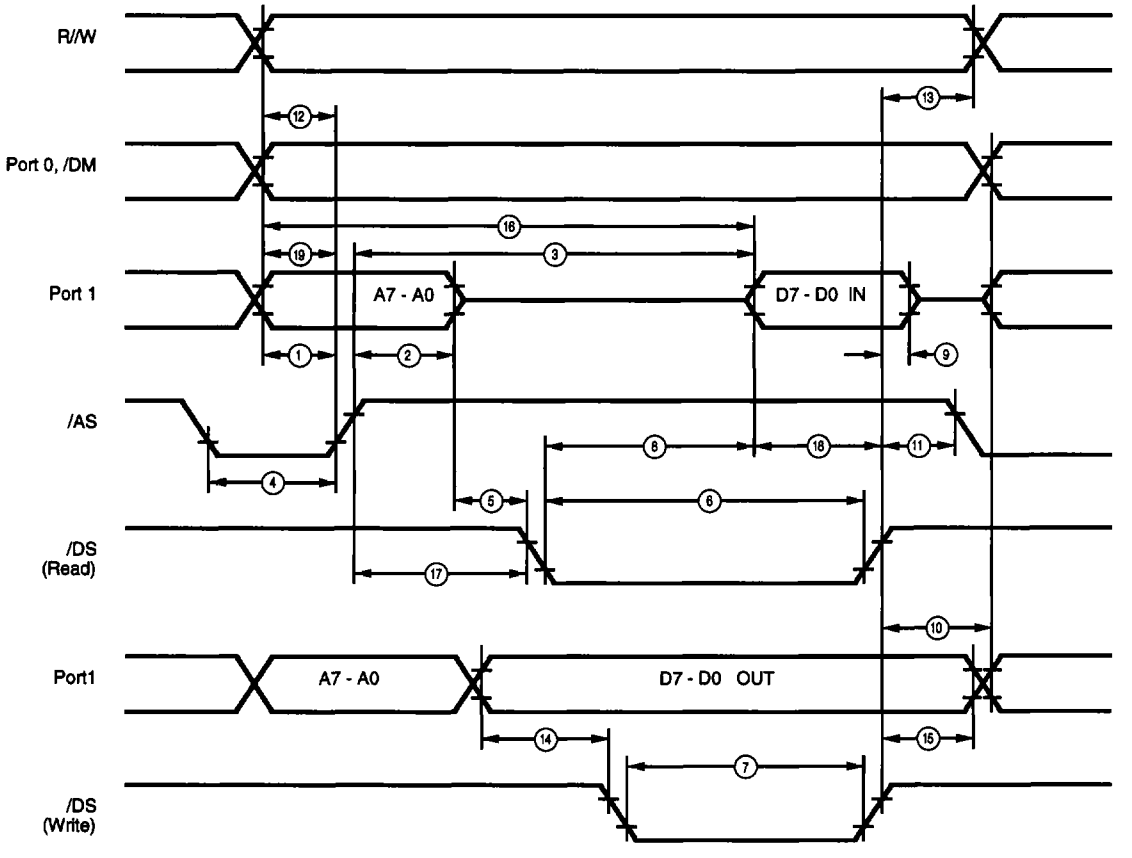


Figure 24. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table
(SCLK/TCLK = XTAL/2)

				T_A = 0°C to +70°C				T_A = -40°C to +105°C					
			Note [3]	12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	3.0	35		25		35		25		ns	[2]
			5.5	35		25		35		25			
2	TdAS(A)	/AS Rise to Address Float Delay	3.0	45		35		45		35		ns	[2]
			5.5	45		35		45		35		ns	
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.0		250		180		250		180	ns	[1,2]
			5.5		250		180		250		180	ns	
4	TwAS	/AS Low Width	3.0	55		40		55		40		ns	[2]
			5.5	55		40		55		40		ns	
5	Td	Address Float to /DS Fall	3.0	0		0		0		0		ns	
			5.5	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.0	200		135		200		135		ns	[1,2]
			5.5	200		135		200		135		ns	
7	TwDSW	/DS (Write) Low Width	3.0	110		80		110		80		ns	[1,2]
			5.5	110		80		110		80		ns	
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.0		150		75		150		75	ns	[1,2]
			5.5		150		75		150		75	ns	
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.0	0		0		0		0		ns	[2]
			5.5	0		0		0		0		ns	
10	TdDS(A)	/DS Rise to Address Active Delay	3.0	45		50		45		50		ns	[2]
			5.5	55		50		55		50		ns	
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.0	30		35		30		35		ns	[2]
			5.5	45		35		45		55		ns	
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	3.0	45		25		45		25		ns	[2]
			5.5	45		25		45		25		ns	
13	TdDS(R/W)	/DS Rise to R//W Not Valid	3.0	45		35		45		35		ns	[2]
			5.5	45		35		45		35		ns	
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.0	55		25		55		25		ns	[2]
			5.5	55		25		55		25		ns	
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.0	45		35		45		35		ns	[2]
			5.5	55		35		55		35		ns	
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230		310		230	ns	[1,2]
			5.5		310		230		310		230	ns	
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.0	65		45		65		45		ns	[2]
			5.5	65		45		65		45		ns	
18	TdDI(DS)	Data Input Setup to /DS Rise	0.0	115		60		115		60		ns	[1,2]
			5.5	75		60		75		60		ns	
19	TdDM(AS)	/DM Valid to /AS Fall Delay	3.0	35		30		35		30		ns	[2]
			5.5	35		30		35		30		ns	

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Diagram

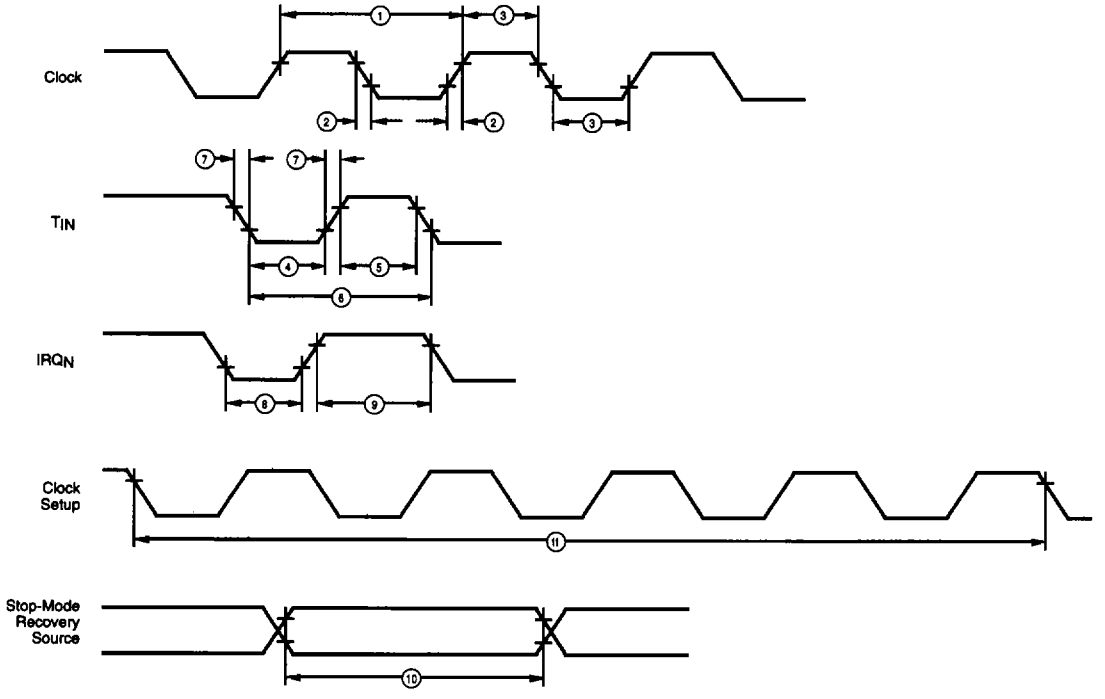


Figure 25. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2)

				T_A = 0°C to +70°C				T_A = −40°C to +105°C					
			V_{CC}	12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	Note[6]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	[1]
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	[1]
			5.5V		15		15		15		15	ns	[1]
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	[1]
			5.5V	41		31		41		31		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1]
			5.5V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin,	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	[1]
	TfTin		5.5V		100		100		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	[1,2]
			5.5V	70		70		70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,3]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,3]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,2]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,2]
10	Twsm	STOP-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		5TpC		5TpC		[4]
			5.5V		5TpC		5TpC		5TpC		5TpC		[4]
12	Twdt	Watch-Dog Timer Delay Time	3.0V	10		10		10		10		ms	D0 = 0 [5]
			5.5V	5		5		5		5		ms	D1 = 0 [5]
			3.0V	30		30		30		30		ms	D0 = 1 [5]
			5.5V	15		15		15		15		ms	D1 = 0 [5]
			3.0V	50		50		50		50		ms	D0 = 0 [5]
			5.5V	25		25		25		25		ms	D1 = 1 [5]
			3.0V	200		200		200		200		ms	D0 = 1 [5]
			5.5V	100		100		100		100		ms	D1 = 1 [5]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request via Port 3 (P31-P33).

[3] Interrupt request via Port 3 (P30).

[4] SMR-D5 = 0.

[5] Reg. WDTMR.

[6] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.

9

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = –40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	125		125		ns	[1,7,8]
			5.5V	125		125		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			[1,7,8]
			5.5V	3TpC		3TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1,7,8]
			5.5V	4TpC		4TpC			[1,7,8]
7	TrTin,	Timer Input Rise & Fall Timer	3.0V		100		100	ns	[1,7,8]
	TfTin		5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC			[1,3,7,8]
			5.5V	3TpC		3TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			[1,2,7,8]
			5.5V	3TpC		2TpC			[1,2,7,8]
10	Twsm	STOP-Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		[4,8,9]
			5.5V		5TpC		5TpC		[4,8,9]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P33-P31).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.5V ±0.5V.
[7] SMR D1 = 0.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams

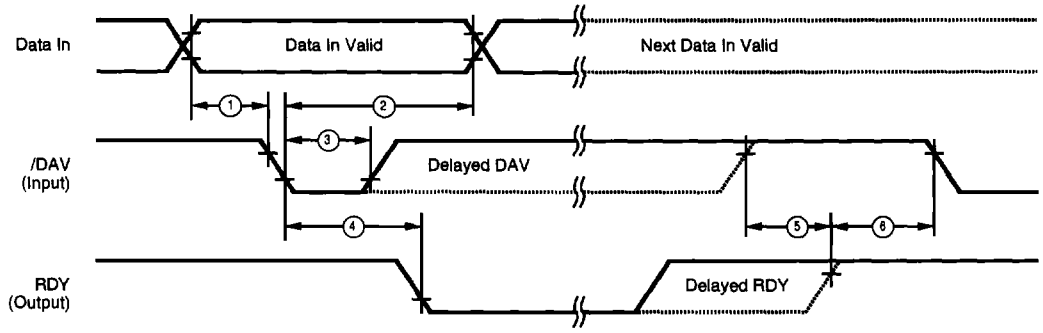


Figure 26. Input Handshake Timing

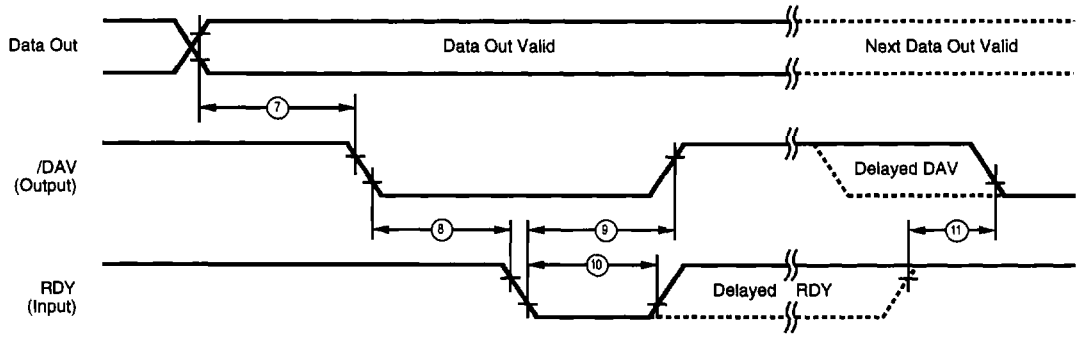


Figure 27. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note[1,2]	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A = –40°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	3.0V	160		160		160		160		IN
			5.5V	115		115		115		115		IN
3	TwDAV	Data Available Width	3.0V	155		155		155		155		IN
			5.5V	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.0V		160		160		160		160	IN
			5.5V		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	3.0V		120		120		120		120	IN
			5.5V		80		80		80		80	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	3.0V	42		31		42		31		OUT
			5.5V	42		31		42		31		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	3.0V	0		0		0		0		OUT
			5.5V	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.0V		160		160		160		160	OUT
			5.5V		115		115		115		115	OUT
10	TwRDY	RDY Width	3.0V	110		110		110		110		OUT
			5.5V	80		80		80		80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V		110		110		110		110	OUT
			5.5V		80		80		80		80	OUT

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.

EXPANDED REGISTER FILE CONTROL REGISTERS

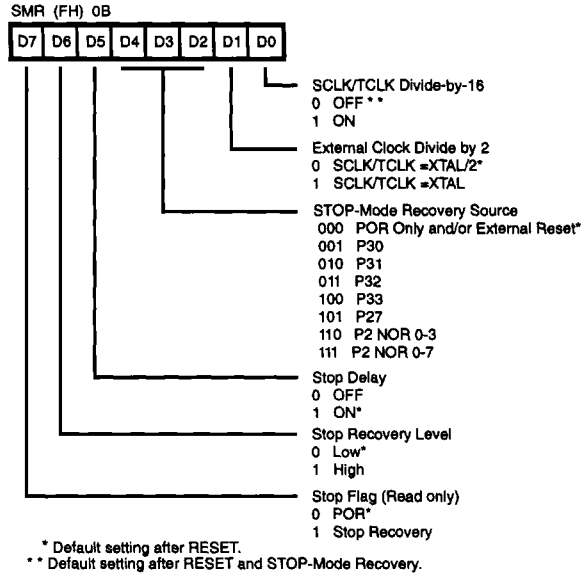


Figure 28. Stop-Mode Recovery Register (Write Only Except Bit D7, Which Is Read Only)

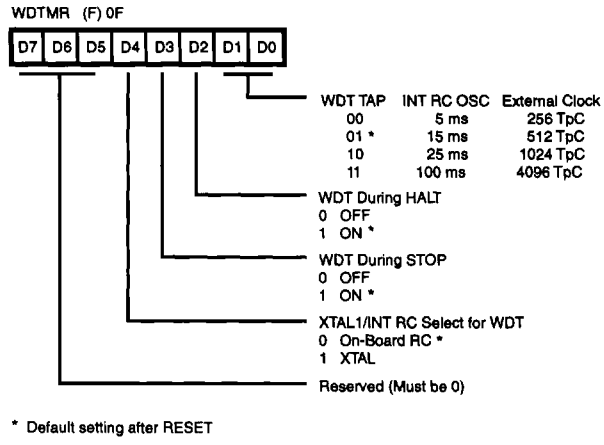


Figure 29. Watch-Dog Timer Mode Register (Write Only)

Z8® CONTROL REGISTERS

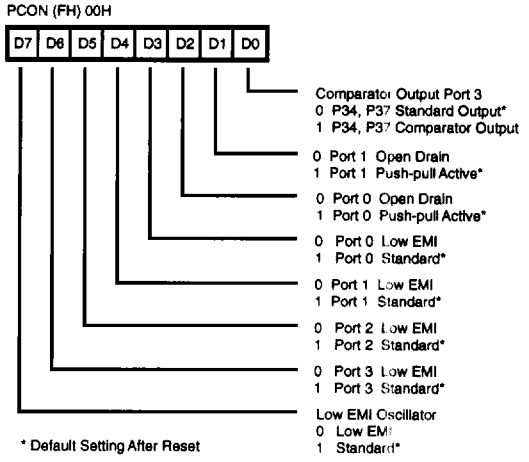


Figure 30. Port Configuration Register (PCON) (Write Only)

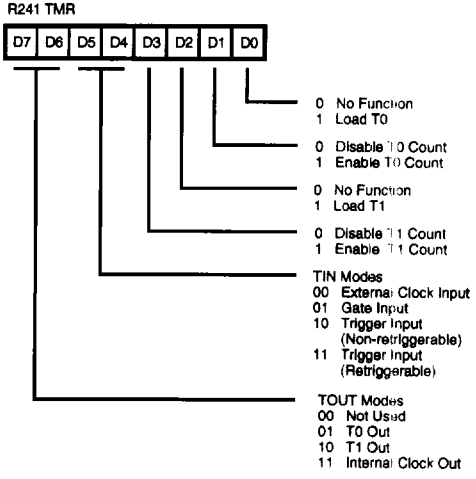


Figure 31. Timer Mode Register ($F1_H$: Read/Write)

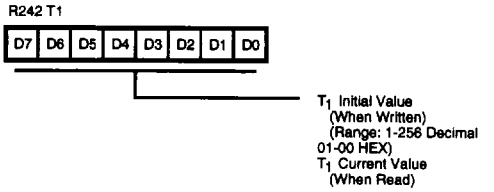


Figure 32. Counter/Timer 1 Register ($F2_H$: Read/Write)

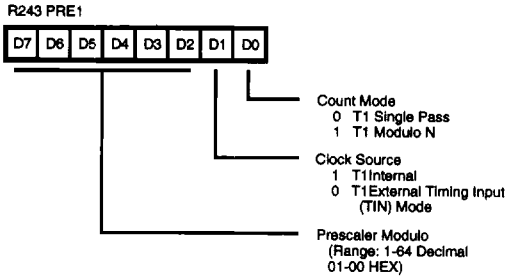


Figure 33. Prescaler 1 Register ($F3_H$: Write Only)

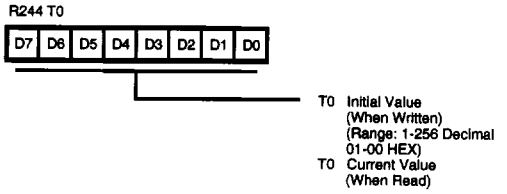


Figure 34. Counter/Timer 0 Register ($F4_H$: Read/Write)

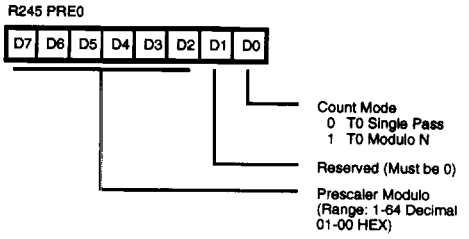


Figure 35. Prescaler 0 Register ($F5_H$: Write Only)

R246 P2M

D7	D6	D5	D4	D3	D2	D1	D0

P20 - P27 I/O Definition
0 Defines Bit as Output
1 Defines Bit as Input

Figure 36. Port 2 Mode Register ($F6_H$: Write Only)

R247 P3M

D7	D6	D5	D4	D3	D2	D1	D0

0 Port 2 Pull-Ups Open Drain
1 Port 2 Pull-Ups Active

0 P31, P32 Digital Mode
1 P31, P32 Analog Mode

0 P32 = Input
P35 = Output
1 P32 = /DAV0/RDY0
P35 = RDY0//DAV0

00 P33 = Input
P34 = Output
01 P33 = Input
10 P34 = /DM
11 P33 = /DAV0/RDY0
P34 = RDY1//DAV1

0 P31 = Input (TIN)
P36 = Output (TOUT)
1 P31 = /DAV2/RDY2
P36 = RDY2//DAV2

0 P30 = Input
P37 = Output

Reserved (Must be 0)

Figure 37. Port 3 Mode Register ($F7_H$: Write Only)

R248 P01M

D7	D6	D5	D4	D3	D2	D1	D0

P00 - P03 Mode
00 Output
01 Input
1X A11 - A8

Stack Selection
0 External
1 Internal

P10 - P17 Mode
00 Byte Output
01 Byte Input
10 AD7 - AD0
11 High-Impedance AD7 - AD0, /AS, /DS, /R/W, A11 - A8, A15 - A12, If Selected

External Memory Timing
0 Normal
1 Extended

P04 - P07 Mode
00 Output
01 Input
1X A15 - A12

Figure 38. Port 0 and 1 Mode Register ($F8_H$: Write Only)

R249 IPR

D7	D6	D5	D4	D3	D2	D1	D0

Interrupt Group Priority
000 Reserved
001 C > A > B
010 A > B > C
011 A > C > B
100 B > C > A
101 C > B > A
110 B > A > C
111 Reserved

IRQ1, IRQ4 Priority (Group C)
0 IRQ1 > IRQ4
1 IRQ4 > IRQ1

IRQ0, IRQ2 Priority (Group B)
0 IRQ2 > IRQ0
1 IRQ0 > IRQ2

IRQ3, IRQ5 Priority (Group A)
0 IRQ5 > IRQ3
1 IRQ3 > IRQ5

Reserved (Must be 0)

Figure 39. Interrupt Priority Register ($F9_H$: Write Only)

9

Z8 CONTROL REGISTERS (Continued)

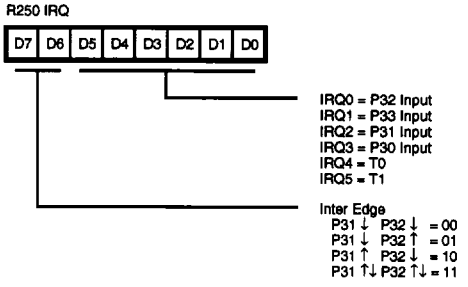


Figure 40. Interrupt Request Register (FA_H: Read/Write)

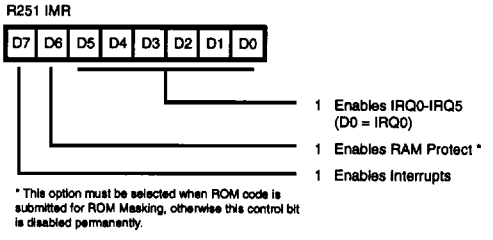


Figure 41. Interrupt Mask Register (FB_H: Read/Write)

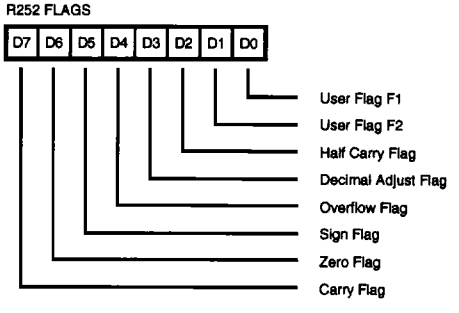


Figure 42. Flag Register (FC_H: Read/Write)

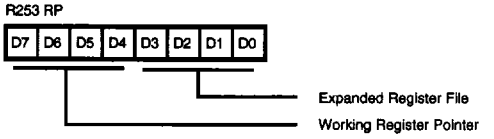


Figure 43. Register Pointer (FD_H: Read/Write)

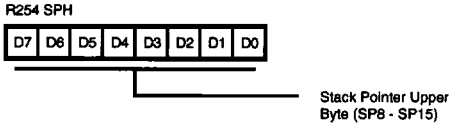


Figure 44. Stack Pointer High (FE_H: Read/Write)

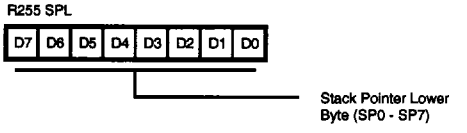


Figure 45. Stack Pointer Low (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

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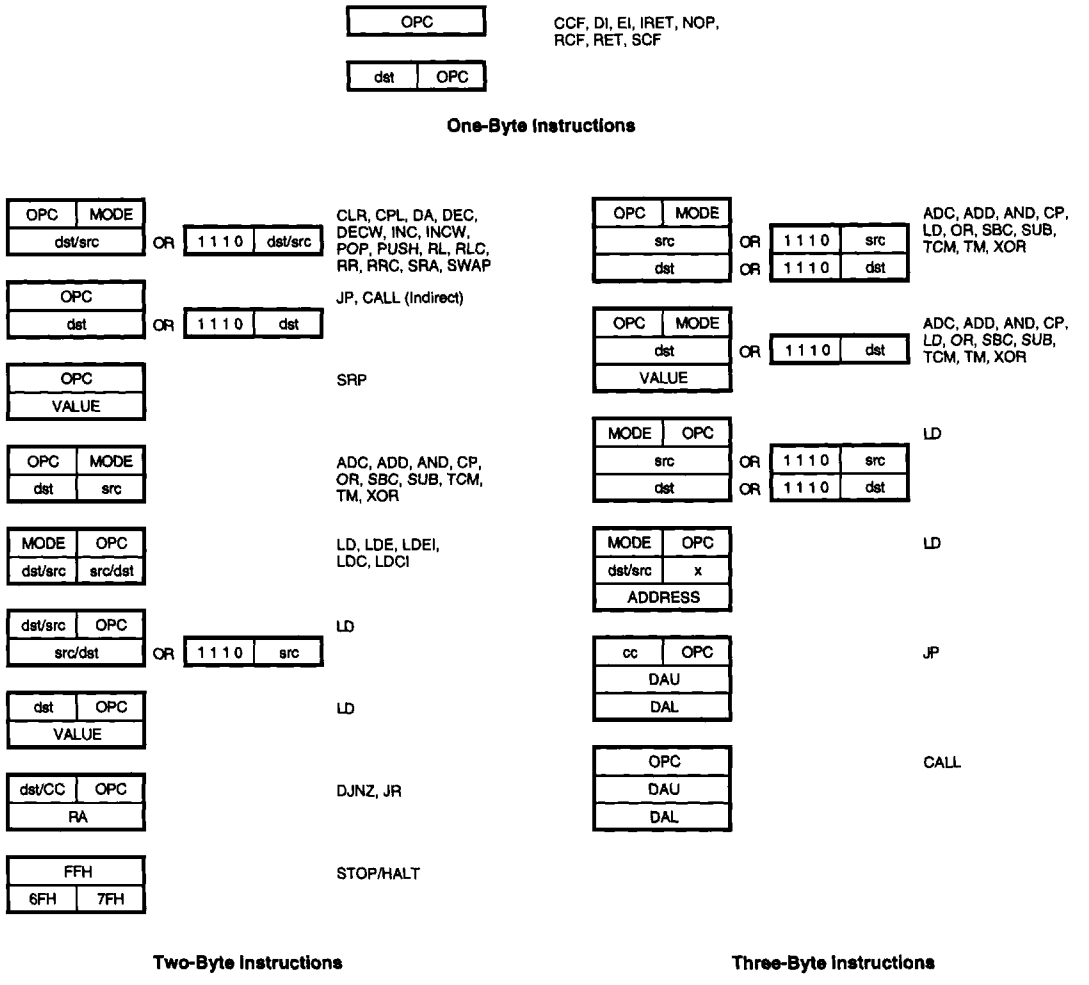
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst	R IR		90 91	*	*	*	*	-	-
RLC dst	R IR		10 11	*	*	*	*	-	-
RR dst	R IR		E0 E1	*	*	*	*	-	-
RRC dst	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst–src–C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst–src	†		2[ ]	*	*	*	*	1	*
SWAP dst	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

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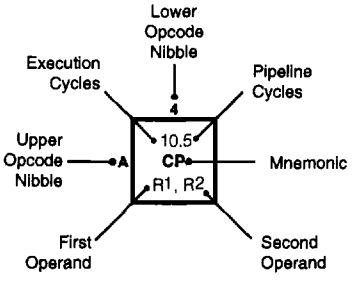
OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** Irr1, r2	18.0 **LDCI** Irr1, Ir2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2				3		1	



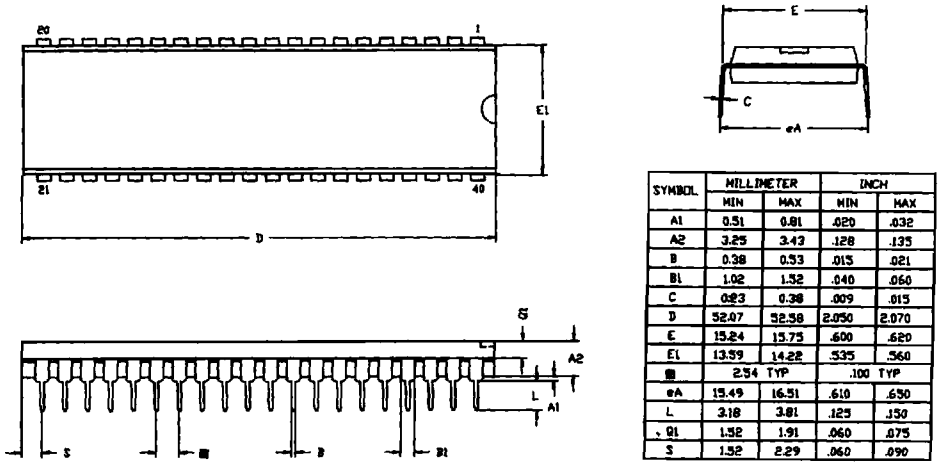
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blanks are reserved.

*2-byte instruction appears as a 3-byte instruction

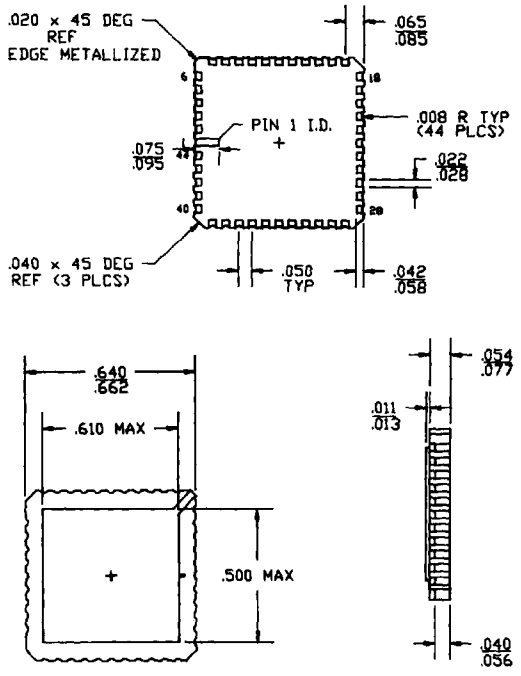
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

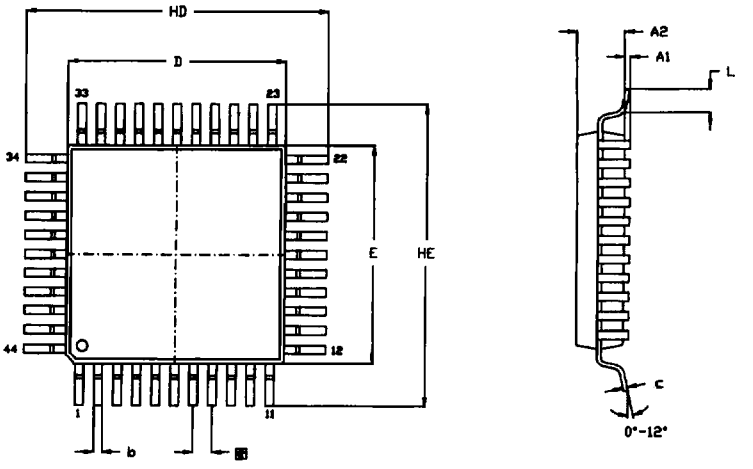
CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram



44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10mm .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86C40 (12 MHz)

Standard Temperature			Extended Temperature		
40-Pin DIP	**40-Pin PLCC**	**44-Pin QFP**	**40-Pin DIP**	**40-Pin PLCC**	**44-Pin QFP**
Z86C4012PSC	Z86C4012VSC	Z86C4012FSC	Z86C4012PEC	Z86C4012VEC	Z86C4012FEC

Z86C40 (16 MHz)

Standard Temperature			Extended Temperature		
40-Pin DIP	**40-Pin PLCC**	**44-Pin QFP**	**40-Pin DIP**	**40-Pin PLCC**	**44-Pin QFP**
Z86C4016PSC	Z86C4016VSC	Z86C4016FSC	Z86C4016PEC	Z86C4016VEC	Z86C4016FEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

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CODES

Preferred Package
P = Plastic DIP
V = Plastic Chip Carrier

Longer Lead Time
F = Plastic Quad Flat Pack

Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
16 = 16 MHz

Environmental
C = Plastic Standard

Example:
Z 86C40 16 P S C is a Z86C40, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow