HORIZONTAL SYNCHRONIZATION AND VERTICAL 625 DIVIDER SYSTEM

The TDA2571A is designed in combination with the TDA2581 as a matched pair for switched-mode driven horizontal deflection stages. When supplied with a composite video signal the TDA2571A delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 625.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such a way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Horizontal phase detector switching to a small time constant during catching. The phase detector is gated when the oscillator is synchronized.
- Horizontal oscillator (31,25 kHz).
- Burst-key pulse generator. This pulse can also be applied as black level clamp pulse.
- Vertical sync pulse separator.
- Automatic vertical synchronization (625 divider system), without delay after channel change.

QUICK REFERENCE DATA

Supply voltage				
horizontal	V_{12-11}	typ.	12	V
vertical	V_{16-11}	typ.	12	V
Sync input voltage (peak-to-peak value)	$V_{2-11(p-p)}$		0,07 to 1	V
Slicing level		typ.	50	%
Control sensitivity of horizontal PLL		typ.	2000	Hz/μs
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{8-11(p-p)}$	typ.	11	V
Vertical sync output pulse (peak-to-peak value)	$V_{1-11(p-p)}$	typ.	11	V
Burst-key output pulse(peak-to-peak value)	$V_{13-11(p-p)}$	typ.	11	V

PACKAGE OUTLINES

TDA2571A: 16 lead DIL; plastic (SOT-38).
TDA2571AQ: 16-lead QIL; plastic (SOT-58).

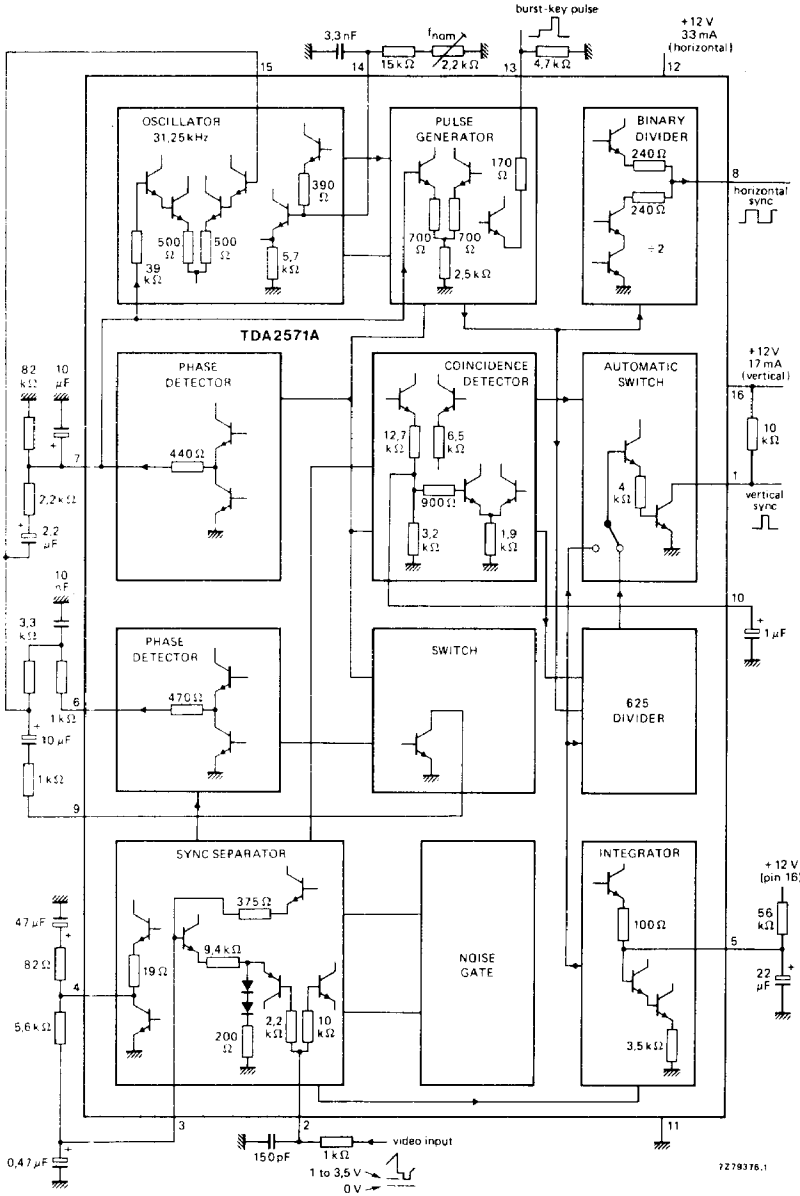


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Sypply voltage			
horizontal	V_{12-11}	max. 13,2	V
vertical	V_{16-11}	max. 13,2	V
Total power dissipation	P_{tot}	max. 1	W
Storage temperature	T_{stg}	−25 to + 130	°C
Operating ambient temperature	T_{amb}	−25 to + 65	°C

CHARACTERISTICS

At V_{12-11} = 12 V; V_{16-11} = 12 V; T_{amb} = 25 °C; measured in Fig. 1

Supply voltage range (pins 12 and 16)	V_{12-11}; V_{16-11}	typ. 12 10 to 13,2	V V
Current consumption	$I_{12} + I_{16}$	typ. 50 < 75	mA mA
Sync separator and noise gate			
Sync pulse amplitude (negative going) peak-to-peak value	$V_{2-11(p-p)}$	0,07 to 1	V*
Top-sync level	V_{2-11}	1,0 to 3,5	V
Slicing level		typ. 50	%**
Slicing level noise gating	V_{2-11}	typ. 0,7	V
Phase locked loop			
Holding range	Δf	typ. ± 1000	Hz
Catching range	Δf	typ. ± 900	Hz
Control sensitivity of horizontal PLL		typ. 2000	Hz/μs
Control sensitivity of phase detector		typ. 1,2	V/μs
Delay between sync input and detector output (pin 6)	t_d	typ. 0,4	μs
Phase modulation due to hum on the supply line		typ. 2,0	μs/V▲

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

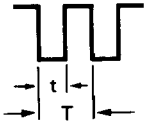
** The slicing level is defined as the ratio of the amplitude of the slicing level to black level to the amplitude of the sync pulse.

▲ The voltage is a peak-to-peak value; the figure given can be reduced to 0,6 μs/V(p-p) by means of an extra capacitor of 330 nF between pins 12 and 7.

CHARACTERISTICS (continued)

Horizontal oscillator				
Frequency; free running	f_o	typ.	31,250	kHz
Frequency at output pin 8	f_8	typ.	15,625	kHz
Spread of frequency without spread of external components	Δf_o	<	4	%
Temperature coefficient	T	typ.	$2,5 \times 10^{-4}$	K^{-1}
Change of frequency when V_{12-11} drops to 6 V	Δf_o	<	10	%
Change of frequency when V_{12-11} increases from 10 to 13,2 V	Δf_o	<	0,5	%
Output voltage; no load (peak-to-peak value)	$V_{8-11(p-p)}$	>	10	V
Output resistance	R_{8-11}	typ.	300	Ω
Output current range (peak-to-peak value)	$I_{8(p-p)}$		0 to 40	mA
Duty factor of output pulse	δ	typ.	46	%*
Delay between falling edge of output pulse and end of sync pulse at pin 2	t_d	typ.	0,9	μs**
Burst-key pulse				
Output voltage (peak-to-peak value)	$V_{13-11(p-p)}$	>	10	V
Duration of upper part of output pulse	t_p	typ.	3,6	μs**
Duration of lower part of output pulse	t_p	typ.	9,1	μs**
Amplitude of lower part of output pulse	$V_{13-11(p-p)}$	typ.	3	V**
Output resistance	R_{13-11}	typ.	200	Ω
Delay between the end of the sync pulse at pin 2 and the rising edge of the burst key pulse	t_d	typ.	0,9	μs**
Coincidence detector				
Voltage level of time constant switch	V_{10-11}	typ.	2,0	V
Voltage when the oscillator is in sync	V_{10-11}	typ.	0,4	V
Voltage when the oscillator is out-of-sync	V_{10-11}	typ.	2,5	V
Voltage during noise	V_{10-11}	typ.	1,0	V

* The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

** See waveforms Fig. 2.

Vertical sync pulse

Output voltage (peak-to-peak value)	$V_{1\text{-}11(p\text{-}p)}$	>	10 V
Duration of output pulse during indirect synchronization	t_p	typ.	170 µs
Duration of output pulse during direct synchronization (coincidence detector high)	t_p	typ.	160 µs
Load resistor to pin 2	R_L	>	2 kΩ
Output voltage low with R_L = 2 kΩ	$V_{1\text{-}11}$	<	500 mV
Ratio between basic horizontal oscillator frequency and vertical pulse			625 *

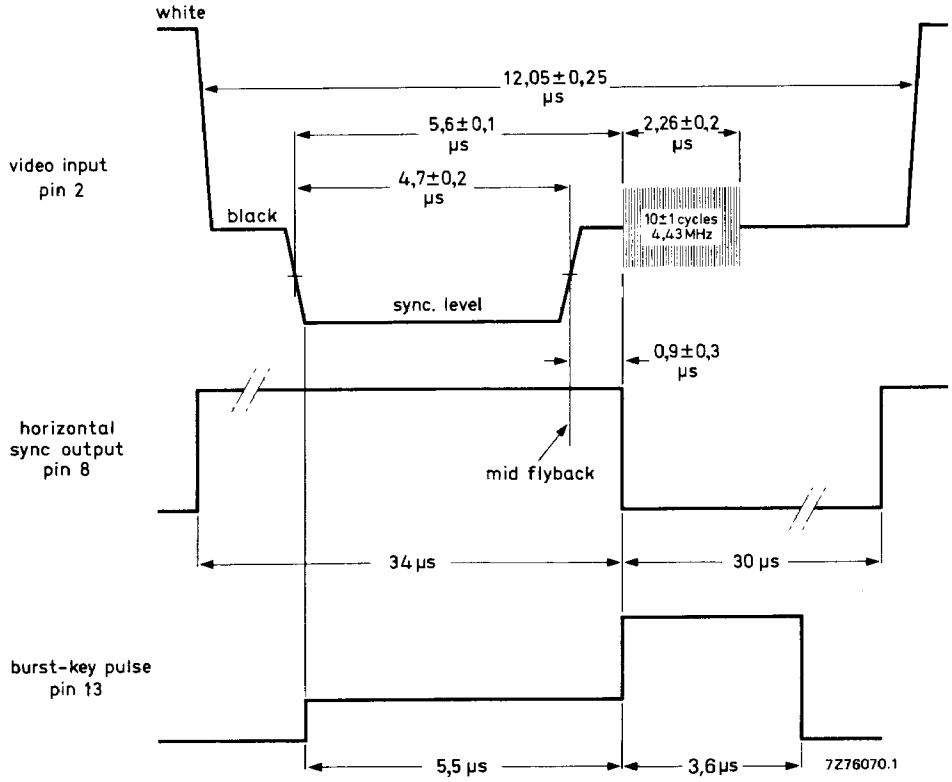


Fig. 2 Relationship between the video input signal to the TDA2571A and the horizontal sync and burst-key pulse output.

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 1; the pulse of the divider circuit is switched off.

PINNING

1. Vertical sync pulse output
2. Video input
3. Sync separator slicing level output
4. Black level detector output
5. Vertical integrator bias network
6. Horizontal phase detector output
7. Reference voltage horizontal frequency control stage
8. Horizontal sync pulse output
9. Time constant switch
10. Coincidence detector output
11. Negative supply (ground)
12. Positive supply (horizontal)
13. Burst-key pulse output
14. RC-network horizontal oscillator
15. Control horizontal oscillator
16. Positive supply (vertical)

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Vertical sync pulse output

   A resistor of about 10 kΩ must be connected between pin 1 and the positive supply line (pin 16; vertical supply).

   The output pulse will come from the 625 divider stage (standard signal) or from the vertical sync pulse separator (non-standard signal), depending on the input signal on pin 2. The standard and non-standard signals are detected automatically.

2. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,07 to 1 V. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 70 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level $< 0,7$ V, thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (e.g. TDA2540; TDA2541) the noise gate of the TDA2571A is not required.

3. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The capacitor connected to pin 3 must be about 0,47 μF.

4. Black level detector output

   The black level of the input signal is detected on this pin, which is required to obtain good sync separator operation. A capacitor of 47 μF in series with a resistor of 82 Ω has to be connected to this pin. A 5,6 kΩ resistor must be connected between pins 3 and 4.

5. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 56 kΩ; C = 22 μF.

6. Horizontal phase detector output

   The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

   This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal oscillator (so a good suppression of interference is obtained which may be present on the supply line). This pin is also used to control the reference waveform for the phase detector to the middle of the gating, giving a good noise immunity of the synchronization.

8. Horizontal sync pulse output

   This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 46%. The falling edge of this pulse has a delay of 0,9 μs with respect to the end of the sync pulse. Because of this phase relationship this pulse can directly drive the TDA2581.

9. Time constant switch

   This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 10). During in-sync or when only noise is received pin 9 assumes ground level, which results in a long time constant and good noise immunity.

   During out-of-sync or VCR playback, pin 9 has a high impedance and consequently only the short time constant is available. In this condition a large catching range is obtained.

10. Coincidence detector output

    A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
    The following output voltages can occur:
    - when in-sync: 0,4 V
    - when out-of-sync: 2,0 V
    - during noise at input: 1,0 V

    When the output voltage $< 1{,}85$ V, the flywheel filter is switched to a long time constant, and the gating of the phase detector is switched-on.

    For a voltage $> 1{,}85$ V, the flywheel filter has a short time constant, and the gating of the phase detector is switched-off. The result is that during noise the flywheel time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer).

    The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

    The time constant value can be switched manually by a resistor (10 kΩ) to + 12 V.

11. Negative supply (ground)

12. Positive supply horizontal oscillator

    Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have a separate decoupling of this pin with respect to pin 16. The current-draw of this pin is typically 33 mA.

13. Burst-key pulse output

    This pulse is composed of two parts. The lower part has an amplitude of 3 V peak-to-peak and a width of 9,1 μs (for phase relation see Fig. 2). The upper part has a total amplitude in excess of 10 V peak-to-peak and a width of 3,6 μs. The leading edge of this pulse has a delay of 0,9 μs with respect to the falling edge of the sync pulse at the input (pin 2).

    This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

APPLICATION INFORMATION (continued)

14. RC-network horizontal oscillator

    Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part should be as small as possible, because of poor stability of variable carbon resistors.

    The oscillator can be adjusted when pins 7 and 15 are short-circuited.

15. Horizontal oscillator control pin

16. Positive supply sync separator and divider circuit (vertical)

    For this supply only a simple decoupling is required. The current-draw of this pin is typically 17 mA.

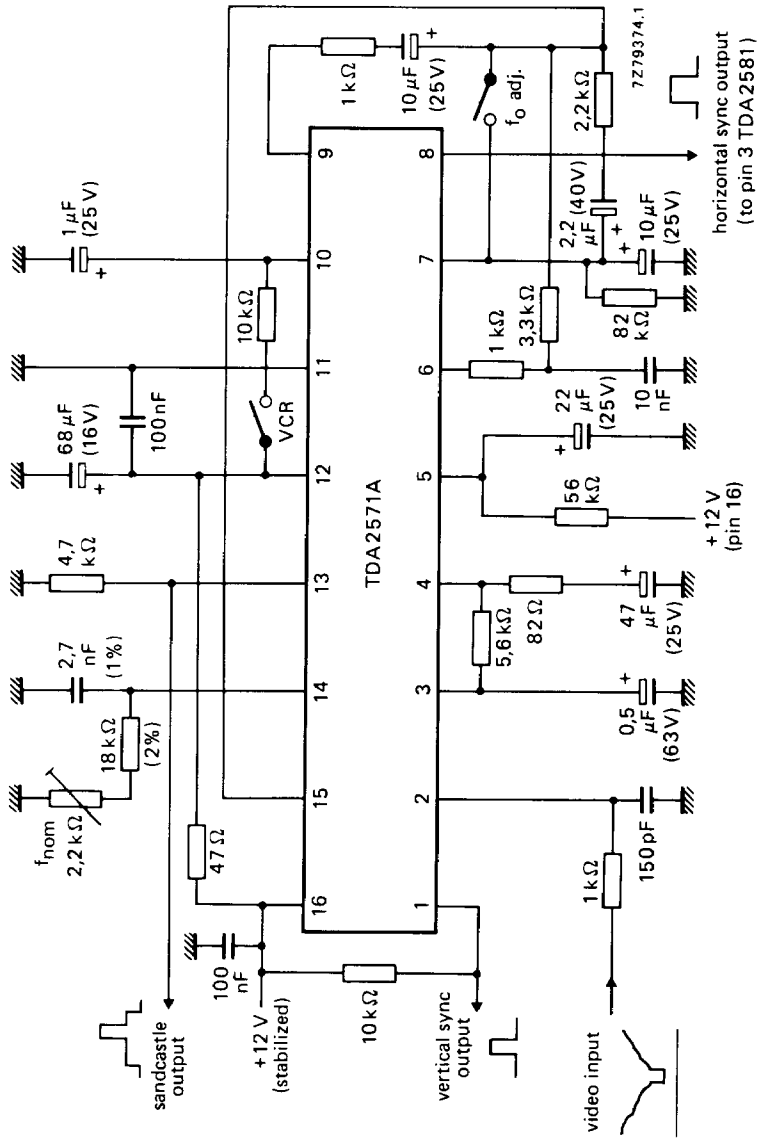


Fig. 3 Typical application circuit diagram; for combination of the TDA2571A with the TDA2581 see Fig. 4.

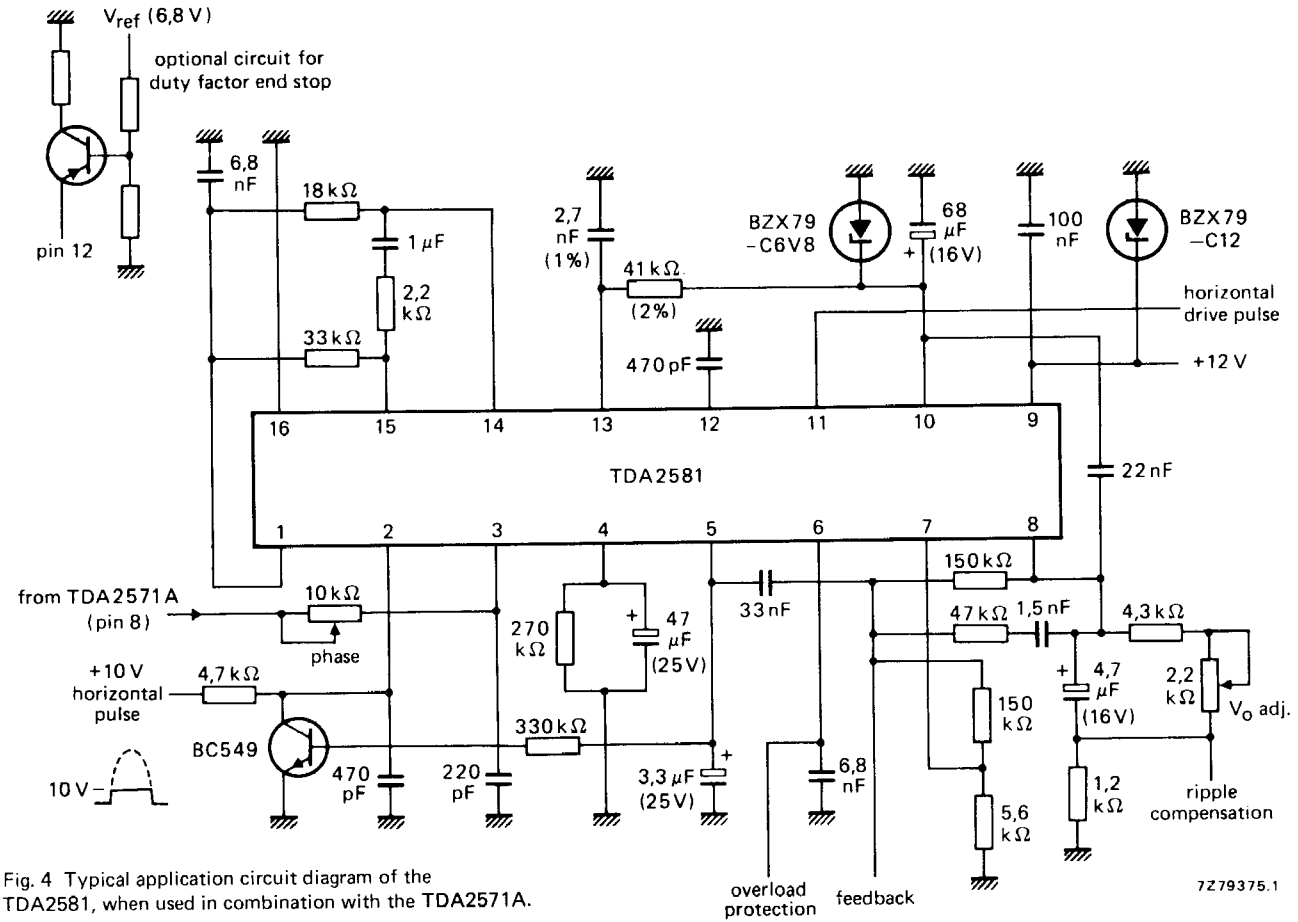


Fig. 4 Typical application circuit diagram of the TDA2581, when used in combination with the TDA2571A.