# PCMCIA FLASH MEMORY CARD — SRV30 SERIES

## SRAM Memory Card 2MB Through 16MB

## FEATURES

- High Performance SRAM memory Card
- Universal 3.3 to 5 Volt Supply allows for wider compatibility between systems.
- Fast Access times: 150ns @ 3.3V – 5V
- x8/x16 PCMCIA standard interface
- Low Power CMOS technology provides very low power and reliable data retention characteristics
  - standby current < 100µA typical
- Rechargeable Lithium battery with recharge circuitry
  - eliminates the need for replaceable batteries
  - standby current during recharge typically < 2mA
  - battery backup time
    - 18 months - type I card
    - 40 months - type II card
      typical based on 4MB
- Unlimited write cycles, no endurance issues
- Optional Features:
  - 2KB EEPROM attribute memory containing CIS
  - Optional Hardware Write Protect switch
- PC Card Standard Type I or Type II Form Factor

## GENERAL DESCRIPTION

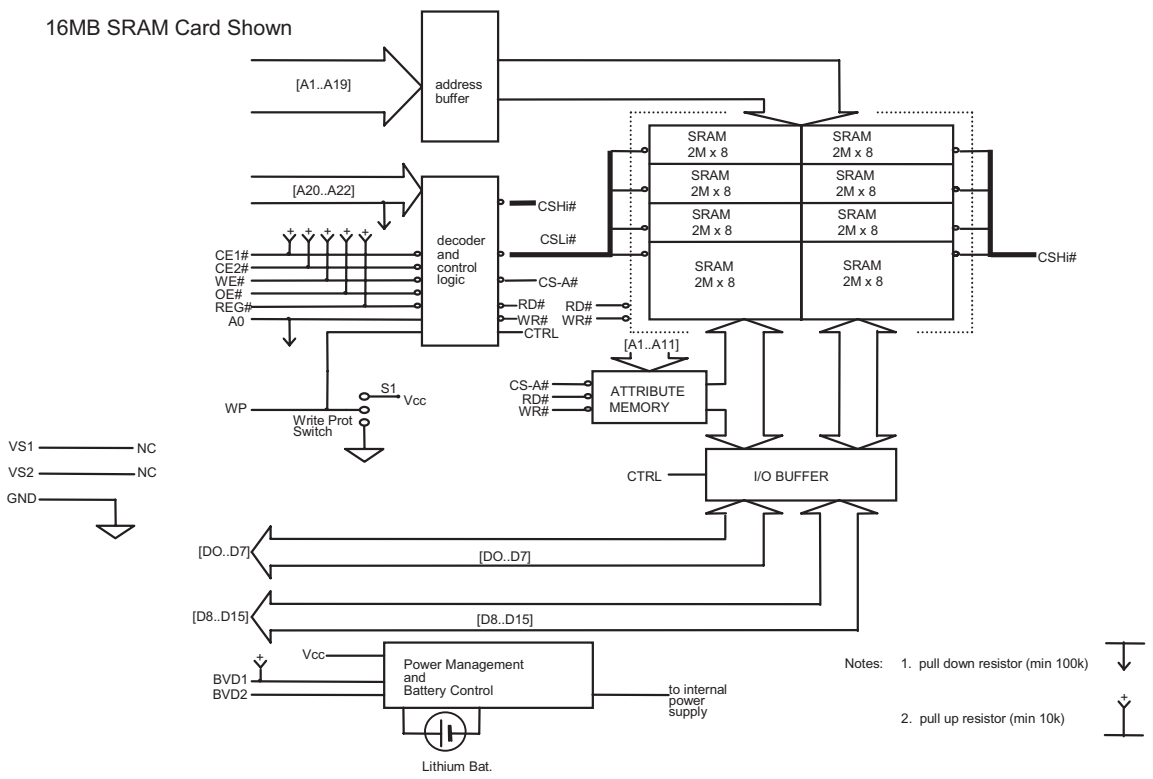
The WEDC SRAM Series (SRV30) memory cards offer a high performance nonvolatile storage solution for code and data storage, disk caching, and write intensive mobile and embedded applications.

Packaged in PCMCIA type I or type II housing (type II for cards with extended battery backup time), the WEDC SRAM SRV30 series is based on high density and super low power SRAM memory devices, providing densities from 2MBytes to 16MBytes.

The SRV30 series of SRAM memory cards has a universal wide power supply (3V to 5V) and operates at speeds as high as 150ns. The cards are based on advanced CMOS technology providing very low power and reliable data retention characteristics. WEDC's SRAM cards contain a rechargeable lithium battery and recharge circuitry, eliminating the need for replaceable batteries found in many SRAM cards.

WEDC's standard cards are shipped with WEDC's SRAM Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

## BLOCK DIAGRAM



## PINOUT

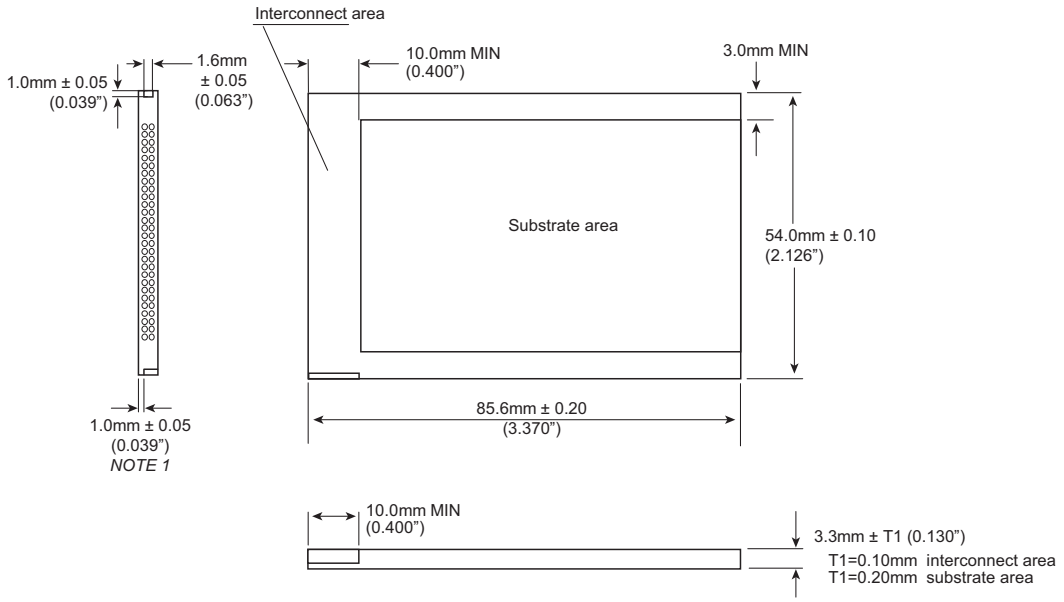
| Pin | Signal name | I/O | Function | Active |
|---|---|---|---|---|
| 1 | GND | | Ground | |
| 2 | DQ3 | I/O | Data bit 3 | |
| 3 | DQ4 | I/O | Data bit 4 | |
| 4 | DQ5 | I/O | Data bit 5 | |
| 5 | DQ6 | I/O | Data bit 6 | |
| 6 | DQ7 | I/O | Data bit 7 | |
| 7 | CE1# | I | Card enable 1 | LOW |
| 8 | A10 | I | Address bit 10 | |
| 9 | OE# | I | Output enable | LOW |
| 10 | A11 | I | Address bit 11 | |
| 11 | A9 | I | Address bit 9 | |
| 12 | A8 | I | Address bit 8 | |
| 13 | A13 | I | Address bit 13 | |
| 14 | A14 | I | Address bit 14 | |
| 15 | WE# | I | Write Enable | LOW |
| 16 | RDY/BSY# | O | Ready/Busy | N.C. |
| 17 | Vcc | | Supply Voltage | |
| 18 | Vppl | | Prog. Voltage | N.C. |
| 19 | A16 | I | Address bit 16 | |
| 20 | A15 | I | Address bit 15 | |
| 21 | A12 | I | Address bit 12 | |
| 22 | A7 | I | Address bit 7 | |
| 23 | A6 | I | Address bit 6 | |
| 24 | A5 | I | Address bit 5 | |
| 25 | A4 | I | Address bit 4 | |
| 26 | A3 | I | Address bit 3 | |
| 27 | A2 | I | Address bit 2 | |
| 28 | A1 | I | Address bit 1 | |
| 29 | A0 | I | Address bit 0 | |
| 30 | DQ0 | I/O | Data bit 0 | |
| 31 | DQ1 | I/O | Data bit 1 | |
| 32 | DQ2 | I/O | Data bit 2 | |
| 33 | WP | O | Write Potect | HIGH |
| 34 | GND | | Ground | |

| Pin | Signal name | I/O | Function | Active |
|---|---|---|---|---|
| 35 | GND | | Ground | |
| 36 | CD1# | O | Card Detect 1 | LOW |
| 37 | DQ11 | I/O | Data bit 11 | |
| 38 | DQ12 | I/O | Data bit 12 | |
| 39 | DQ13 | I/O | Data bit 13 | |
| 40 | DQ14 | I/O | Data bit 14 | |
| 41 | DQ15 | I | Data bit 15 | |
| 42 | CE2# | I | Card Enable 2 | LOW |
| 43 | VS1 | O | Voltage Sense 1 | N.C. |
| 44 | N.C. | | | |
| 45 | N.C. | | | |
| 46 | A17 | I | Address bit 17 | |
| 47 | A18 | I | Address bit 18 | |
| 48 | A19 | I | Address bit 19 | |
| 49 | A20 | I | Address bit 20 | 2MB(2) |
| 50 | A21 | I | Address bit 21 | 4MB(2) |
| 51 | Vcc | | Supply Voltage | |
| 52 | Vpp2 | | Prog. Voltage | N.C. |
| 53 | A22 | | Address bit 22 | 8MB(2,4) |
| 54 | A23 | | Address bit 23 | 16MB(2,3) |
| 55 | A24 | | Address bit 24 | N.C. |
| 56 | A25 | | Address bit 25 | N.C. |
| 57 | VS2 | O | Voltage Sense 2 | N.C. |
| 58 | N.C. | | | |
| 59 | Wait# | O | Extended Bus Cycle | Low |
| 60 | N.C. | | | |
| 61 | REG# | I | Attrib Mem Select | Low |
| 62 | BVD2 | O | Bat. Volt. Detect 2 | (5) |
| 63 | BVD1 | O | Bat. Volt. Detect 1 | (5) |
| 64 | DQ8 | I/O | Data bit 8 | |
| 65 | DQ9 | I/O | Data bit 9 | |
| 66 | DQ10 | O | Data bit 10 | |
| 67 | CD2# | O | Card Detect 2 | LOW |
| 68 | GND | | Ground | |

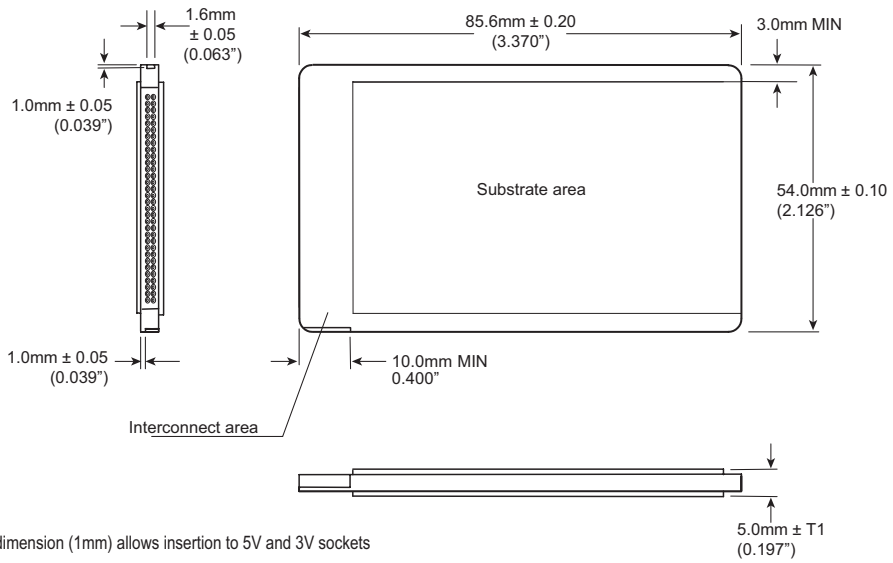
Notes:
1. CD1# and CD2# are grounded internal to PC Card.
2. Shows density for which specified address bit is MSB. Higher order address bits are no connects (ie 1MB A19 is MSB, A20 - A21 are NC).
3. The A23 Address line for 16MB capacities is also used for 12MB cards.
4. VS1 is grounded and VS2 is open to indicate a 3.3V/5V card, with a 5V key, has been inserted.
5. BVD1 and BVD2 are open drain outputs with a 10KOhm internal pull-up resistors

## PACKAGE DIMENSIONS

### Type I




### Type II




Note 1: this dimension (1mm) allows insertion to 5V and 3V sockets

## CARD SIGNAL DESCRIPTION

| Symbol | Type | Name and Function |
|---|---|---|
| A0 - A25 | INPUT | **ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit. (address pins used are based on card density,see pinout for highest used address pin) |
| DQ0 - DQ15 | INPUT/OUTPUT | **DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ0 - DQ7 constitute the lower (even) byte and DQ8 - DQ15 the upper (odd) byte. DQ15 is the MSB. |
| CE1#, CE2# | INPUT | **CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7. |
| OE# | INPUT | **OUTPUT ENABLE:** Active low signal enabling read data from the memory card. |
| WE# | INPUT | **WRITE ENABLE:** Active low signal gating write data to the memory card. |
| RDY/BSY# | OUTPUT | **READY/BUSY OUTPUT:** Not used for SRAM cards |
| CD1#, CD2# | OUTPUT | **CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins. |
| WP | OUTPUT | **WRITE PROTECT:** Follows hardware Write Protect Switch. When Switch is placed in on position, signal is pulled high (10K ohm). When switch is off signal is pulled low. |
| VPP1, VPP2 | N.C. | **PROGRAM/ERASE POWER SUPPLY:** Not used for SRAM cards. |
| $V_{CC}$ | | **CARD POWER SUPPLY:** 5.0V for all internal circuitry. |
| GND | | **GROUND:** for all internal circuitry. |
| REG# | INPUT | **ATTRIBUTE MEMORY SELECT:** only used with cards built with optional attribute memory. |
| RST | INPUT | **RESET:** Not used for SRAM cards |
| WAIT# | OUTPUT | **WAIT:** This signal is pulled high internally for compatibility. No wait states are generated. |
| BVD1, BVD2 | OUTPUT | **BATTERY VOLTAGE DETECT:** Provides status of Battery voltage.<br>BVD2 = BVD1 = $V_{OH}$ (battery voltage is guaranteed to retain data)<br>BVD2 = $V_{OL}$, BVD1 = Voh (data is valid, battery recharge required)<br>BVD2 = BVD1 = $V_{OL}$ (data may no longer be valid, battery requires extended recharge) |
| VS1, VS2 | OUTPUT | **VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V, 16 bit card has been inserted. |
| RFU | | **RESERVED FOR FUTURE USE** |
| N.C. | | **NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating |

## FUNCTIONAL TRUTH TABLE

| **READ function** | | | | | | **Common Memory** | | | **Attribute Memory** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Function Mode | CE2# | CE1# | A0 | OE# | WE# | REG# | D15-D8 | D7-D0 | REG# | D15-D8 | D7-D0 |
| Standby Mode | H | H | X | X | X | X | High-Z | High-Z | X | High-Z | High-Z |
| Byte Access (8 bits) | H | L | L | L | H | H | High-Z | Even-Byte | L | High-Z | Even-Byte |
| | H | L | H | L | H | H | High-Z | Odd-Byte | L | High-Z | Not Valid |
| Word Access (16 bits) | L | L | X | L | H | H | Odd-Byte | Even-Byte | L | Not Valid | Even-Byte |
| Odd-Byte Only Access | L | H | X | L | H | H | Odd-Byte | High-Z | L | Not Valid | High-Z |
| **WRITE function** | | | | | | | | | | | |
| Standby Mode | H | H | X | X | X | X | X | X | X | X | X |
| Byte Access (8 bits) | H | L | L | H | L | H | X | Even-Byte | L | X | Even-Byte |
| | H | L | H | H | L | H | X | Odd-Byte | L | X | X |
| Word Access (16 bits) | L | L | X | H | L | H | Odd-Byte | Even-Byte | L | X | Even-Byte |
| Odd-Byte Only Access | L | H | X | H | L | H | Odd-Byte | X | L | X | X |

## ABSOLUTE MAXIMUM RATINGS[2]

| Operating Temperature $T_A$ (ambient) | |
|---|---|
| Commercial | 0°C to +60 °C |
| Industrial | -40°C to +85 °C |
| **Storage Temperature** | |
| Commercial | 0°C to +60 °C |
| Industrial | -40°C to +85 °C |
| Voltage on any pin relative to $V_{SS}$ | -0.5V to $V_{CC}$+0.5V (1) |
| $V_{CC}$ supply Voltage relative to $V_{SS}$ | -0.5V to +7.0V |

Notes: Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC CHARACTERISTICS[1]

CMOS Test Conditions: $V_{IL}$ = $V_{SS}$ ± 0.2V, $V_{IH}$ = 5V ± 0.2V, $V_{CC}$ = 3.3V or 5V

| Sym | Parameter | Density | Notes | Min | Typ(3) | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | $V_{CC}$ Active Current | All | 1 | | | 25 | mA | $V_{CC}$ = 5.25V<br>tcycle = 150ns |
| $I_{CCS}$ | $V_{CC}$ Standby Current | All | 2,4! | | < 1 | 10 | mA | $V_{CC}$ = 5.25V<br>Control Signals = $V_{CC}$ |
| $I_{LI}$ | Input Leakage Current | All | 5,6 | | | ±20 | µA | $V_{CC}$ = $V_{CC}$ MAX<br>$V_{IN}$ =$V_{CC}$ or $V_{SS}$ |
| $I_{LO}$ | Output Leakage Current | All | 6 | | | ±20 | µA | $V_{CC}$ = $V_{CC}$ MAX<br>$V_{OUT}$ =$V_{CC}$ or $V_{SS}$ |
| $V_{IL}$ | Input Low Voltage | All | 6 | | | 0.9<br>1.6 | V | $V_{CC}$ = 3V<br>$V_{CC}$ = 5.25V |
| $V_{IH}$ | Input High Voltage | All | 6 | 2.1<br>3.85 | | $V_{CC}$ +0.5<br>$V_{CC}$ +0.5 | V | $V_{CC}$ = 3V<br>$V_{CC}$ = 5.25V |
| $V_{OL}$ | Output Low Voltage | All | 6 | | | 0.4 | V | $I_{OL}$ = 3.2mA |
| $V_{OH}$ | Output High Voltage | All | 6 | 2.4 | 2.8 | | V | $I_{OH}$ = -2.0mA |

Notes:
1. All currents are for x16 mode and are RMS values unless otherwise specified.
2. Control Signals: CE1#, CE2#, OE#, WE#, REG#.
3. Typical: $V_{CC}$ = 5V, T = +25C.
4. ICCS includes battery recharge current. Value depends on battery discharge level. $I_{CCS}$ min is specified for fully charged battery. $I_{CCS}$ typical value is specified for battery discharge to 2.7V. $I_{CCS}$ max is specified for a fully discharged battery (0V). Battery will recharge to 1.5V in 20 sec.
5. Values are the same for byte and word wide modes for all card densities.
6. Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when $V_{IN}$ = GND due to internal pull-up resistors

## BATTERY CHARACTERISTICS

| | | | SRV31-34 | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Density** | **Notes** | **Type I** | **Type II** | **Units** | **Conditions** |
| Battery Life | All | (1) | min 10 | | years | Normal operation, T=25C |
| Battery Backup Time | 2MB | (2) | 18 | 40 | months (typical) | Battery backup time is a calculated value and is not guaranteed. This should not be used to schedule battery recharging. (Temp 25°C) |
| | 4MB | | 18 | 40 | | |
| | 8MB | | 12 | 30 | | |
| | 12MB | | 10 | 25 | | |
| | 16MB | | 9 | 20 | | |

Notes:
1. Battery Life refers to functional lifetime of battery.
2. Battery backup time is density and temperature dependent.

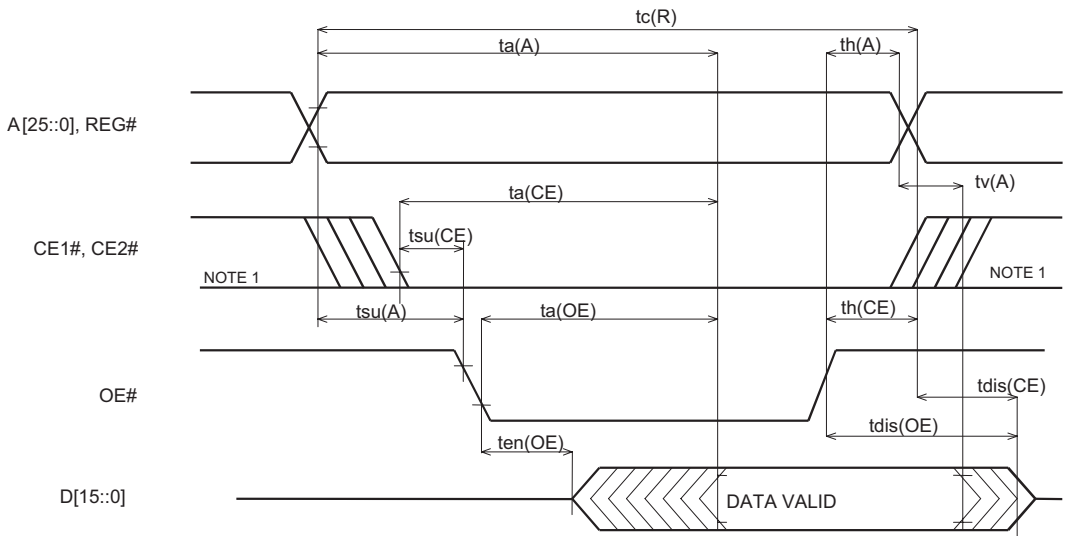
## AC CHARACTERISTICS

### Read Timing Parameters

| SYM (PCMCIA) | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 150 | | ns |
| $t_a$(A) | Address Access Time | | 150 | ns |
| $t_a$(CE) | Card Enable Access Time | | 150 | ns |
| $t_a$(OE) | Output Enable Access Time | | 75 | ns |
| $t_{su}$(A) | Address Setup Time | 20 | | ns |
| $t_{su}$(CE) | Card Enable Setup Time | 0 | | ns |
| $t_h$(A) | Address Hold Time | 20 | | ns |
| $t_h$(CE) | Card Enable Hold Time | 20 | | ns |
| $t_v$(A) | Output Hold from Address Change | 0 | | ns |
| $t_{dis}$(CE) | Output Disable Time from CE# | | 75 | ns |
| $t_{dis}$(OE) | Output Disable Time from OE# | | 75 | ns |
| $t_{dis}$(CE) | Output Enable Time from CE# | 5 | | ns |
| $t_{dis}$(CE) | Output Enable Time from OE# | 5 | | ns |

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

### Read Timing Diagram



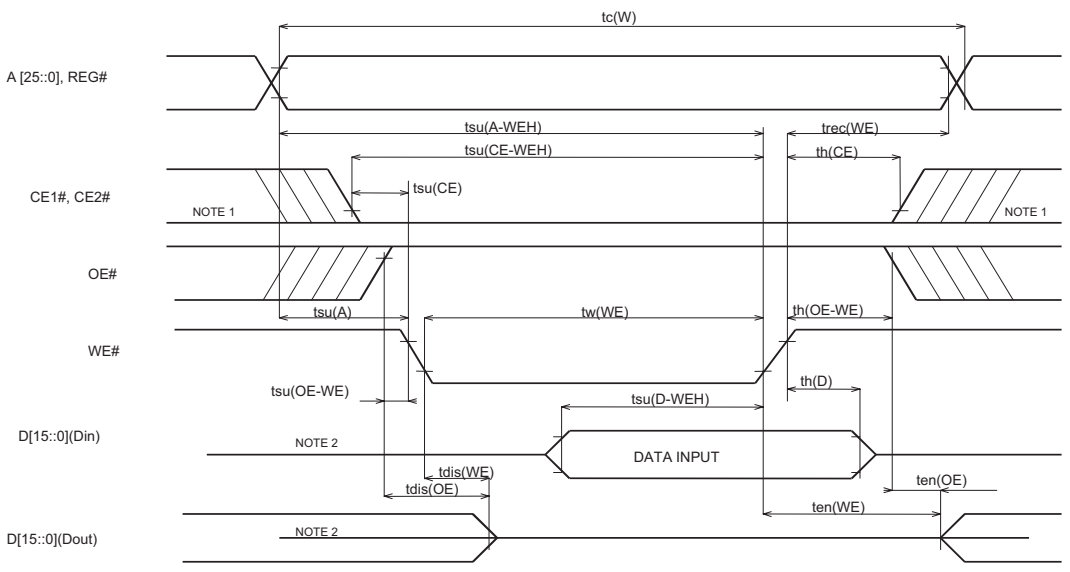

Note: Signal may be high or low in this area.

## AC CHARACTERISTICS
## Write Timing Parameters

| SYM (PCMCIA) | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| tCW | Write Cycle Time | 150 | | ns |
| tw(WE) | Write Pulse Width | 80 | | ns |
| tsu(A) | Address Setup Time | 20 | | ns |
| tsu(A-WEH) | Address Setup Time for WE# | 100 | | ns |
| tsu(CE-WEH) | Card Enable Setup Time for WE# | 100 | | ns |
| tsu(D-WEH) | Data Setup Time for WE# | 50 | | ns |
| th(D) | Data Hold Time | 20 | | ns |
| trec(WE) | Write Recover Time | 20 | | ns |
| tdis(WE) | Output Disable Time from WE# | | 75 | ns |
| tdis(OE) | Output Disable Time from OE# | | 75 | ns |
| ten(WE) | Output Enable Time from WE# | 5 | | ns |
| tdis(OE) | Output Enable Time from OE# | 5 | | ns |
| tsu(OE-WE) | Output Enable Setup from WE# | 10 | | ns |
| th(OE-WE) | Output Enable Hold from WE# | 10 | | ns |
| tsu(CE) | Card Enable Setup Time from OE# | 0 | | ns |
| th(CE) | Card Enable Hold Time | 20 | | ns |

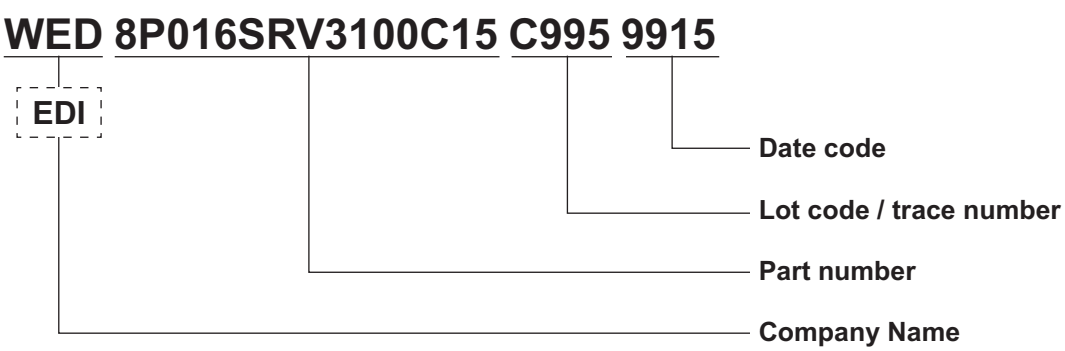
Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

## Write Timing Diagram




Note:
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 -D0) by the host system.

## PRODUCT MARKING




Note:
Some products are currently marked with our pre-merger company name/ acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2001 all PCMCIA products will be marked only with the WED prefix.

## PRODUCT NUMBERING

**8 P 016 SRV31 00 C 15**

**Card access time**
15 150ns
25 250ns

**Temperature range**
C Commercial 0°C to +70°C
I Industrial -40°C to +85°C

**Packaging option**
00 Standard, type 1

**Card family and version**
– See Card Family and Version Info. for details (next page)

**Card capacity**
016 16MB

**PC card**
P Standard PCMCIA
R Ruggedized PCMCIA

**Card technology**
7 FLASH
8 SRAM

## ORDERING INFORMATION

# 8P XXX SRV YY SS T ZZ

where

| | | | | |
|---|---|---|---|---|
| **XXX:** | 002 | 2MB | | |
| | 004 | 4MB | | |
| | 006 | 6MB | | |
| | 008 | 8MB | | |
| | 012 | 12MB | | |
| | 016 | 16MB | | |
| **YY:** | 31 | no attribute memory, no Write Protect Switch | | |
| | 32 | with attribute memory, no Write Protect Switch | | |
| | 33 | with Write Protect Switch, no attribute memory | | |
| | 34 | with attribute memory, with Write Protect Switch | | |
| **SS:** | 00 | WEDC SRAM Logo | Type I | |
| | 01 | Blank Housing, | Type I | |
| | 02 | Blank Housing, | Type I Recessed | |
| | 03 | WEDC SRAM Logo, | Type II | (extended battery backup time) |
| | 04 | Blank Housing, | Type II | (extended battery backup time) |
| | 05 | Blank Housing, | Type II Recessed | (extended battery backup time) |
| **T:** | C | Commercial | | |
| | I | Industrial | | |
| **ZZ:** | 15 | 150ns | | |

## Document Title

PCMCIA FLASH Memory Card — SRV30 Series

SRAM Memory Card 2MB through 16MB

## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev 0 | Initial release | 1-23-02 | |