FIFO

4K x 9 FIFO

VARIABLE FLAGS

FEATURES

- High speed: 25ns access, 35ns cycle time
- Asynchronousand simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Empty/Full Flags (128 increments)

OPTIONS — MARKING

- Timing

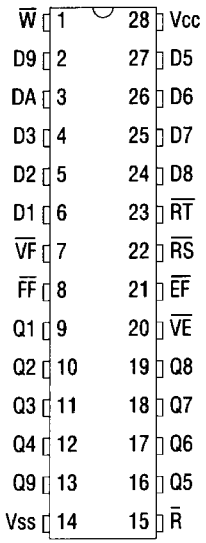
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

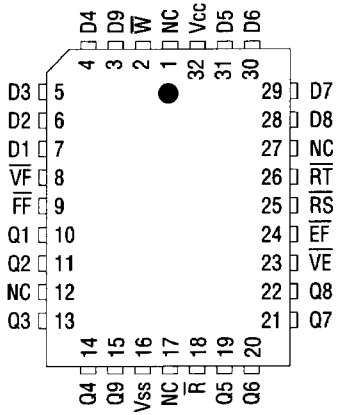
Plastic DIP	None
Ceramic DIP	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.