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MITEL
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SA868/9

Pulse Width Modulation Waveform Generator

Preliminary Information

DS3755 - 3.0 January 1996

The SA868/9 Domestic Appliance Motor Controller IC has been designed specifically for pulse width modulation (PWM) control of motors used in household goods such as washing machines, food processors and drills. The IC allows selection of sixteen separate factory programmed rotational speeds with smooth, preselectable acceleration and deceleration in between and externally programmable direction.

Selection of a particular frequency is via 4 digital inputs allowing easy interface to mechanical process timers, push buttons or microcontroller port pins. The preselectable speeds are programmed into the ROM area on the IC during manufacture and are specified by the customer.

The IC controls both voltage and frequency via its PWM algorithm ensuring that the flux in the machine is constant in the constant torque region of operation. Differing machine characteristics are catered for by allowing the customer to dictate the exact profile of the voltage/frequency curve.

Acceleration and deceleration are controlled automatically by the IC, taking full account of the instantaneous direction of rotation. In addition, the carrier frequency, power frequency range, waveform type, minimum pulse length and pulse underlap times may be preset at manufacture to allow for the whole spectrum of power devices.

Comprehensive protection circuitry is provided to ensure reliable operation.

All parameters are derived from a single ceramic resonator oscillator source. All six PWM outputs are capable of directly driving an optocoupler or pulse transformer without further buffering. The TRIP output is capable of driving an external LED.

Special versions of the SA868/9 are available which are customised for waveform generation applications such as Switched Mode Power Supplies, Uninterruptible Power Supplies etc. These include 50Hz, 60Hz and 400Hz output frequencies. The acceleration and deceleration function is defeated as is the voltage/frequency profile.

ORDERING INFORMATION

SA868/CG/DP1 24-Lead DIL (3 Phase)

SA868/CG/MP1 24-Lead SOIC (3 Phase)

SA869/CG/DP1 20-Lead DIL (1 Phase)

SA869/CG/MP1 20-Lead SOIC (1 Phase)

All Plastic Packages, commercial temp.range

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	7V
Voltage on any pin	V_{SS} - 0.3V to V_{DD} + 0.3V
Storage Temperature	-65°C to +125°C
Operating Temperature	0°C to +70°C

(Temperature ratings above based upon plastic encapsulation).

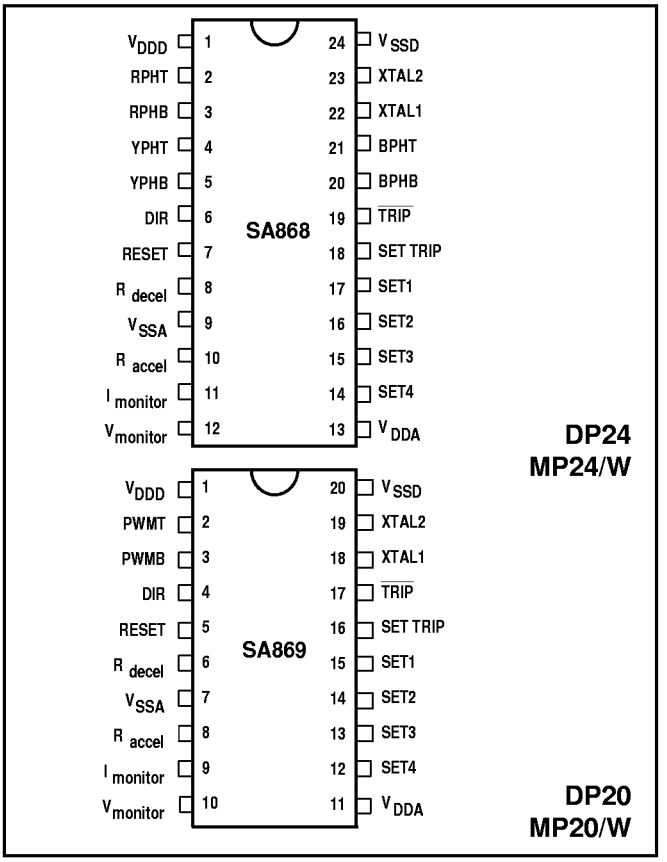


Fig. 1: Pin connections - top view

FEATURES

- Mixed Signal Technology Allows Single Chip Solution
- Specifically Designed for Control of Domestic Appliances and Waveform Generation
- Built-in High Current Drivers Suitable for Direct Drive of Opto-isolators
- Selectable Carrier Frequency up to 24kHz to allow Silent Operation
- Wide Power Frequency Range 0 - 4000Hz
- All User Defined Parameters Held in Factory Programmed ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Times
- Selectable Acceleration and Deceleration Times via External Resistors
- Three Selectable Power Waveforms held in Internal ROM, including Deadbanding Technique for Reduced Losses

PIN FUNCTIONS

3PH	1PH	NAME	TYPE	FUNCTION
1	1	V_{DDD}	POWER	Positive supply voltage (digital)
24	20	V_{SSD}	POWER	Negative (0V) supply (digital)
13	11	V_{DDA}	POWER	Positive supply voltage (analog)
9	7	V_{SSA}	POWER	Negative (0V) supply (analog)
17	15	SET1	I/P	Speed reference bits. SET4=MSB. 4-bit nibble sets new aiming frequency (user selected) from Speed Selection Table
16	14	SET2	I/P	
15	13	SET3	I/P	
14	12	SET4	I/P	
6	4	DIR	I/P	Direction bit. Selects reverse direction when high and Speed SelectionTable permits. Tie to V_{SSD} on SA869
12	10	$V_{MONITOR}$	I/P	Inhibits acceleration and deceleration whilst >Vdd/2 (Dominant over Imonitor input)
11	9	$I_{MONITOR}$	I/P	Forces system to decelerate whilst >Vdd/2 If still >Vdd/2 when zero speed reached, all PWM outputs are temporarily disabled Normal acceleration recommences when <Vdd/2
18	16	SET TRIP	I/P	Debounced input disables all PWM outputs when taken high. Internal pull-down resistors included
2	2	RPHT	O/P	Red Phase Top - true signal. (PWMT on SA869)
3	3	RPHB	O/P	Red Phase Bottom.- true signal. (PWMB on SA869)
4	-	YPHT	O/P	Yellow Phase Top - true signal
5	-	YPHB	O/P	Yellow Phase Bottom - true signal.
21	-	BPHT	O/P	Blue Phase Top - true signal
20	-	BPHB	O/P	Blue Phase Bottom - true signal
19	17	$\overline{TRIP}$	O/P	Active low output indicates state of trip latch. Capable of directly driving an LED
22	18	XTAL1	I/P	Clock input/crystal connection
23	19	XTAL2	O/P	Clock output/crystal connection
7	5	$\overline{RESET}$	I/P	Clears internal states and counters. Also resets Trip condition
10	8	Raccel	I/P	Connection to external resistor and capacitor. Sets acceleration rate
8	6	Rdecel	I/P	Connection to external resistor and capacitor. Sets deceleration rate

DC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated) V_{DDD} V_{DDA} = 5V ±5% T_{amb} = 25°C

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Input High Voltage.	V_{IH}	2	-	-	V	
Input Low Voltage	V_{IL}	-	-	0.8	V	
Input Leakage Current	I_{IN}	-	-	10	uA	$V_{IN}=V_{DDD}$ or V_{SSD}
Output High Voltage	V_{OH}	4.0	>4.5	-	V	I_{OH}= -12mA
Output Low Voltage	V_{OL}	-	<0.2	0.4	V	I_{OL}= +12mA
Static Supply Current	I_{DDSt}	-	-	1	mA	O/Ps open cct.
Dynamic Supply Current	$I_{DD}dy$	-	<5	25	mA	XTAL=25MHz
Supply Voltage	V_{DDD}/V_{DDA}	4.5	5.0	5.5	V	
Vmonitor/Imonitor threshold	V_{THR}	-	$V_{DDA}/2$	-	V	Rising
	V_{THE}	-	$V_{DDA}/2.08$	-	V	Falling

AC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated) V_{DDD} V_{DDA} = 5V ±5% T_{amb} = 25°C

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Clock Frequency	f_{CLK}	-	-	25	MHz	
External Clock Duty Cycle	D_{CLK}	40	-	60	%	
SET TRIP = 1 to Outputs tripped and TRIP = 0	t_{TRIP}	-	$3/f_{clk}$	$4/f_{clk}$	s	
Minimum Reset Period at power on	t_{RST}	-	2CRaccel	-	s	
Raccel, Rdecel Freq Range	R_{AD}	1	-	200	kHz	
Accel/Decel Defeat threshold	V_{DFT}	-	$0.1V_{DDA}$	-	V	
SET 1 : SET 4, DIR Debounce Period	t_{DBNCE}	-	$768/f_{carr}$	$1024/f_{carr}$	s	

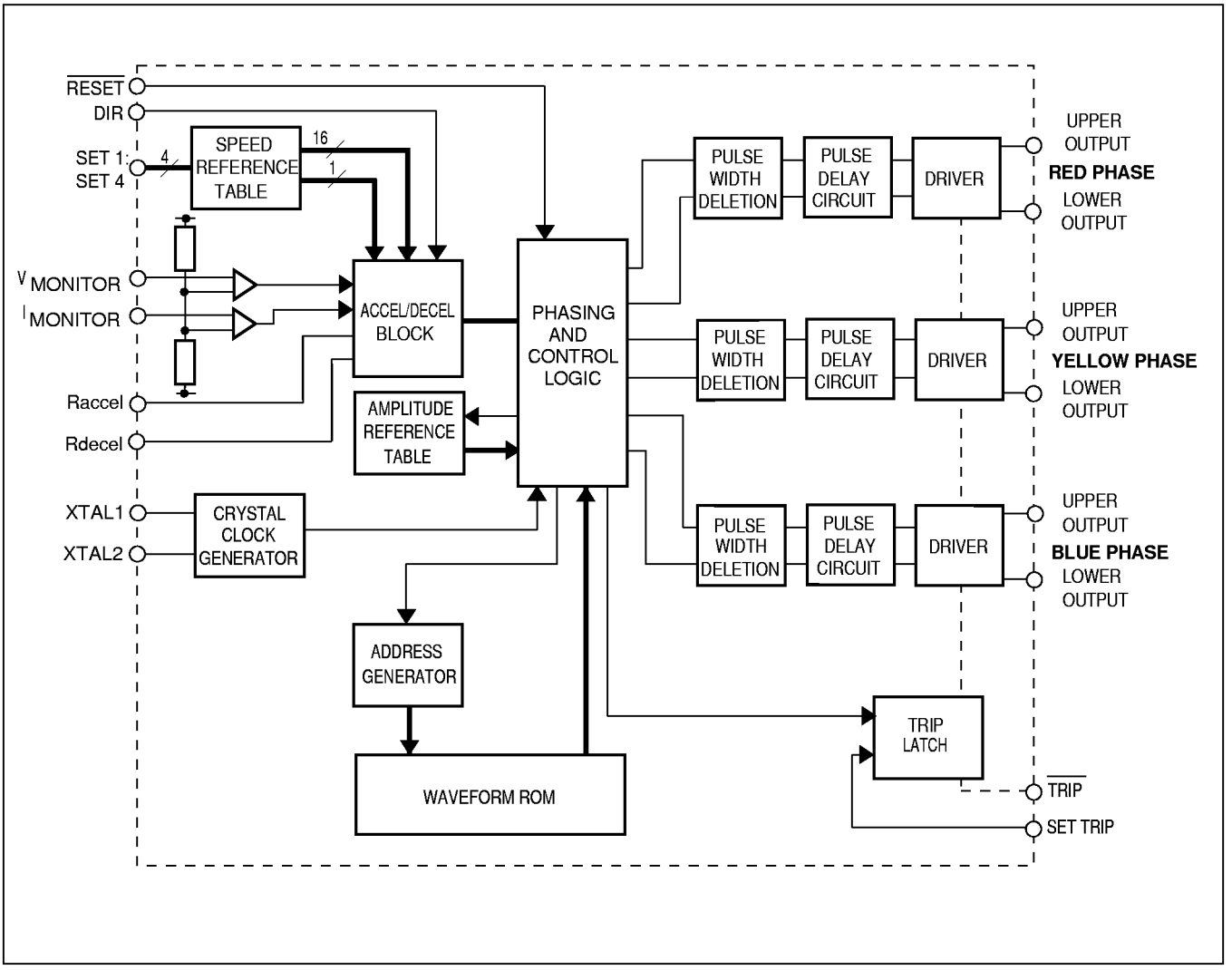


Fig. 2: Block diagram

SPEED SELECTION BLOCK

The Speed Selection Table consists of a 16*18 ROM containing user-specific data. Each 18-bit field dictates a particular setpoint speed to the rest of the IC. The least significant 16 bits dictate the scalar value of the frequency of the PWM output. The remaining 2 bits, in conjunction with the DIR pin are dedicated to the direction of rotation, as follows:-

BIT16 External Sign	BIT17 (MSB) Internal Sign	DIR PIN	ACTUAL DIRECTION (SETPOINT)
0	0	X	0 (REVERSE)
0	1	X	1 (FORWARD)
1	X	0	0 (REVERSE)
1	X	1	1 (FORWARD)

Table 1: External/internal direction decoder

This allows the external state of DIR to be "locked-out" for any entry in the look-up table and the direction forced internally. Note that these are direction demands and do not indicate an instantaneous change to a particular direction. The actual change of direction will only occur after the appropriate deceleration period.

The frequency represented by the 16-bit word is calculated as follows:-

$$^{f}power = \frac{^{f}range * p}{65536}$$

where: p = decimal value of 16 least significant bits in speed look-up table.
$^{f}range$ = power frequency range (see later).

Location 0 in the look-up table always dictates "deceleration to rest and turn off PWM outputs". This location is never available for customer specific values.

Zero speed is always represented as +0 (i.e. sign bit high) to ensure correct acceleration/deceleration. A speed of -0 is illegal and is not programmed into the look-up table.

Note that SET1 : SET4 and DIR inputs are debounced since they may be fed by mechanical switches. Please refer to AC Electrical Characteristics for details.

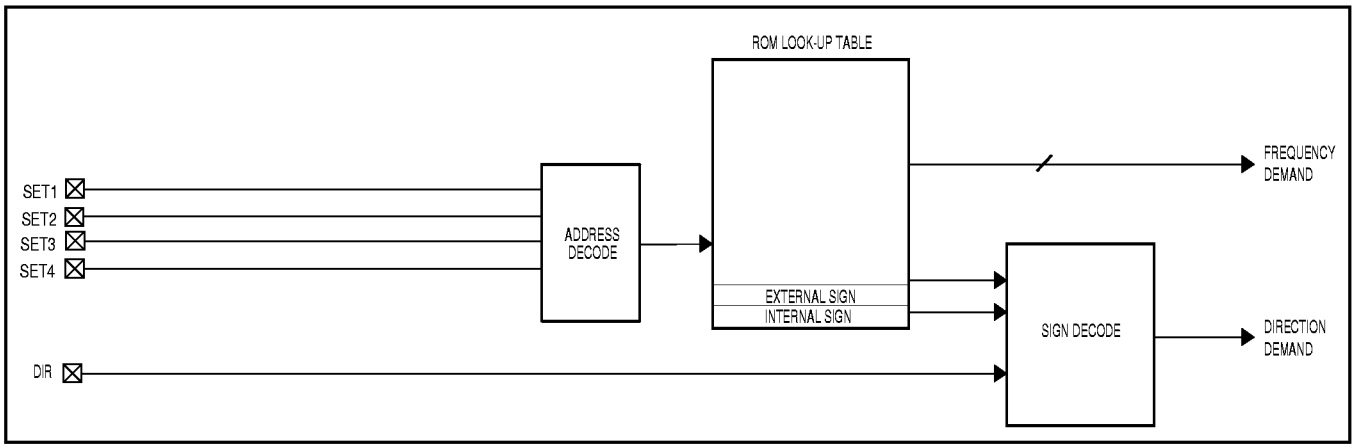


Fig. 3: Speed selection block

ACCELERATION/DECELERATION BLOCK

The acceleration/deceleration block consists of a 16-bit magnitude comparator and a 17-bit up/down counter clocked by the output from the Accel or Decel oscillators. The acceleration and deceleration rates are seperately selectable using external resistors and capacitors.

The time taken to accelerate from rest to frange (or to decelerate from frange to rest is given by:

$$t_{acc/dec} = \frac{131072\ RC}{\sqrt{2}} \quad \text{where} \quad 5k\Omega \leq R \leq 100k\Omega,\ 1nF \leq C \leq 25nF$$

If Raccel is connected to V_{SSA}, all acceleration and deceleration will be instantaneous (irrespective of Rdecel). This makes the device suitable for waveform generation applications such as UPS or SMPS. In this mode of operation it is not necessary to connect a resistor and capacitor to Rdecel, although the Rdecal pin must be tied low in this case.

The 16-bit magnitude comparator compares the scalar frequency demand from the Speed Reference Table with the instantaneous scalar frequency output from the up/down counter. The result is a 2-bit output as follows:-

UP	DOWN	RESULT
0	0	SAME, NO ACCEL OR DECEL
0	1	LOWER
1	0	HIGHER
1	1	ILLEGAL STATE

Table 2: Acceleration/deceleration decoder

These 2 bits are used in conjunction with the Vmonitor and Imonitor pins and the sign bits to obtain an absolute indication of the required acceleration/deceleration, according to the following rules:-

1) If the Vmonitor condition is invoked (Vmonitor $>V_{DDA/2}$), any acceleration/deceleration will be prevented until Vmonitor falls to $>V_{DDA/2.08}$. This condition has highest priority.

Normal acceleration/deceleration will continue when Vmonitor falls to $>V_{DDA/2.08}$, as dictated by the rest of the algorithm.

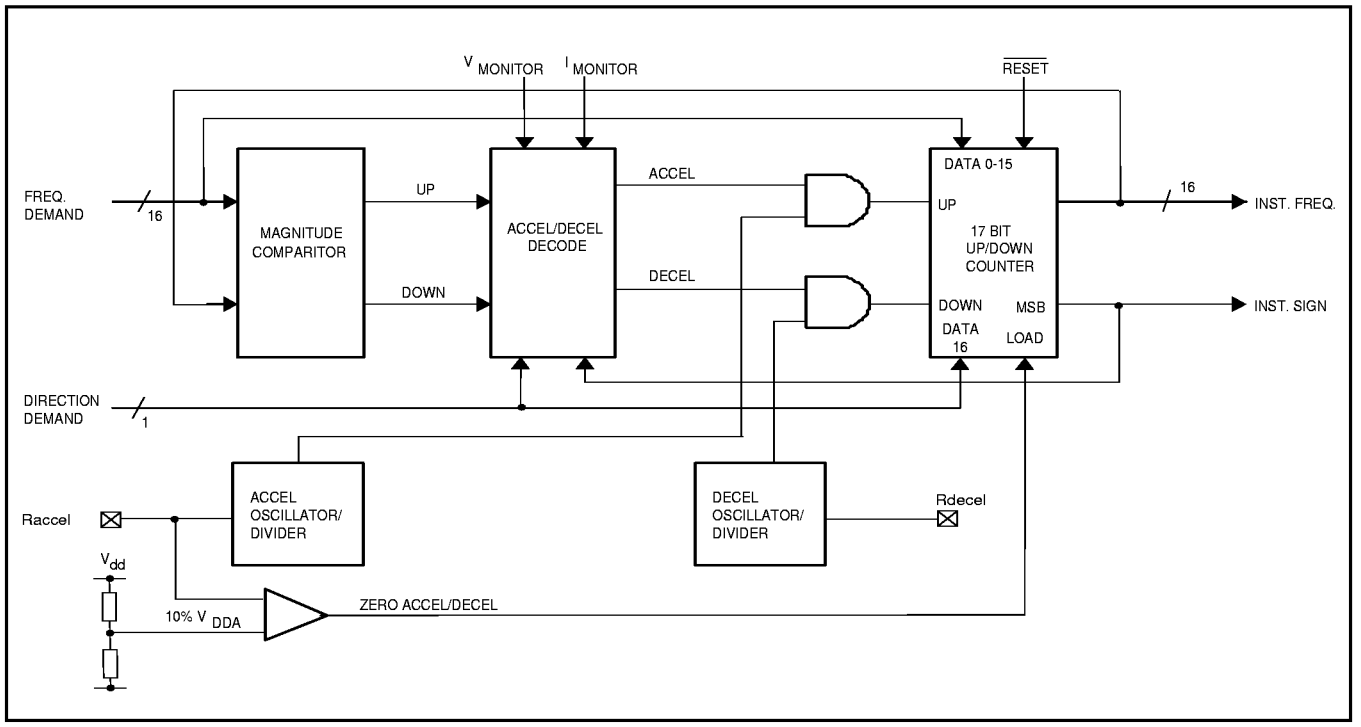


Fig. 4: Acceleration/deceleration block

This input is used to prevent excessive deceleration rates from regenerating too much power into the switching circuitry and causing an overvoltage condition.

2) If Imonitor is invoked (i.e. $>V_{DDA/2}$) the scalar value of the instantaneous frequency is reduced at the predetermined deceleration rate irrespective of the states of UP and DOWN. If the instantaneous frequency attains the value zero whilst Imonitor is $>V_{DDA/2}$ the PWM outputs are turned off (logic 0) for the duration of this condition (this prevents undue motor heating whilst at rest). No acceleration or deceleration is allowed once the frequency has attained the value zero. When Imonitor is released normal acceleration/deceleration resumes as required by the prevailing conditions. In addition, the PWM outputs are re-enabled.

This condition has lower priority than Vmonitor since the act of decelerating due to Imonitor being taken high may itself invoke the Vmonitor condition.

This input is intended to prevent too high an acceleration rate from causing an overcurrent/overtemperature situation at the switching devices.

3) If Imonitor and Vmonitor are inactive, the algorithm takes the UP and DOWN outputs from the magnitude comparator, together with the required sign from the Speed Reference Table and the instantaneous sign from the up/down counter to compute whether acceleration or deceleration is required:-

(a) If the required and instantaneous signs are different, the first requirement is to decelerate to rest since no change of direction is possible until this has occurred. Therefore, so long as this condition holds, decelerate (see 1 and 2 in Table 3).

(b) If the signs are the same and UP and DOWN are both zero then the required and instantaneous speeds are matched both in terms of direction and magnitude, therefore neither acceleration or deceleration is required (see 3 and 4 in Table 3).

(c) If the signs are the same but either UP or DOWN is high then the direction of rotation does not need to change, but the magnitude does. Therefore, if UP is high, accelerate or if DOWN is high, decelerate (see 5,6,7 and 8 in Table 3).

(d) UP and DOWN both high is an illegal state since both conditions cannot exist concurrently.

CONDITION	UP	DOWN	REQD. DIRECTION	INSTANT-ANEOUS DIRECTION	ACCEL	DECEL
					Active High	
1.	X	X	0	1	0	1
2.	X	X	1	0	0	1
3.	0	0	0	0	0	0
4.	0	0	1	1	0	0
5.	0	1	0	0	0	1
6.	0	1	1	1	0	1
7.	1	0	0	0	1	0
8.	1	0	1	1	1	0
9.	1	1	X	X	ILLEGAL STATE	

Table 3: Acceleration/deceleration block conditions

The ACCEL and DECEL signals are gated with the accel or decel oscillator to increment or decrement the speed.

This algorithm is clarified above in a flow diagram of Fig.5.

The counter is a 17-bit synchronous up/down counter, the most significant bit being the instantaneous sign or direction bit. The reset condition of this block is a logic 1 on the sign bit (MSB) and zeros on all other bits, being representative of zero speed and a forward direction. Zero speed must always be represented in this way to prevent confusion between +/- 0, therefore -0 is not a valid state and on no account is programmed.

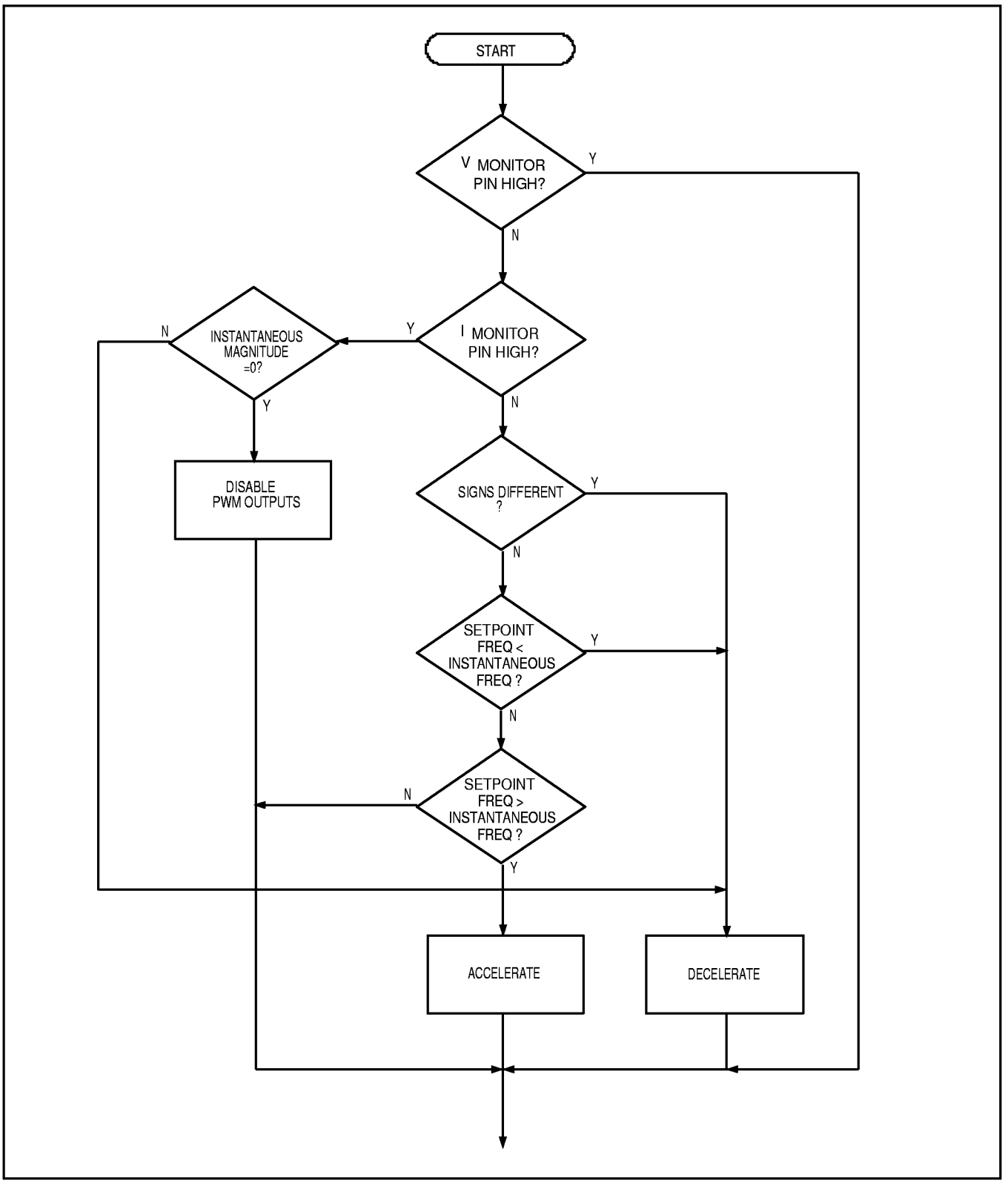


Fig. 5: Acceleration/deceleration block flow diagram

AMPLITUDE CONTROL BLOCK

In order to ensure adequate control of motor flux, the SA868/9 controls the motor voltage at all frequencies. The general form of the voltage/frequency curve is shown in Fig.6.

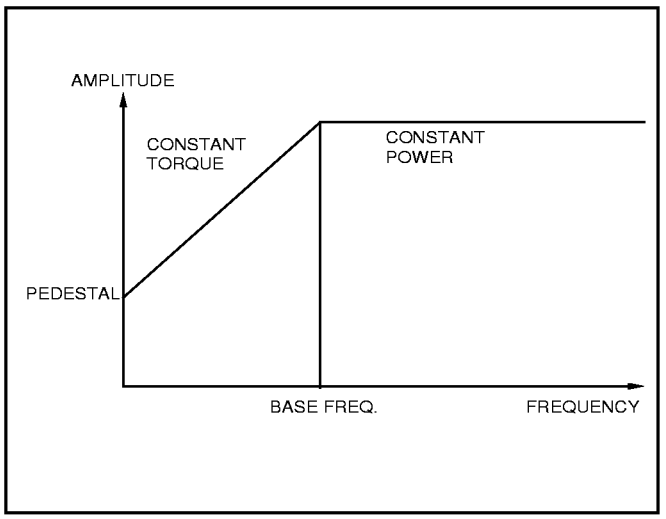


Fig. 6: General form of the voltage/frequency curve

At zero frequency a variable 'Pedestal' voltage is applied to the motor to overcome copper losses. The voltage then increases in proportion to the frequency up to the selectable 'Base Frequency'. This is generally 50Hz or 60Hz but may be selected to be anywhere in the frequency range. Frequencies up to the Base Frequency are said to be in the Constant Torque region.

Beyond the Base Frequency the amplitude is held at its maximum value. This inevitably leads to a fall in the generated torque with increasing frequency. Hence this is termed the Constant Power region.

The SA868/9 incorporates an Amplitude Control Block as shown in Fig.7.

The instantaneous frequency word is multiplied by the preselected Gradient word. The result is added to the 8-bit Pedestal value and the result is rounded to 8 bits by the Overflow Detection/Correction circuit before being passed to the PWM generator blocks.

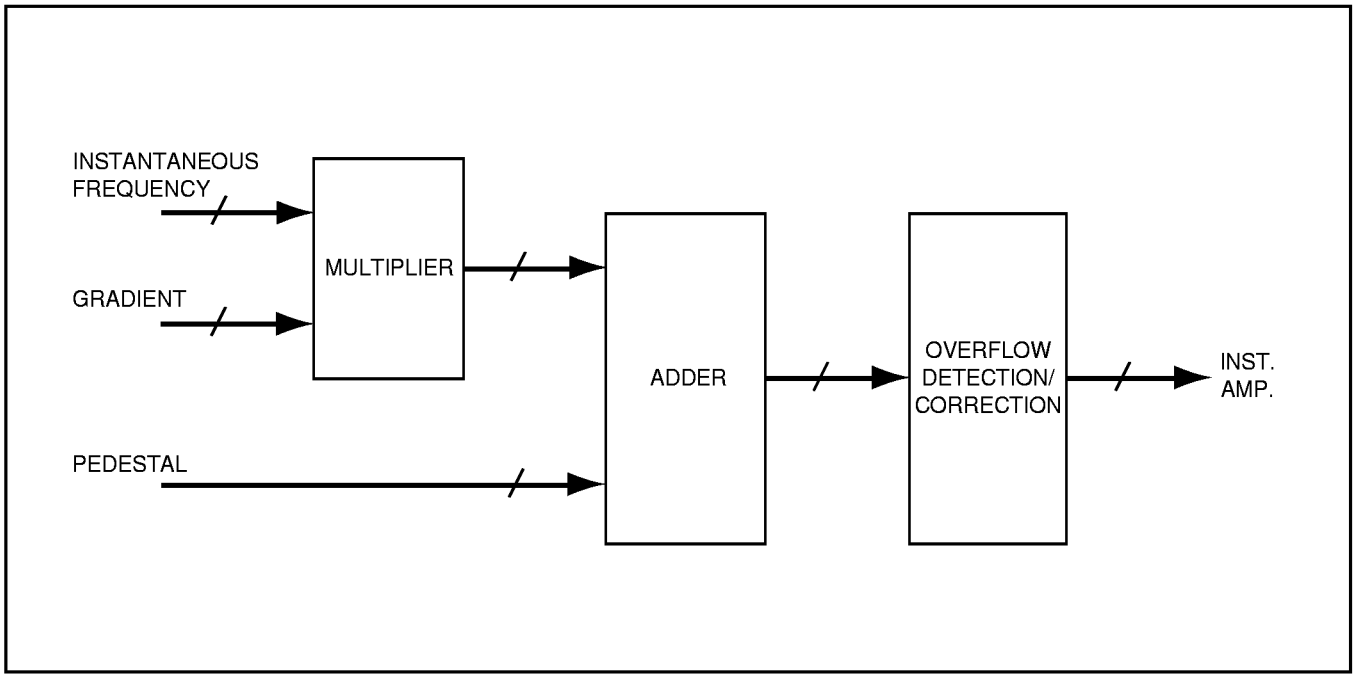


Fig. 7: Amplitude control block diagram

FACTORY MASKED INITIALISATION PARAMETERS

CARRIER FREQUENCY SELECTION

The carrier frequency is a function of the externally applied clock frequency and a division ratio *n*, determined by the 3-bit CFS word set during initialisation. The values of *n* are selected as shown in Table 4.

CFS word	101	100	011	010	001	000
Value of n	5	4	3	2	1	0

Table 4 Values of clock division ratio n

The carrier frequency, f_{CARR}, is then given by:

$$f_{CARR} = \frac{f_{CLK}}{512 \times 2^{n+1}}$$

where f_{CLK} = clock input frequency.

POWER FREQUENCY RANGE SELECTION

The power frequency range defines the maximum limit of the power frequency. The operating power frequency is controlled by the 16-bit Power Frequency Select (PFS) word in the Control Register.

The power frequency range is a function of the carrier waveform frequency (f_{CARR}) and a multiplication factor *m*, determined by the 3-bit FRS word. The value of *m* is determined as shown in Table 5.

FRS word	110	101	100	011	010	001	000
Value of m	6	5	4	3	2	1	0

Table 5 Values of carrier frequency multiplicaion factor m

The power frequency range, f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR} \times 2^{m}}{384}$$

where f_{CARR} = carrier frequency.

PULSE DELAY TIME

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and PDY, defined by the 6-bit pulse delay time select word. The value of PDY is selected as shown in Table 6.

PDY word	111111	111110	...etc...	000000
Value of PDY	63	62	...etc...	0

Table 6 Values of PDY

The pulse delay time, t_{pdy}, is then given by:

$$t_{pdy} = \frac{64 - PDY}{f_{CARR} \times 512}$$

where f_{CARR} = carrier frequency.

Fig.8 shows the effect of pulse delay on a pure PWM waveform.

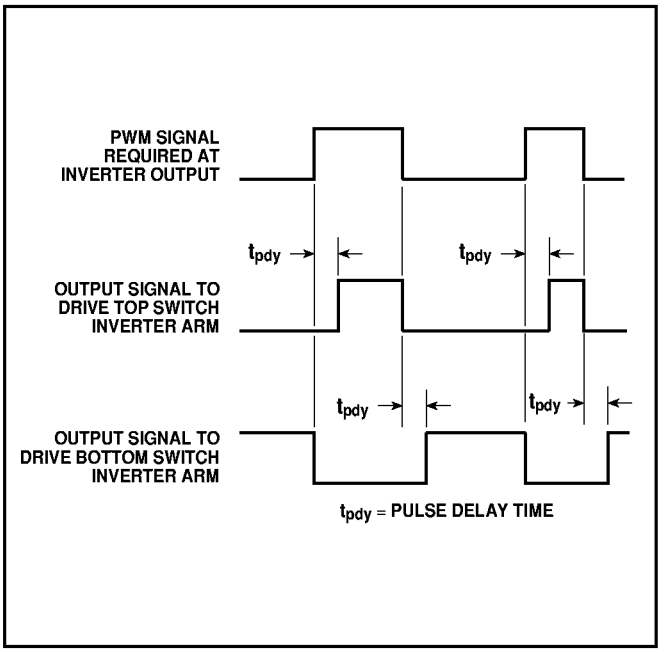


Fig.8 Effect of pulse delay on PWM pulse train

PULSE DELETION TIME

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the Initialisation Register. If a pulse (either positive or negative) is greater than or equal in duration to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd}, is a function of the carrier wave frequency and PDT, defined by the 7-bit pulse deletion time word. The value of PDT is selected as shown in Table 7.

PDT word	1111111	1111110	...etc...	0000000
Value of PDT	127	126	...etc...	0

Table 7 Values of PDT

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{128 - PDT}{f_{CARR} \times 512}$$

where f_{CARR} = carrier frequency.

Fig. 9 shows the effect of pulse deletion on a pure PWM waveform.

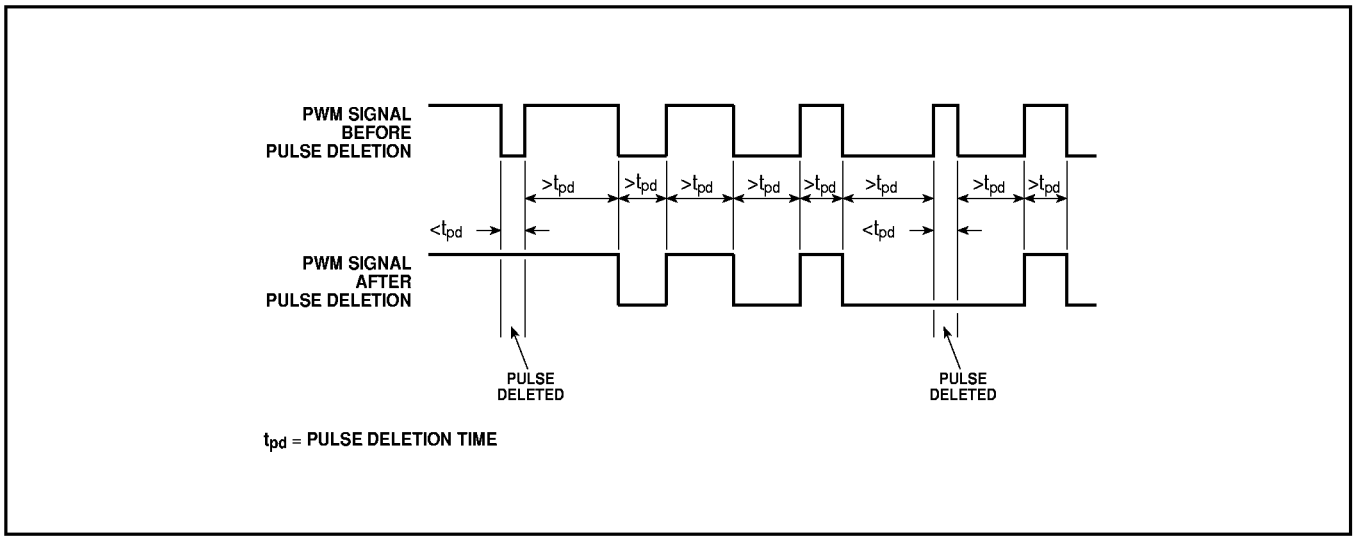


Fig.9 The effect of the pulse delay deletion circuit

WAVEFORM SELECTION

Two bits, WS0 and WS1, are used to define the power waveform, according to Table 8:

WS1	WS0	Waveform
0	0	Sinusoid (default)
0	1	Triplen (harmonic injection)
1	0	Deadbanding (switching loss reduction)
1	1	Reserved for customer specific variants

Table 8: Waveform Selection

The waveforms may be described by the following mathematical relationships and are shown graphically in Fig. 10:

Sinusoid:

$f(t) = A \sin(\omega t)$ *where A = amplitude, ω = angular displacement*

Triplen:

$f(t) = 2A \sin(\omega t + 30) - 1$ } $0 < \omega < 60,\ 120 < \omega < 240,\ 300 < \omega < 360$

$f(t) = 1$ } $60 <= \omega <= 120,\ 240 <= \omega <= 300$

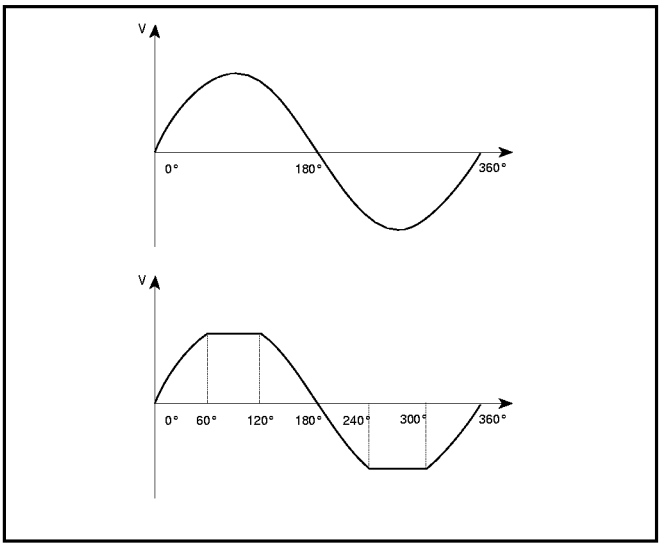


Fig.10 Waveforms implemented in SA868/9

VOLTAGE/FREQUENCY GRADIENT SELECTION

GRAD7	GRAD6	GRAD5	GRAD4	GRAD3	GRAD2	GRAD1	GRAD0
MSB							LSB

This parameter is used to define the Voltage/Frequency gradient in the Constant Torque region of motor operation - as shown in Fig.6. Its value is dependent upon the PEDESTAL value and the BASE FREQUENCY according to the following equation:

$$GRAD = \frac{(255 - PEDESTAL)\ f_{range}}{f_{base} \times 16}$$

where $0 \leq GRAD \leq 255$

PEDESTAL SELECTION

PED7	PED6	PED5	PED4	PED3	PED2	PED1	PED0
MSB							LSB

This pedestal value defines the voltage present on the motor at zero frequency and is used to counteract the effects of the copper loss which tends to dominate the overall losses at low speeds. The specific value should be chosen carefully to ensure that the power dissipation in the motor is not excessive.

It is possible to defeat the Voltage/Frequency profile if necessary by setting Pedestal = 255.

$$PEDESTAL\ value\ (\%) = \frac{PED \times 100}{255}$$

where $0 \leq PED \leq 255$

HARDWARE INPUT/OUTPUT FUNCTIONS

SET TRIP INPUT

The SET TRIP allows an external, active high event to provide a rapid shutdown of the PWM signals. When the SET TRIP input is taken to a logic 1, a delay of 3-4 master clock cycles is triggered internally. If, at the end of this delay, the SET TRIP input has remained high, then the PWM outputs will be shut down and the $\overline{\text{TRIP}}$ acknowledge output will become active.

This condition can only be cleared by applying a $\overline{\text{RESET}}$ cycle.

The SET TRIP input has an internal pull-down resistor with a value of approximately 100kΩ

OUTPUT TRIP STATUS

The $\overline{\text{TRIP}}$ output indicates the status of the trip latch and is active low. It does not become active until the end of the SET TRIP delay time (assuming that the SET TRIP input stays high for this period).

This output is capable of directly driving an LED through a current limiting resistor for display purposes.

$\overline{\text{RESET}}$ INPUT

The $\overline{\text{RESET}}$ input is active low and performs the following functions:-

i) All PWM outputs are forced low
ii) All internal counters are reset to zero
iii) The instantaneous frequency word is set to zero and the direction bit to 1 (forward).
iv) When released, the rising edge reactivates the PWM outputs and sets the trip latch to inactive, provided that the SET TRIP input is inactive and SET1 : SET4 ≠0.

$\overline{\text{RESET}}$ must be held low for a minimum of 2 Raccel Caccel seconds at power up to prevent acceleration defeat.

As a consequence of (iii) and (iv) the device will be re-enabled and will re-accelerate when reset after a $\overline{\text{TRIP}}$ event.

TEST MODE

A test mode is provided for in-house test purposes. This mode is invoked by linking the $\overline{\text{TRIP}}$ and DIR pins during RESET. A pulse train is output on the $\overline{\text{TRIP}}$ pin, and if detected at the DIR pin the device enters test mode. The pulses are no more than $1/2_{fCLK}$ seconds in length to minimise the disturbance to the $\overline{\text{TRIP}}$ circuitry. No pulses are sent after $32/_{fCLK}$ seconds following $\overline{\text{RESET}}$ going low. These tests continue even when $\overline{\text{RESET}}$ becomes inactive. A subsequent $\overline{\text{RESET}}$ toggle will always force the device out of test mode so long as no connection exists between $\overline{\text{TRIP}}$ and DIR.

XTAL1/XTAL2

These pins are for the crystal or ceramic resonator, if used. Alternatively, XTAL1 may be used as an input for an externally generated clock signal. Any external input is constrained to having a mark/space ratio of 1:1 ± 20% to ensure correct device operation.

A small capacitor (approx 33pF) should be connected from each of these pins to the negative supply rail when using a crystal or ceramic resonator. However, no other components are necessary.

$V_{MONITOR}$ INPUT

Analog input which, when $>V_{DDA/2}$ inhibits acceleration and deceleration. This input has higher priority than the $I_{monitor}$ pin and the Vmonitor condition therefore prevails if both $V_{monitor}$ and $I_{monitor}$ are active simultaneously.

DIR INPUT

Logical input which, in combination with External Sign and Internal Sign bits allow direction of rotation of PWM outputs to be reversed. A high input (when allowed by External Sign bit) causes forward rotation and low causes reverse rotation. This pin is must be tied to V_{SSD} on the SA869.

$I_{MONITOR}$ INPUT

Analog input which causes the instantaneous output frequency to reduce at the predetermined deceleration rate when $>V_{DDA/2}$. If the frequency is reduced to zero whilst this input is $>V_{DDA/2}$. the PWM outputs are temporarily turned off and the deceleration inhibited. Normal acceleration may resume when $I_{monitor}$ is below $>V_{DDA/2.08}$. In addition, the PWM outputs are re-enabled in the event that the frequency had fallen to zero.

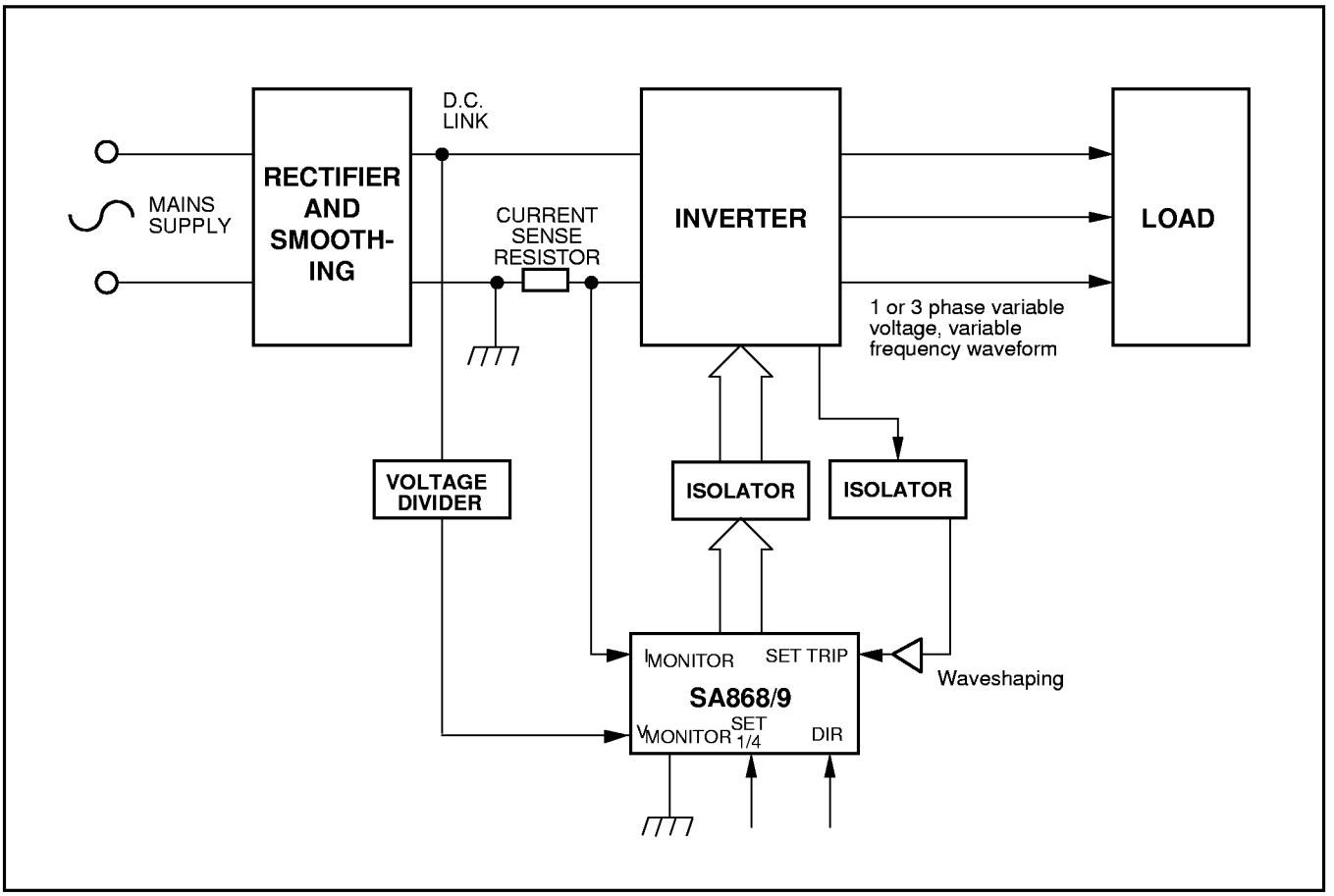
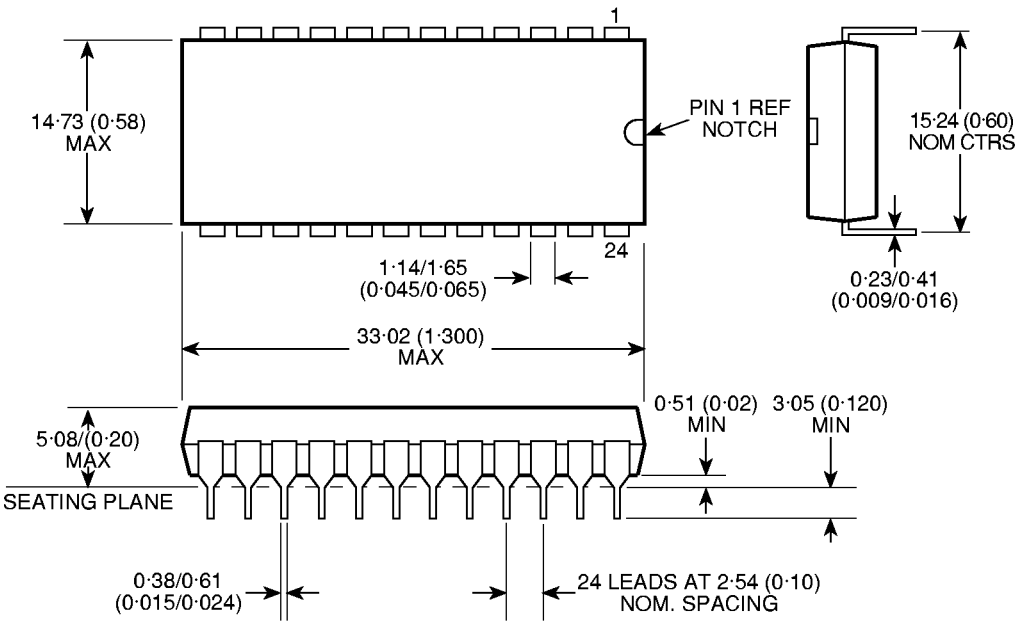


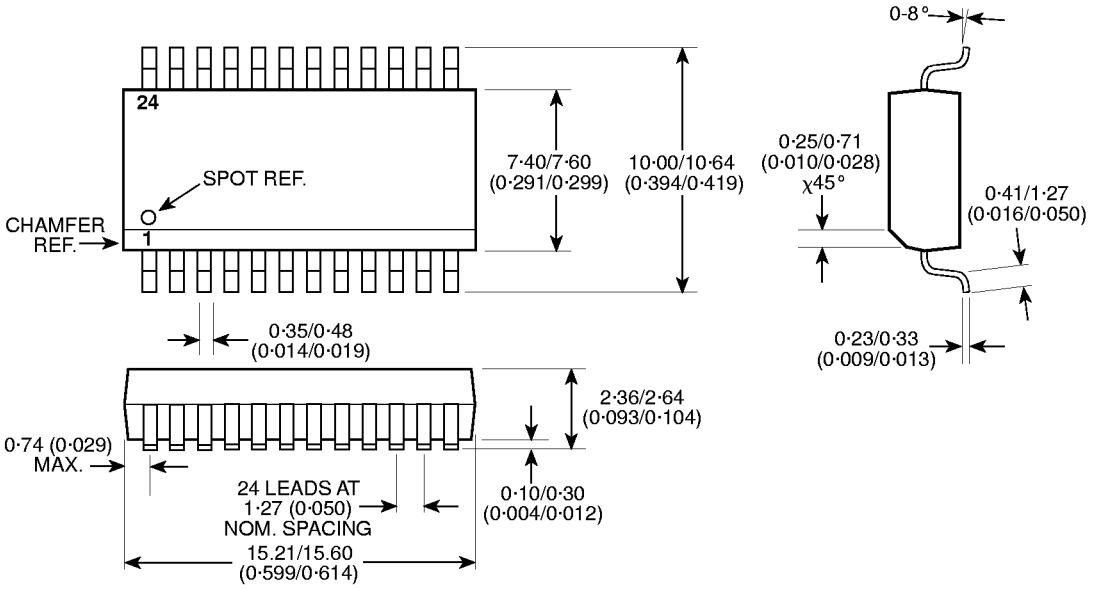
Fig. 11 Typical applications circuit

PACKAGE DETAILS

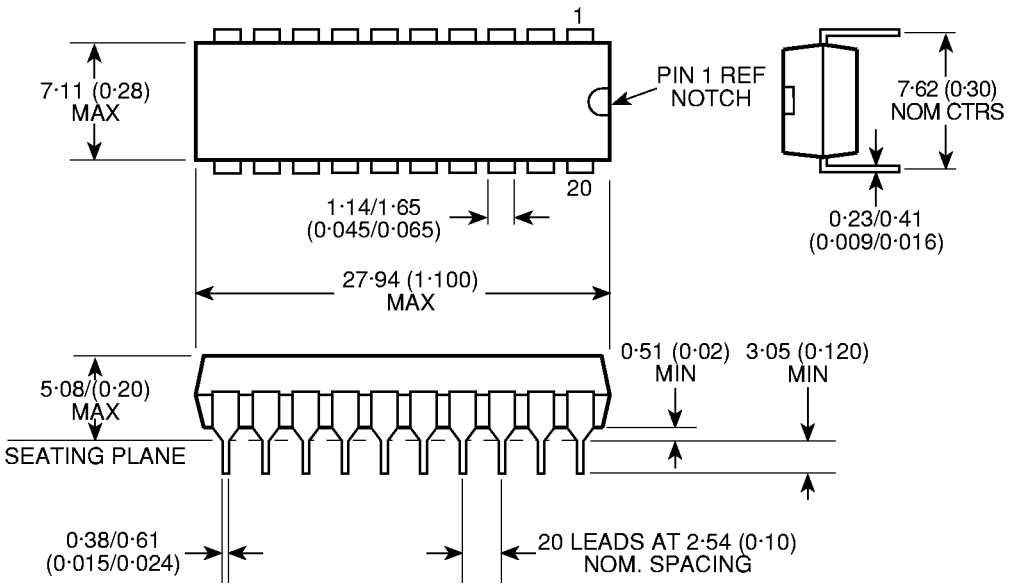
Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



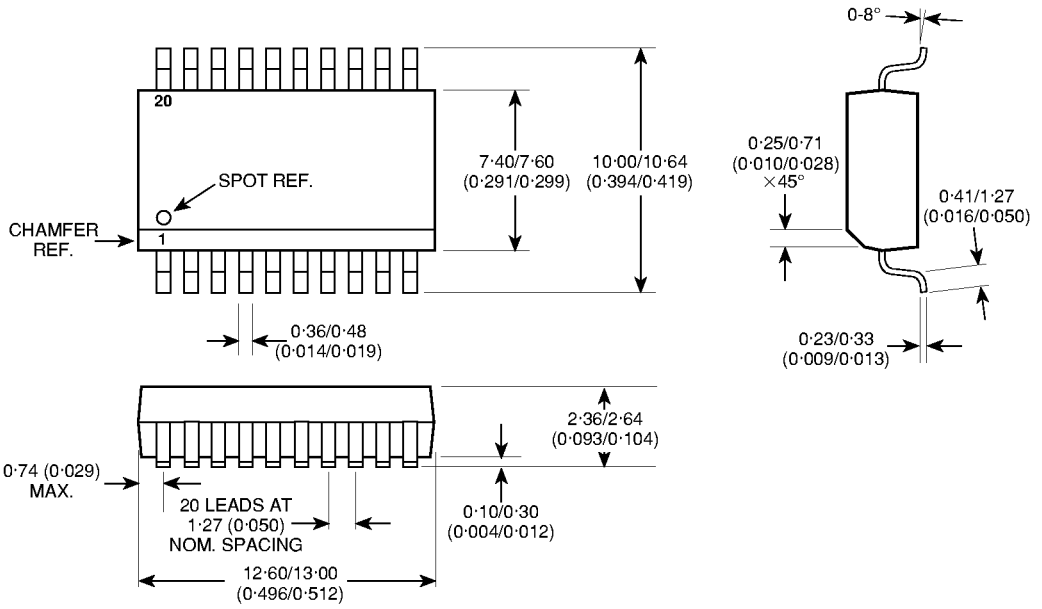
24-LEAD PLASTIC DIL – DP24



24-LEAD MINIATURE PLASTIC DIL - MP24



20-LEAD PLASTIC DIL – DP20



20-LEAD MINIATURE PLASTIC DIL - MP20

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