



## P-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package						
			TO-39	TO-52	TO-92	TO-220	Quad P-DIP	Quad C-DIP*	DICE†
-40V	8Ω	-0.5A	VP0104N2	VP0104N9	VP0104N3	VP0104N5	VP0104N6	VP0104N7	VP0104ND
-60V	8Ω	-0.5A	VP0106N2	VP0106N9	VP0106N3	VP0106N5	VP0106N6	VP0106N7	VP0106ND
-90V	8Ω	-0.5A	VP0109N2	VP0109N9	VP0109N3	VP0109N5	—	—	VP0109ND

\* 14 pin side brazed ceramic DIP

† MIL visual screening available

### High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

### Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

### Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

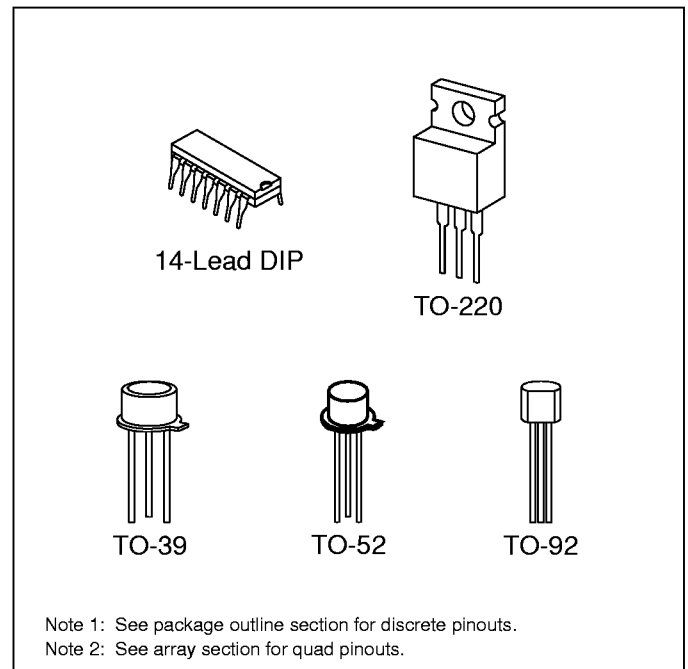
\* Distance of 1.6 mm from case for 10 seconds.

### Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{ja}$ $^\circ\text{C/W}$	$\theta_{jc}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-39	-0.45A	-1.0A	3.5W	125	35	-0.45A	-1.0A
TO-52	-0.25A	-1.0A	1.0W	240	125	-0.25A	-1.0A
TO-92	-0.25A	-0.8A	1.0W	170	125	-0.25A	-0.8A
TO-220	-1.0A	-1.2A	15.0W	70	8.3	-1.0A	-1.2A
Plastic DIP	Refer to Arrays & Special Functions Section.						
Ceramic DIP							

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

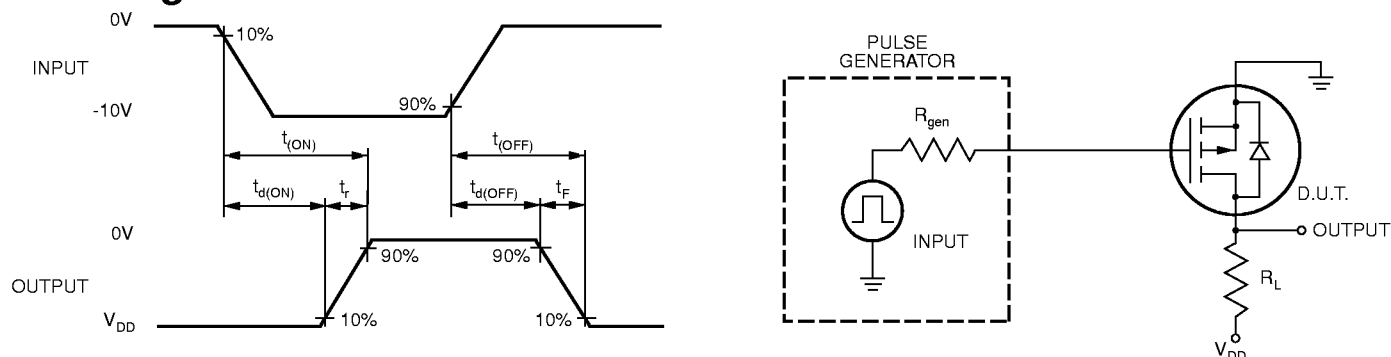
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	VP0109	-90			V	$I_D = -1.0\text{mA}$ , $V_{GS} = 0\text{V}$
		VP0106	-60				
		VP0104	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	$V_{GS} = V_{DS}$ , $I_D = -1.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			5.8	6.5	mV/ $^\circ\text{C}$	$I_D = -1.0\text{mA}$ , $V_{GS} = V_{DS}$
$I_{GSS}$	Gate Body Leakage			-1.0	-100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current				-10	$\mu\text{A}$	$V_{GS} = 0\text{V}$ , $V_{DS} = \text{Max Rating}$
					-1	mA	$V_{GS} = 0\text{V}$ , $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		-0.15	-0.25		A	$V_{GS} = -5\text{V}$ , $V_{DS} = -25\text{V}$
			-0.50	-1.2			$V_{GS} = -10\text{V}$ , $V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			11	15	$\Omega$	$V_{GS} = -5\text{V}$ , $I_D = -0.1\text{A}$
				6	8		$V_{GS} = -10\text{V}$ , $I_D = -0.5\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.55	1.0	%/ $^\circ\text{C}$	$I_D = -0.5\text{A}$ , $V_{GS} = -10\text{V}$
$G_{FS}$	Forward Transconductance		150	190		m $\Omega$	$V_{DS} = -25\text{V}$ , $I_D = -0.5\text{A}$
$C_{ISS}$	Input Capacitance			45	60	pF	$V_{GS} = 0\text{V}$ , $V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance			22	30		
$C_{RSS}$	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			4	6	ns	$V_{DD} = -25\text{V}$ $I_D = -0.5\text{A}$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			3	7		
$t_f$	Fall Time			4	10		
$V_{SD}$	Diode Forward Voltage Drop			-1.2	-2.0	V	$I_{SD} = -1.0\text{A}$ , $V_{GS} = 0\text{V}$
$t_{rr}$	Reverse Recovery Time			400		ns	$I_{SD} = -1.0\text{A}$ , $V_{GS} = 0\text{V}$

### Notes:

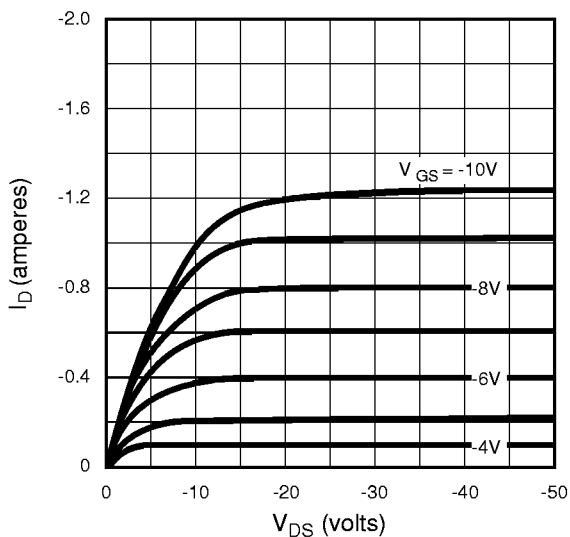
- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

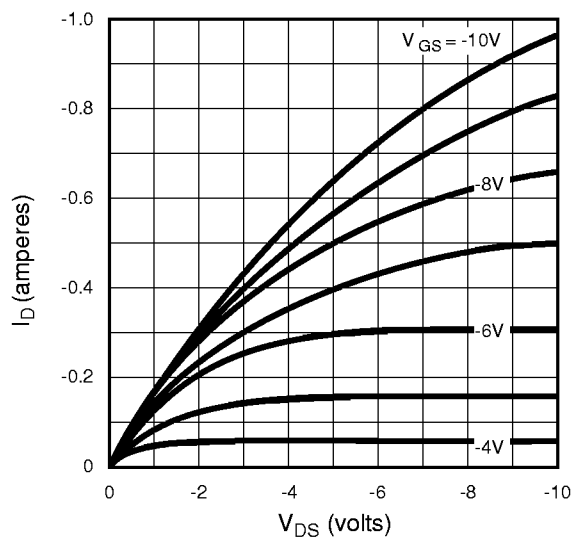


# Typical Performance Curves

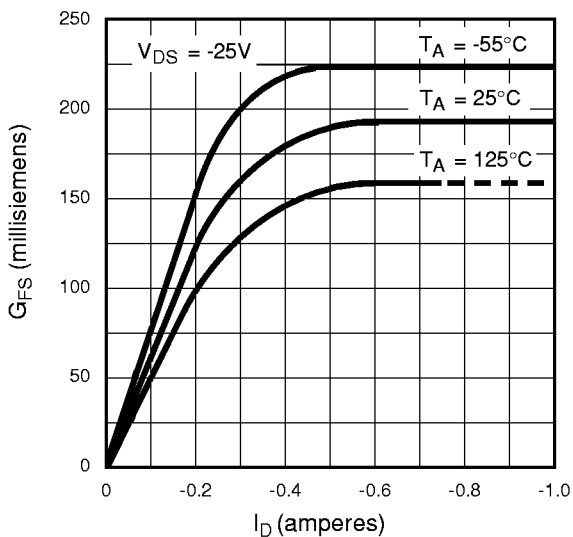
Output Characteristics



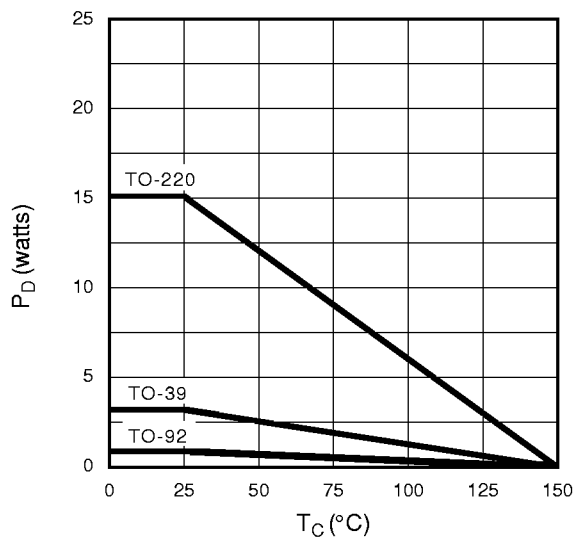
Saturation Characteristics



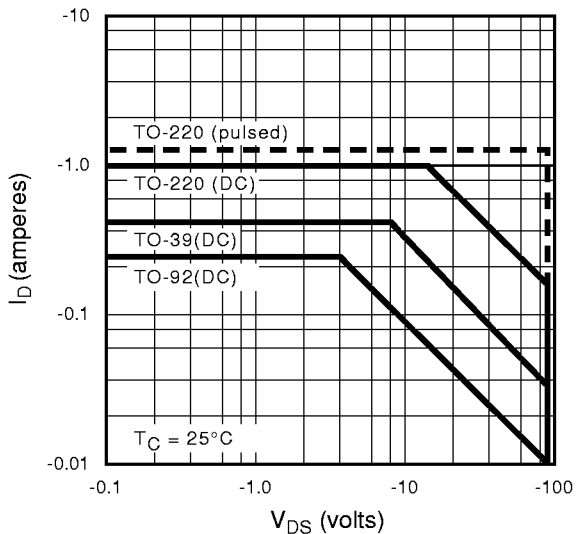
Transconductance vs. Drain Current



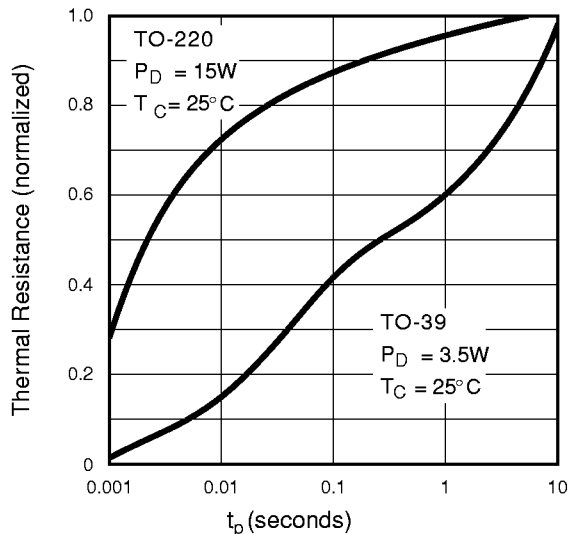
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

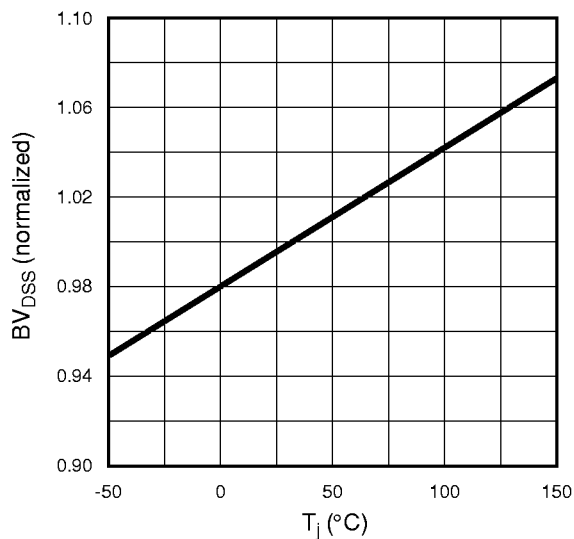


Thermal Response Characteristics

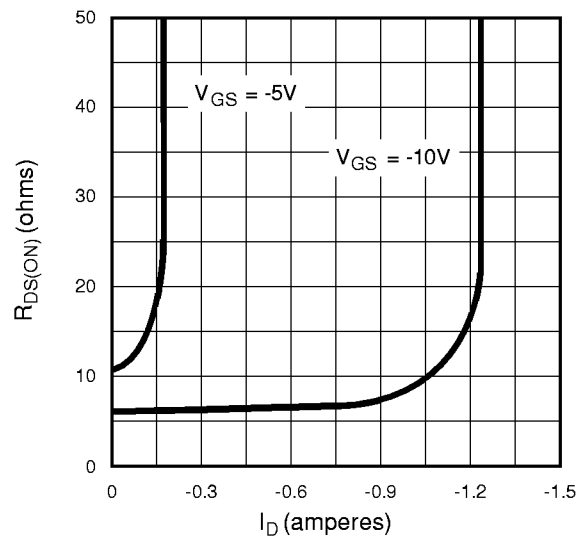


# Typical Performance Curves

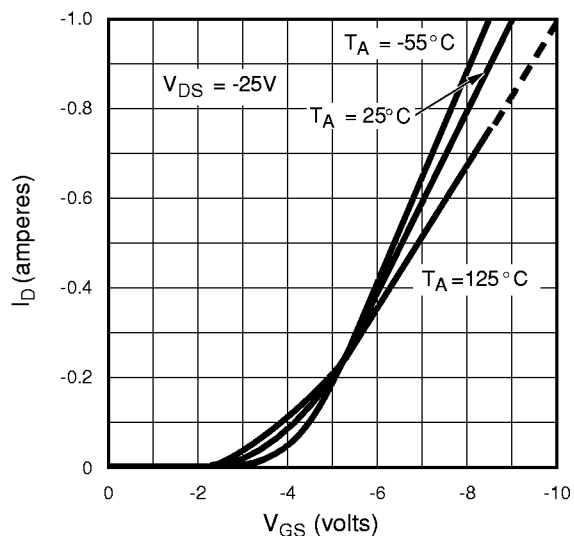
BV<sub>DSS</sub> Variation with Temperature



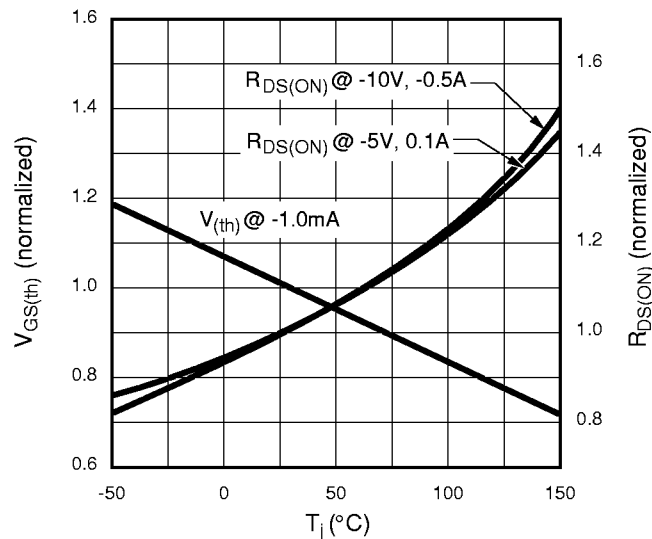
On-Resistance vs. Drain Current



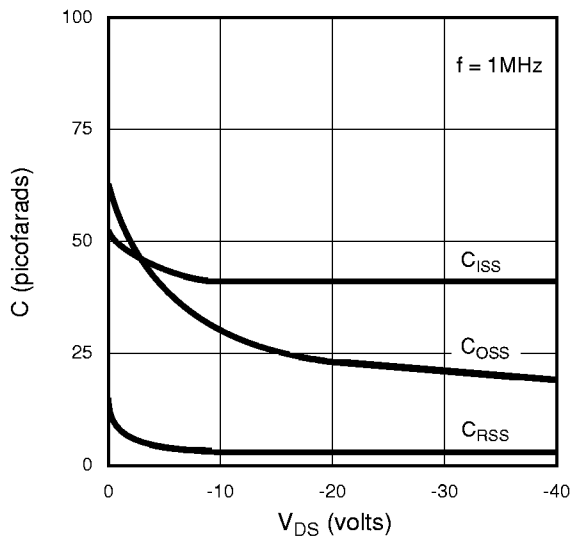
Transfer Characteristics



V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

