

HA17324A Series

Quad Operational Amplifier

HITACHI

ADE-204-031B (Z)

Rev.2
May 2001

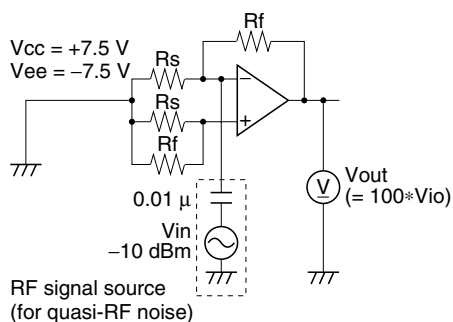
Description

HA17324A series are quad operational amplifier that provide high gain and internal phase compensation, with single power supply. They can be widely used to control equipments.

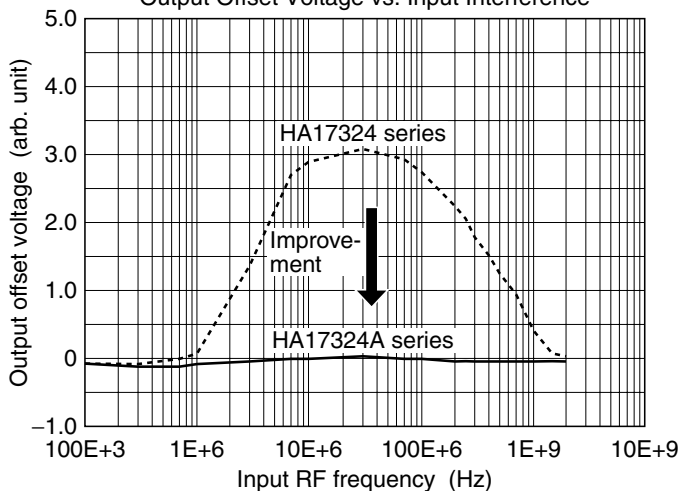
Features

- Wide range of supply voltage, and single power supply used
- Internal phase compensation
- Wide range of common mode voltage, and possible to operate with an input about 0 V
- Low electro-magnetic susceptibility level

Measurement Condition



Output Offset Voltage vs. Input Interference

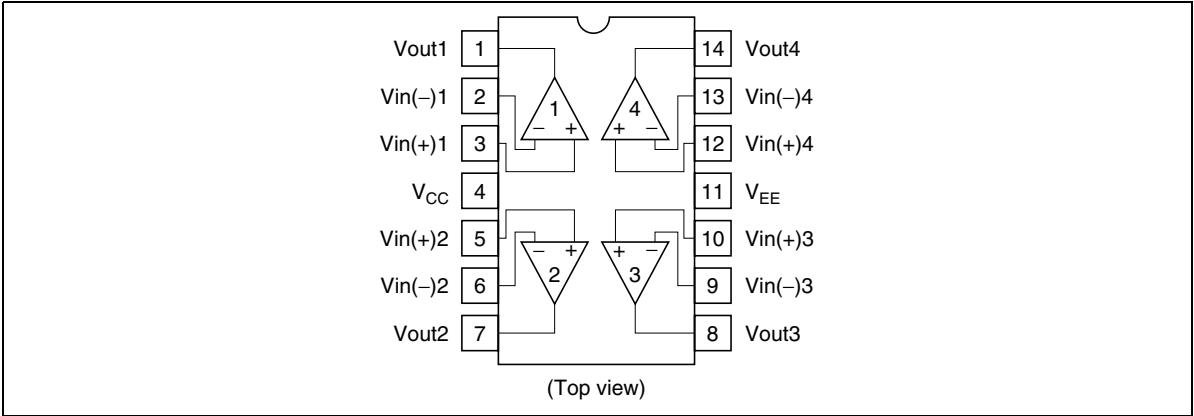


HA17324A Series

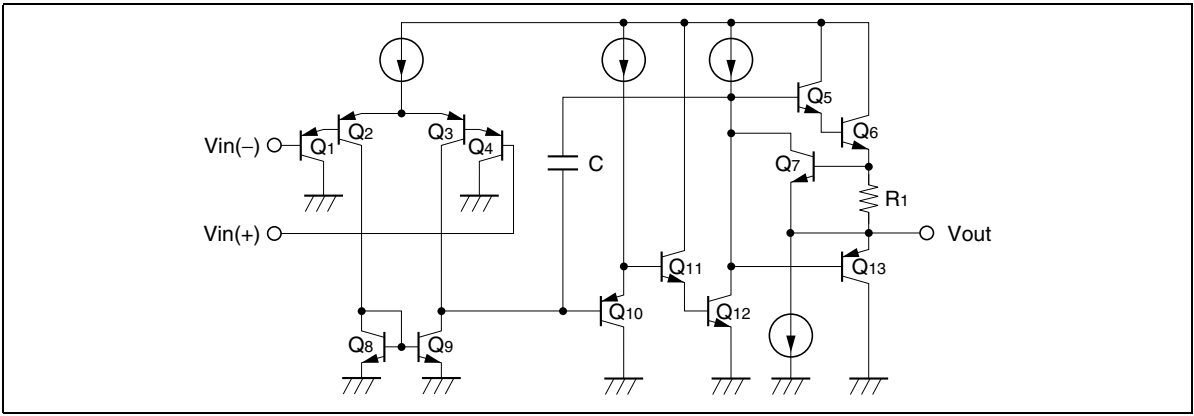
Ordering Information

Type No.	Application	Package
HA17324A	Commercial use	DP-14
HA17324AF		FP-14DA
HA17324ARP		FP-14DN

Pin Arrangement



Circuit Schematic (1/4)



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	32	V
Sink current	I_{sink}	50	mA
Power dissipation	P_T	625 ^{*1,2}	mW
Common mode input voltage	V_{CM}	-0.3 to V_{CC}	V
Differential input voltage	V_{in} (diff)	$\pm V_{CC}$	V
Operating temperature	T_{opr}	-40 to $+85$	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to $+125$	$^\circ\text{C}$

Notes: 1. For the DILP package.

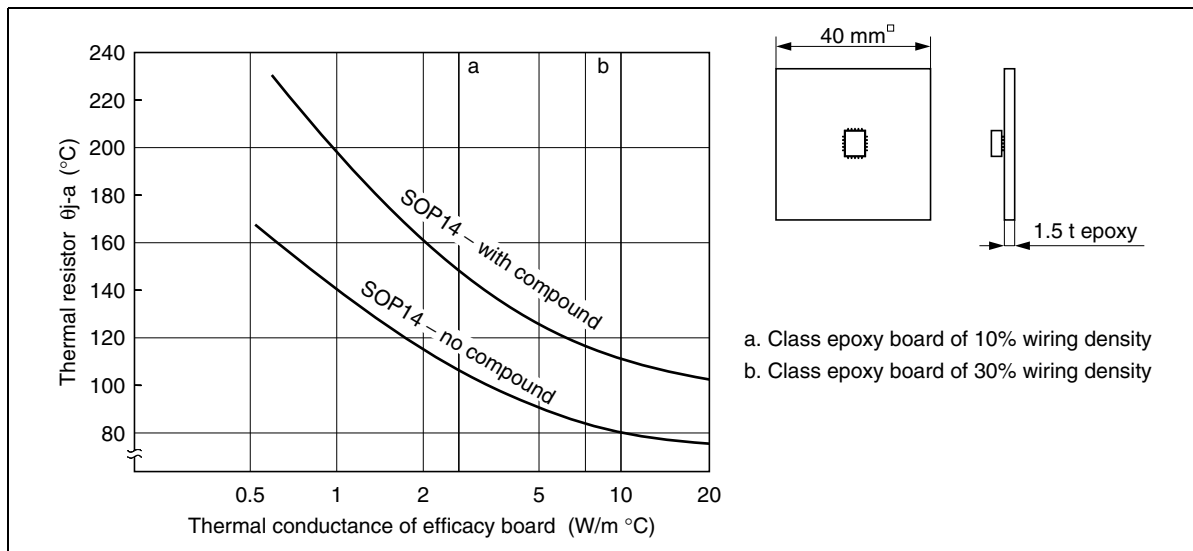
This is the allowable values up to $T_a = 50^\circ\text{C}$. Derate by $8.3 \text{ mW}/^\circ\text{C}$.

2. For the SOP package.

$T_{jmax} = \theta_{j-a} \cdot P_{c,max} + T_a$ (θ_{j-a} ; Thermal resistor between junction and ambient at set board use).

The wiring density and the material of the set board must be chosen for thermal conductance of efficacy board.

And $P_{c,max}$ cannot be over the value of P_T .



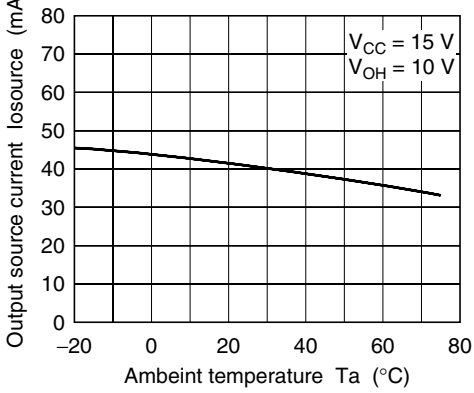
Electrical Characteristics

($V_{CC} = +15\text{ V}$, $T_a = 25^\circ\text{C}$)

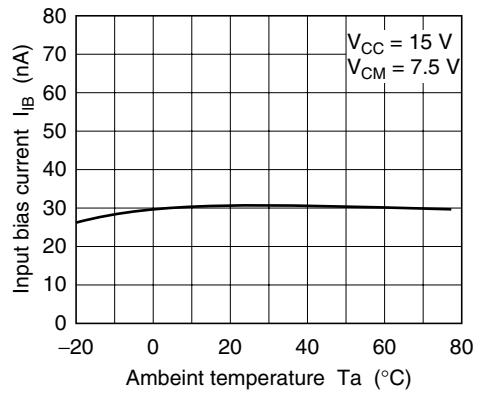
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input offset voltage	V_{IO}	—	2	7	mV	$V_{CM} = 7.5\text{ V}$, $R_S = 50\ \Omega$, $R_f = 50\text{ k}\Omega$
Input offset current	I_{IO}	—	5	50	nA	$V_{CM} = 7.5\text{ V}$, $I_{IO} = I_{I(-)} - I_{I(+)} $
Input bias current	I_{IB}	—	30	500	nA	$V_{CM} = 7.5\text{ V}$
Power source rejection ratio	PSRR	—	93	—	dB	$f = 100\text{ Hz}$, $R_S = 1\text{ k}\Omega$, $R_j = 100\text{ k}\Omega$
Voltage gain	A_{VD}	75	90	—	dB	$R_S = 1\text{ k}\Omega$, $R_f = 100\text{ k}\Omega$, $R_L = \infty$
Common mode rejection ratio	CMR	—	80	—	dB	$R_S = 50\ \Omega$, $R_f = 5\text{ k}\Omega$
Common mode input voltage range	V_{CM}	-0.3	—	13.5	V	$R_S = 1\text{ k}\Omega$, $R_f = 100\text{ k}\Omega$, $f = 100\text{ Hz}$
Maximum output voltage	V_{op-p}	—	13.6	—	V	$f = 100\text{ Hz}$, $R_S = 1\text{ k}\Omega$, $R_f = 100\text{ k}\Omega$, $R_L = 20\text{ k}\Omega$
Output source current	$I_{osource}$	20	40	—	mA	$V_{IN}^+ = 1\text{ V}$, $V_{IN}^- = 0\text{ V}$, $V_{OH} = 10\text{ V}$
Output sink current	I_{osink}	10	20	—	mA	$V_{IN} = 0\text{ V}$, $V_{IN} = 1\text{ V}$, $V_{OL} = 2.5\text{ V}$
Supply current	I_{CC}	—	0.8	2	mA	$V_{IN} = \text{GND}$, $R_L = \infty$
Slew rate	SR	—	0.19	—	V/ μs	$f = 1.5\text{ kHz}$, $V_{CM} = 7.5\text{ V}$, $R_L = \infty$
Channel separation	CS	—	120	—	dB	$f = 1\text{ kHz}$
Output sink current	I_{osink}	15	50	—	μA	$V_{IN}^+ = 0\text{ V}$, $V_{IN}^- = 1\text{ V}$, $V_{OL} = 200\text{ mV}$
	I_{osink}	3	9	—	mA	$V_{IN}^+ = 0\text{ V}$, $V_{IN}^- = 1\text{ V}$, $V_{OL} = 1\text{ V}$
Output voltage	V_{OH}	13.2	13.6	—	V	$I_{OH} = -1\text{ mA}$
	V_{OH}	12.0	13.3	—	V	$I_{OH} = -10\text{ mA}$
Output voltage	V_{OL}	—	0.8	1.0	V	$I_{OL} = 1\text{ mA}$
	V_{OL}	—	1.1	1.8	V	$I_{OL} = 10\text{ mA}$

Characteristic Curves

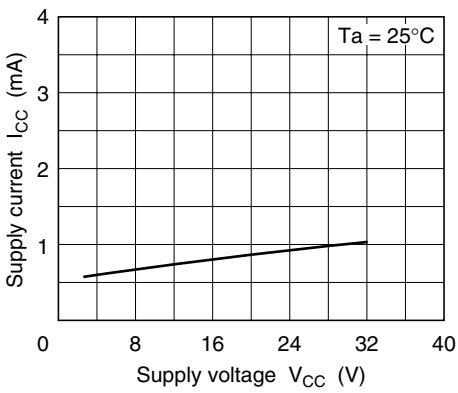
Output Source Current vs. Ambient Temperature



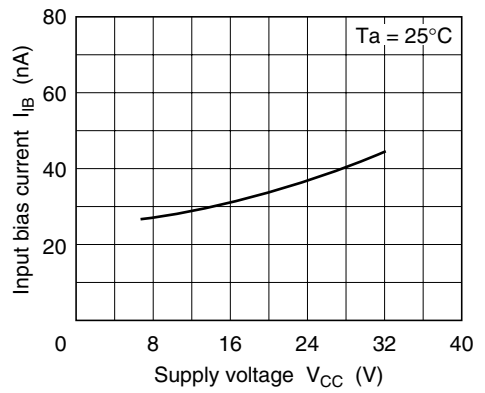
Input Bias Current vs. Ambient Temperature



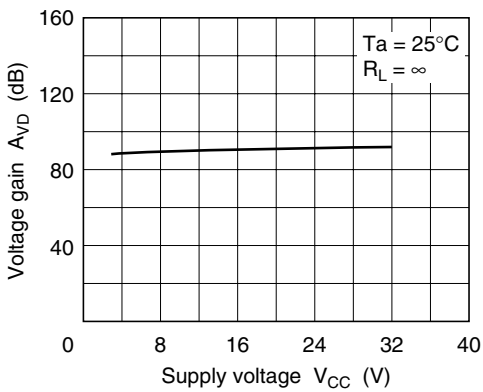
Supply Current vs. Supply Voltage



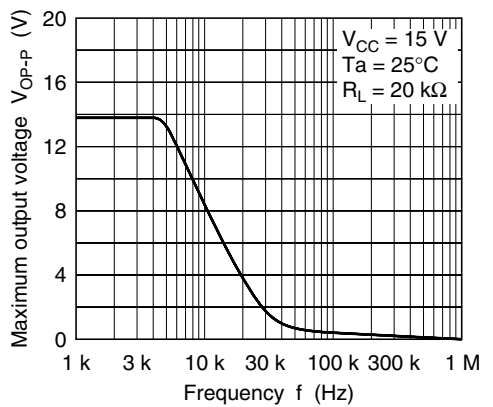
Input Bias Current vs. Supply Voltage

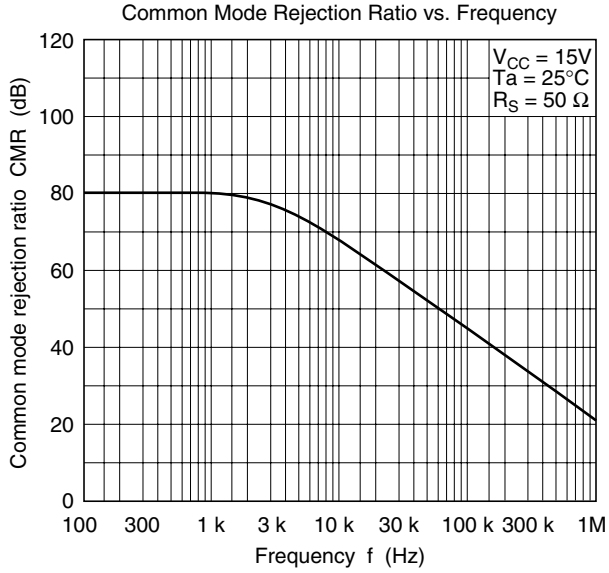
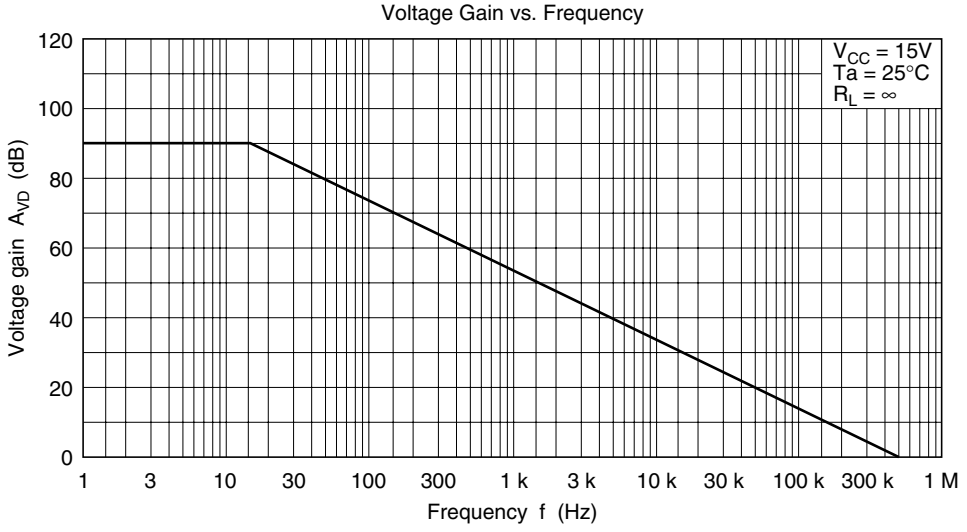


Voltage Gain vs. Supply Voltage



Maximum Output Voltage vs. Frequency





Solder Mounting Method

1. Small and light surface-mount packages require special attentions on solder mounting.
On solder mounting, pre-heating before soldering is needed.
The following figure show an example of infrared rays reflow.
2. The difference of thermal expansion coefficient between mounted substrates and IC leads may cause a failure like solder peeling or solder wet, and electrical characteristics may change by thermal stress.
Therefore, mounting should be done after sufficient confirmation for especially in case of ceramic substrates.

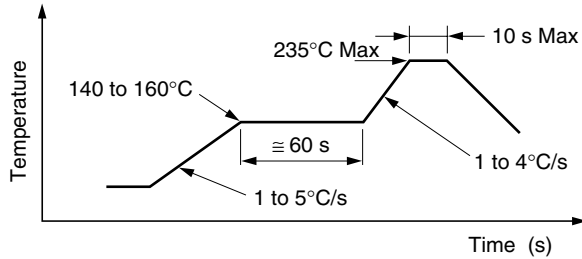
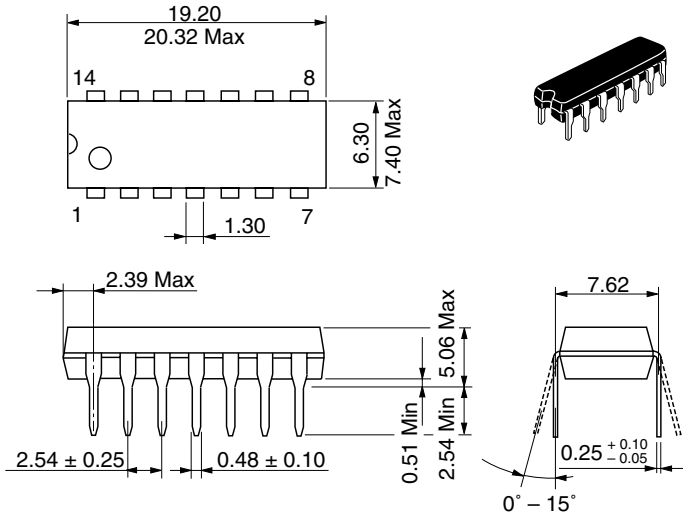


Figure 1 An Example of Infrared Rays Reflow Conditions

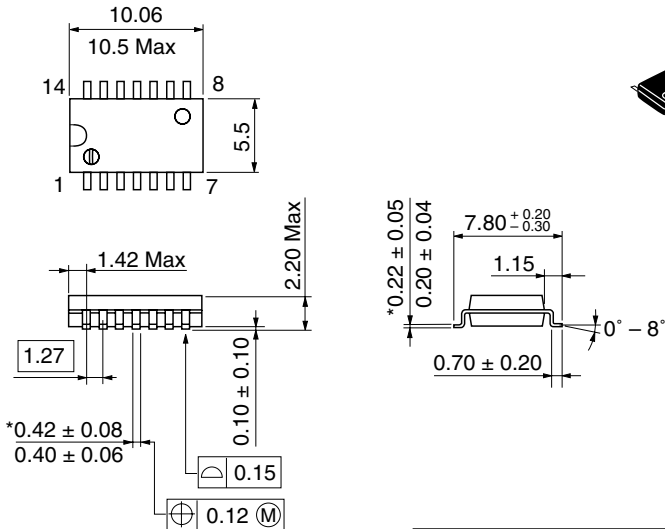
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

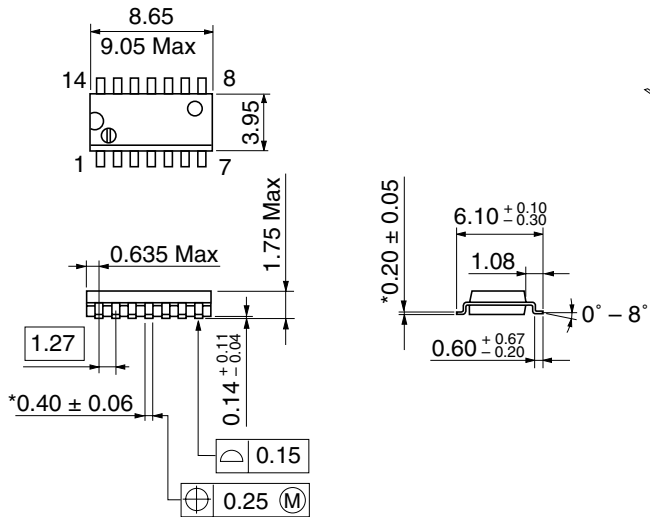
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

Unit: mm



*Pd plating

Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.13 g

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