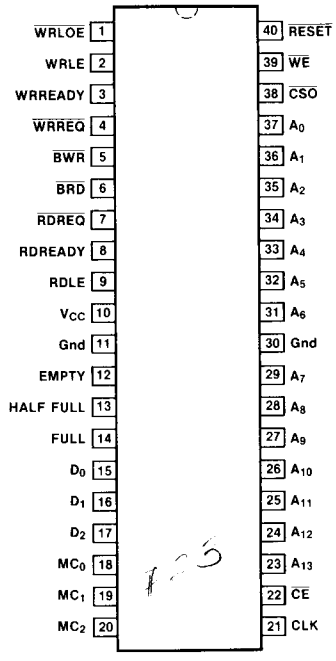
54F/74F411

FIFO RAM Controller

Description

The 'F411 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs. The 'F411 can control up to 16K words of buffer memory; intermediate buffer sizes can be selected (see device functional description). Built-in arbitration logic controls read/write operations on first-come/first-served basis.

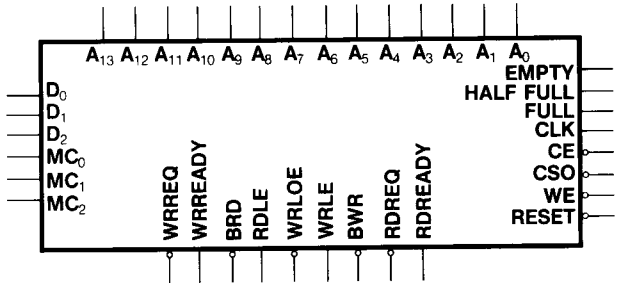
Connection Diagrams

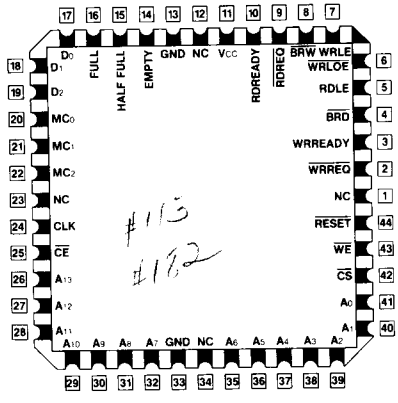


Pin Assignment for DIP

Ordering Code: See Section 5

Logic Symbol





Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_{13}	Read/Write Address	75/15 (12.5)
MC_0-MC_2	Memory Clock Select	0.5/0.375
D_0-D_2	FIFO Depth Select	0.5/0.375
EMPTY	Status Line	25/12.5
HALF FULL	Status Line	25/12.5
FULL	Status Line	25/12.5
$\overline{BRD}$, $\overline{BWR}$	Burst Read, Burst Write	0.5/0.375
WRLE, RDLE	Write Latch Enable, Read Latch Enable	25/12.5
$\overline{RDREQ}$	Read Request	0.5/0.375
$\overline{WRREQ}$	Write Request	0.5/0.375
$\overline{WE}$	RAM Write Enable	25/12.5
$\overline{CSO}$	RAM Chip Select Output	25.12.5
$\overline{RESET}$	Master Reset	0.5/0.375
CLK	Clock	0.5/0.375
$\overline{CE}$	Chip Enable	0.5/0.375
WRREADY	Write Ready	25/12.5
RDREADY	Read Ready	25/12.5
$\overline{WRLOE}$	Write Latch Output Enable	25/12.5

Functional Description

The 'F411 FIFO RAM Controller consists of three 14-bit counters. Two of these counters provide read/write addresses for FIFO read/write operations respectively. The third counter is an up-down counter. Depending on the operation of FIFO, the counter is either incremented (write operation) or decremented (read operation). The output of the counter is decoded according to the memory length select lines D_0-D_2 to produce EMPTY, HALF FULL, or FULL status lines. (See Table 2).

The arbitration logic handles all read/write requests on first-come/first-served basis. In the event of a tie, the priority is based on the HALF FULL status signal. Normally write requests have higher priority over read requests unless the HALF FULL signal is active, in which case the read requests have priority over write requests. The arbiter decision can be disabled by Burst Read or Burst Write request in which case all subsequent read or write requests are denied until burst read or write operation is terminated. The priority will be the same as normal read and write should Burst Write and Burst Read become active simultaneously. (See Table 3.)

The WRLE and RDLE signals control the external latches at the top and bottom of the FIFO stack. Read (RD) and Write (WR) pulses are used to transfer data to and from the RAM locations specified by the address bus. Read and Write pulse widths can be programmed using memory clock pins MC_0-MC_2, (See Table 1). RESET will reset all counters to zero. HALF FULL and FULL status lines are forced LOW and EMPTY status forced HIGH.

Functional Operation

A_0-A_{13}

Fourteen 3-state outputs are capable of driving an 8 mA DC load. The FIFO can address up to 16K words of data.

The three Memory Clock select lines determine the number of master clock cycles by which Write or Read pulse width is extended. See Table 1 for selection guide.

D_0-D_2

The length of the FIFO memory can be hardware-selected via the length select (D_0-D_2) inputs. When less than the maximum length is selected, the unused high-order bits of the address outputs are held in the high-impedance state.

Write Request ($\overline{WRREQ}$)

Write request for write cycle; active LOW input.

Read Request ($\overline{RDREQ}$)

Read request for read cycle; active LOW input.

Write Enable ($\overline{WE}$)

Write cycle address valid, active LOW 3-State output.

Chip Select Output ($\overline{CSO}$)

When active, the RAM will be selected. Active LOW, 3-State output.

RESET

Active LOW master reset input. The user must force the RESET input LOW to initialize the chip. The following actions occur when RESET is active:

1. All internal counters are set to '0'.
2. Half Full and Full outputs are forced LOW.
3. $\overline{WE}$, $\overline{CSO}$ and EMPTY outputs are forced HIGH.
4. WRREADY and RDREADY signals are forced HIGH and LOW respectively.
5. Write latch will be disabled and transparent.
6. Read latch will be disabled and transparent.
7. RAM write address selected.

Burst Read ($\overline{BRD}$)

Active LOW input; the following actions occur when $\overline{BRD}$ is active:

1. Write Ready is forced HIGH.
2. Priority is always given to read requests.

Burst Write ($\overline{BWR}$)

Active LOW input; the following actions occur when $\overline{BWR}$ is active:

1. Read Ready is forced HIGH.
2. Priority is always given to write requests.

Write Ready (WRREADY)

Active HIGH output; WRREADY HIGH signals that FIFO is ready to accept write requests. WRREADY goes LOW on the positive-going edge of Master Clock on a pending write request. The WRREADY will go from LOW-to-HIGH one clock cycle later if FULL signal is LOW.

Read Ready (RDREADY)

Active HIGH output; RDREADY HIGH signals that FIFO is ready to accept read requests. RDREADY goes LOW on the positive-going edge of Master Clock on a pending read request. The RDREADY will go from LOW-to-HIGH on the positive going edge of $\overline{CS}$ if EMPTY signal is LOW.

Clock (CLK)

Clock input to the FIFO (variable); typical clock = 50 MHz.

Chip Enable ($\overline{CE}$)

Active LOW input; when inactive all RAM interface signals are held in high impedance state and further read or write requests are denied. Read or Write cycles in progress when $\overline{CE}$ goes HIGH will finish before the chip is deactivated.

Read Latch Enable (RDLE)

Active HIGH output; on the HIGH-to-LOW transition of RDLE, FIFO data is latched into the external output data latch.

Note RDLE will remain HIGH for modes 0-3 of MC.

Write Latch Enable (WRLE)

Active HIGH output; on the HIGH-to-LOW transition of WRLE data to be written into the FIFO is latched into the external input data latch.

Write Latch Output Enable ($\overline{WRLOE}$)

Active LOW output; on the HIGH-to-LOW transition of WRLOE the output of external input data latch is enabled.

FULL

Memory Full status output. The FULL signal goes HIGH on the negative-going edge of Master Clock if WRREADY is LOW and all bits of status counter for selected length are equal to '1'. The FULL signal goes from HIGH-to-LOW on the negative-going edge of Master Clock if RDREADY is LOW.

Note: WRREADY will remain LOW so long as full signal is active.

HALF FULL

Memory Half Full status output. The HALF FULL operates in the same way as FULL signal except that it goes HIGH when status counter reaches a count of 127 ($D_2 = H$, $D_1 = H$, $D_0 = L$). The HALF FULL signal goes from HIGH-to-LOW on the negative-going edge of Master Clock if RDREADY is LOW.

EMPTY

Memory Empty Status Output. The EMPTY signal goes HIGH on the negative-going edge of Master Clock if status counter contains a value of '1' and RDREADY is LOW. The EMPTY signal goes from HIGH-to-LOW on the negative-going edge of Master Clock if WRREADY is LOW.

Note: RDREADY will remain LOW so long as EMPTY signal is valid.

Block Diagram

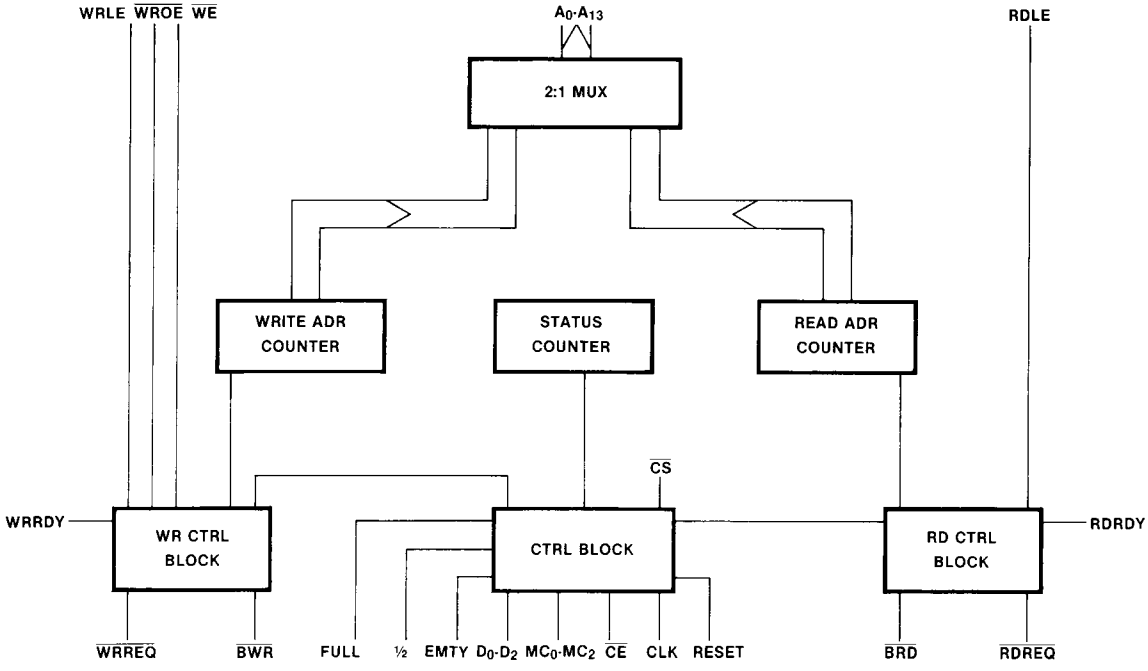


Table 1

MC_2	MC_1	MC_0	Mode	$\overline{WE}$ Duration	$\overline{CS}$ Duration
0	0	0	0	1	LOW*
0	0	1	1	2	LOW*
0	1	0	2	3	LOW*
0	1	1	3	4	LOW*
1	0	0	4	1	1
1	0	1	5	2	2
1	1	0	6	3	3
1	1	1	7	4	4

*Chip Select output remains LOW irrespective of MC_nsettings.

Table 2

D_2	D_1	D_0	Half Length Words	Full Length Words
0	0	0	8K	16K
0	0	1	4K	8K
0	1	0	2K	4K
0	1	1	1K	2K
1	0	0	512	1024
1	0	1	256	512
1	1	0	128	256
1	1	1	64	128

Table 3

$\overline{RDREQ}$	$\overline{WRREQ}$	$\overline{BWR}$	$\overline{BRD}$	Half Full	Priority
L	L	L	L	L	NOOP
L	L	L	L	H	NOOP
L	L	L	H	L	WRITE
L	L	L	H	H	WRITE
L	L	H	L	L	READ
L	L	H	L	H	READ
L	L	H	H	L	WRITE
L	L	H	H	H	READ
L	H	L	L	L	NOOP
L	H	L	L	H	NOOP
L	H	L	H	L	NOOP
L	H	L	H	H	NOOP
L	H	H	L	L	READ
L	H	H	L	H	READ
L	H	H	H	L	READ
L	H	H	H	H	READ
H	L	L	L	L	NOOP
H	L	L	L	H	NOOP
H	L	L	H	L	WRITE
H	L	L	H	H	WRITE
H	L	H	L	L	NOOP
H	L	H	L	H	NOOP
H	L	H	H	L	WRITE
H	L	H	H	H	WRITE
H	H	X	X	X	NOOP

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		125	190	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency Data Rate with 20 ns SRAM	50 25							MHz
t_{PHL}	Propagation Delay $\overline{CSO}$ to $\overline{WE}$			5.0					ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{WRREQ}$ to WRREADY			13.0 13.0					ns
t_{PLH} t_{PHL}	Propagation Delay WRREADY to WRLE			10.0 10.0					ns
t_{PLH} t_{PHL}	Propagation Delay WRREADY to $\overline{WRLOE}$			10.0 10.0					ns
t_{PLH} t_{PHL}	Propagation Delay Clock to WRREADY			6.0 6.0					ns
t_{PLH} t_{PHL}	Propagation Delay WRREADY to Status Output			20.0 20.0					ns
t_{PLH} t_{PHL}	Propagation Delay RDREADY to RDLE			25.0 25.0					ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW RAM Add	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW RAM Add	5.0 5.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{WRREQ}$	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{WRREQ}$	5.0 5.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{BWR}$	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{BWR}$	5.0 5.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{BRD}$	5.0 5.0			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{BRD}$	5.0 5.0			ns
$t_w(H)$ $t_w(L)$	$\overline{CSO}$ Pulse Width HIGH or LOW	20.0 20.0			ns

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Fig. 411-a Write Cycle

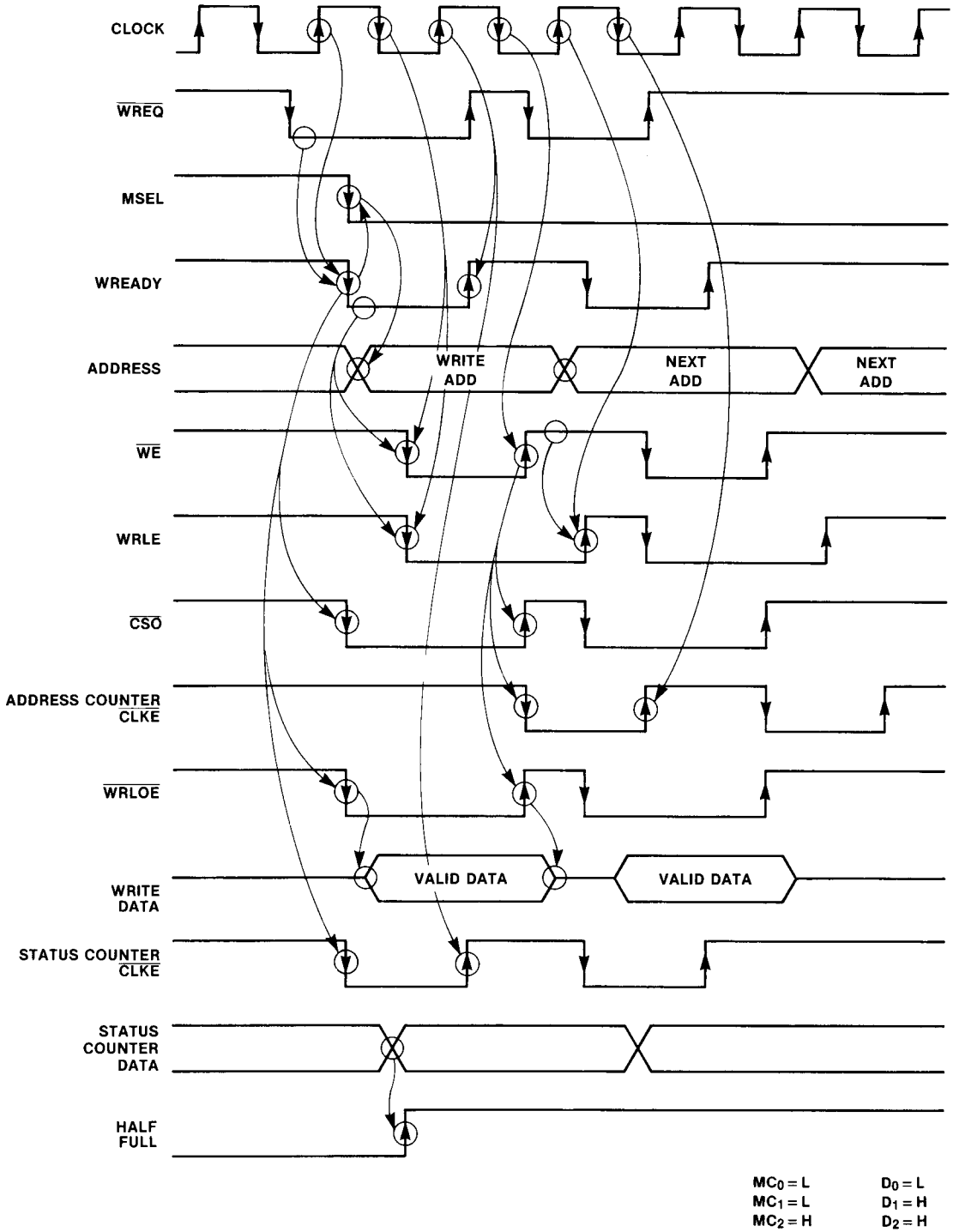

Fig. 411-b Read Cycle