MOTOROLA

MC74AC160
MC74ACT160
MC74AC162
MC74ACT162

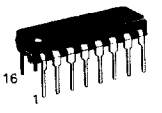
Product Preview

Synchronous Presettable BCD Decade Counter

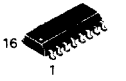
SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

The MC74AC160/74ACT160 and MC74AC162/74ACT162 are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74AC160/74ACT160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC162/74ACT162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz
- Outputs Source/Sink 24 mA
- 'ACT160 and 'ACT162 Have TTL Compatible Inputs

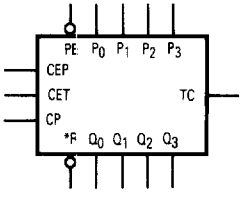


N SUFFIX
CASE 648-08
PLASTIC

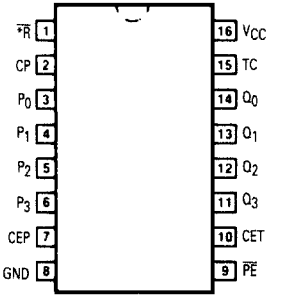


D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL



* $\overline{MR}$ for '160
* $\overline{SR}$ for '162



PIN NAMES

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ ('160)	Asynchronous Master Reset Input
$\overline{SR}$ ('162)	Synchronous Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

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FUNCTIONAL DESCRIPTION

The MC74AC160/74ACT160 and MC74AC162/74ACT162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('160), synchronous reset ('162), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, '160), Synchronous Reset ($\overline{SR}$, '162), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('160) or $\overline{SR}$ ('162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC160/74ACT160 and MC74AC162/74ACT162 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the MC74AC160/74ACT160 and MC74AC162/74ACT162 decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$

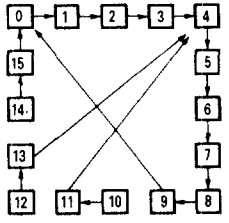
$TC = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot CET$

MODE SELECT TABLE

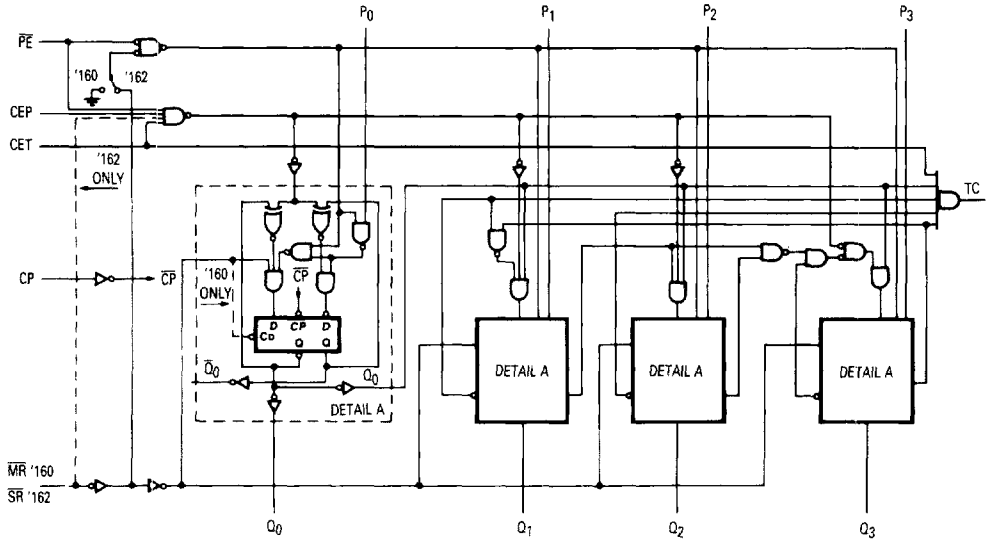
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge ($\int$)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For '162 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT160/162)	1.5	mA	V_{IN} = V_{CC} – 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		87 118				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.3 5.0		7.5 5.5				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.3 5.0		8.5 6.0				ns	3-6
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		11 8.0				ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0		7.5 5.5				ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0		8.5 6.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n ('AC160)	3.3 5.0		8.5 6.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('AC160)	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	3.3 3.3	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5			ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5			ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0			ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW ('AC160)	3.3 5.0	4.5 3.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP ('AC160)	3.3 5.0	0 0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0		118				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	5.0		5.5				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	5.0		6.0				ns	3-6
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	5.0		7.0				ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0		8.0				ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0		5.5				ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0		6.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n ('ACT160)	5.0		6.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('ACT160)	5.0		6.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP ('ACT162)	5.0	4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP ('ACT162)	5.0	−5.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{MR}$ to CP ('ACT160)	5.0	4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{MR}$ to CP ('ACT160)	5.0	−5.5			ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5			ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0			ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0			ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW ('ACT160)	5.0	3.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP ('ACT160)	5.0	0			ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

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