ADE-207-179 (Z)

HD153044TF

90-Mbps Single Chip Read Channel

HITACHI

1st. Edition
Sep. 1995

Description

The HD153044TF is fully integrated single-chip Data Channel LSI for high performance magnetic disk drives. Function block include the automatic gain control (AGC) circuit, pulse detector, electric programmable filter, 4-burst servo demodulator, write clock synthesizer, data synchronizer, and 1,7RLL ENDEC with programmable write precompensation circuit. This LSI achieves from 32 Mbit/s to 90 Mbit/s data rate, supports both single and multiple zone recording.

The HD153044TF is fabricated in HITACHI 0.7 µm Hi-Bi-CMOS process technology which achieves a high performance device with low power consumption. In powerdown mode, power consumption is 10 mW.

Features

General :

- 32 to 90 Mbit/s data transfer rate.
- A serial port for register access.
- User-selectable single zone recording or multiple zone recording options. The following are programmable for multiple zone recording : VCO center frequency, Read-PLL loop filter dumping factor, charge pump current levels (16 settings), active filter cut-off frequency for servo and data modes (128 settings).
- Power Management system
  (Servo = 400mW, Idle = 50mW, Sleep = 10mW)
- 2 bits parallel NRZ bus.
- Power consumption 680 mW typical.
- A single 5 V supply is required.
- This type 64 pin QFP package (1.2 mm height)

Read Pulse Detector & Servo Functions :

- Built-in AGC amplifier for stable operation in spite of varying media and head characteristics.
- AGC amplifier gain can be set to zero during writing.
- Fast AGC attack can be accomplished with RX function.
- AGC input's short time can be controlled by register. 0.25 ns typ. pulse pairing (sine wave input).
- 4-burst servo circuit (peak-hold) with buffer amp.
- Servo reference voltage output.
- Servo charge speed can be controlled by register.

Programmable Filter (AF) :

- Programmable cut-off frequency of 6 to 33 MHz.
- Cutoff frequency and boost level can be setting independently each servo and data mode.
- 7th order equiripple filter.
- ±10 % fc accuracy.
- ±3 % group delay variation. (0.2 fc to fc)

Write Clock Synthesizer :

- On-chip frequency synthesizer generates write clock.
- Independent M and N divide by registers.
- Unlock detect function.
- VCO center frequency matched to data synchronizer.
- VCO center frequency accuracy is less than ±5 %.

Synchronizer :

- High-speed acquisition can be accomplished with highly stable reproduction by switching between normal-gain and high-gain modes, and by switching loop filter constants.(6 bytes typ. acquisition time)
- Dual-mode phase detector compares both phase and frequency to ensure a wide capture range.
- VCO center frequency accuracy is less than ±5 %.

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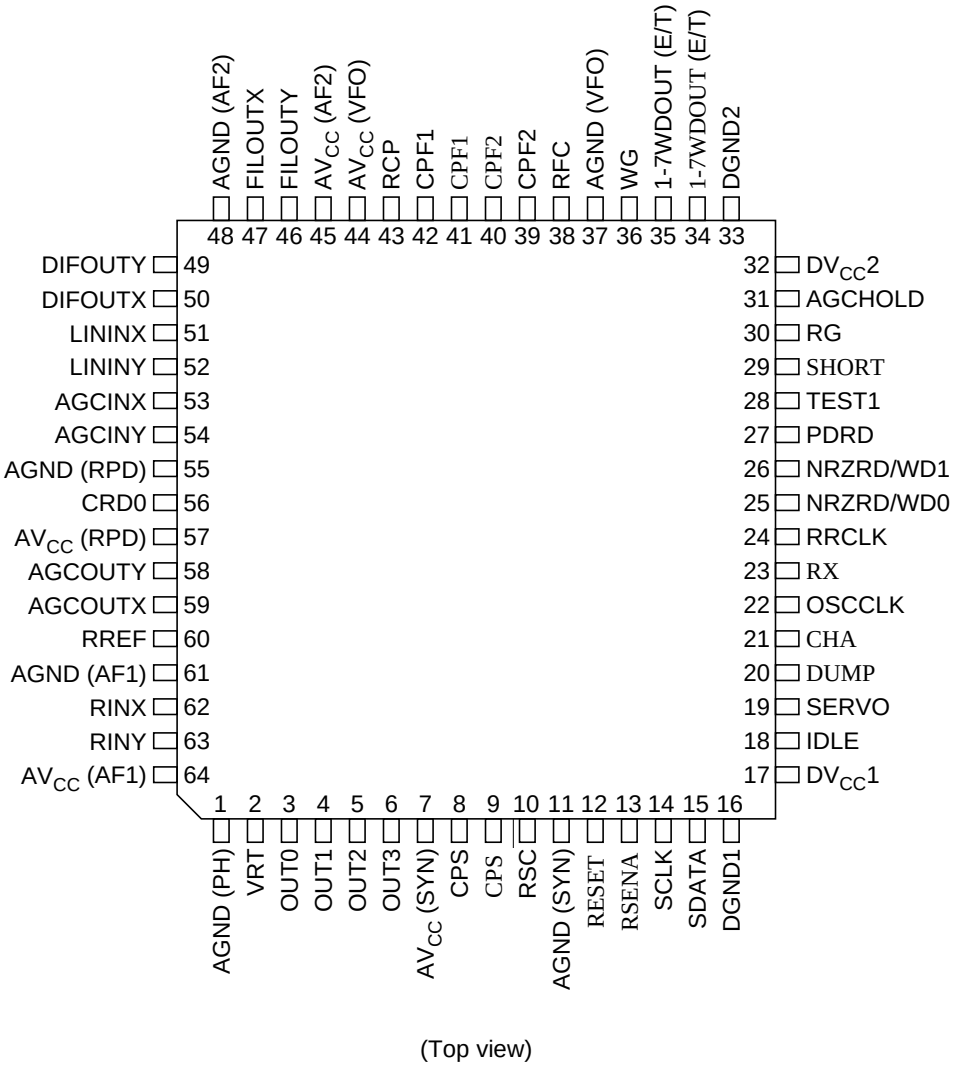
Data Separator :

- Window center accuracy is 0 ± halfwindow × 27 % ns.
- Programmable window shift control. (1.5 %/step)

Encoder/Decoder :

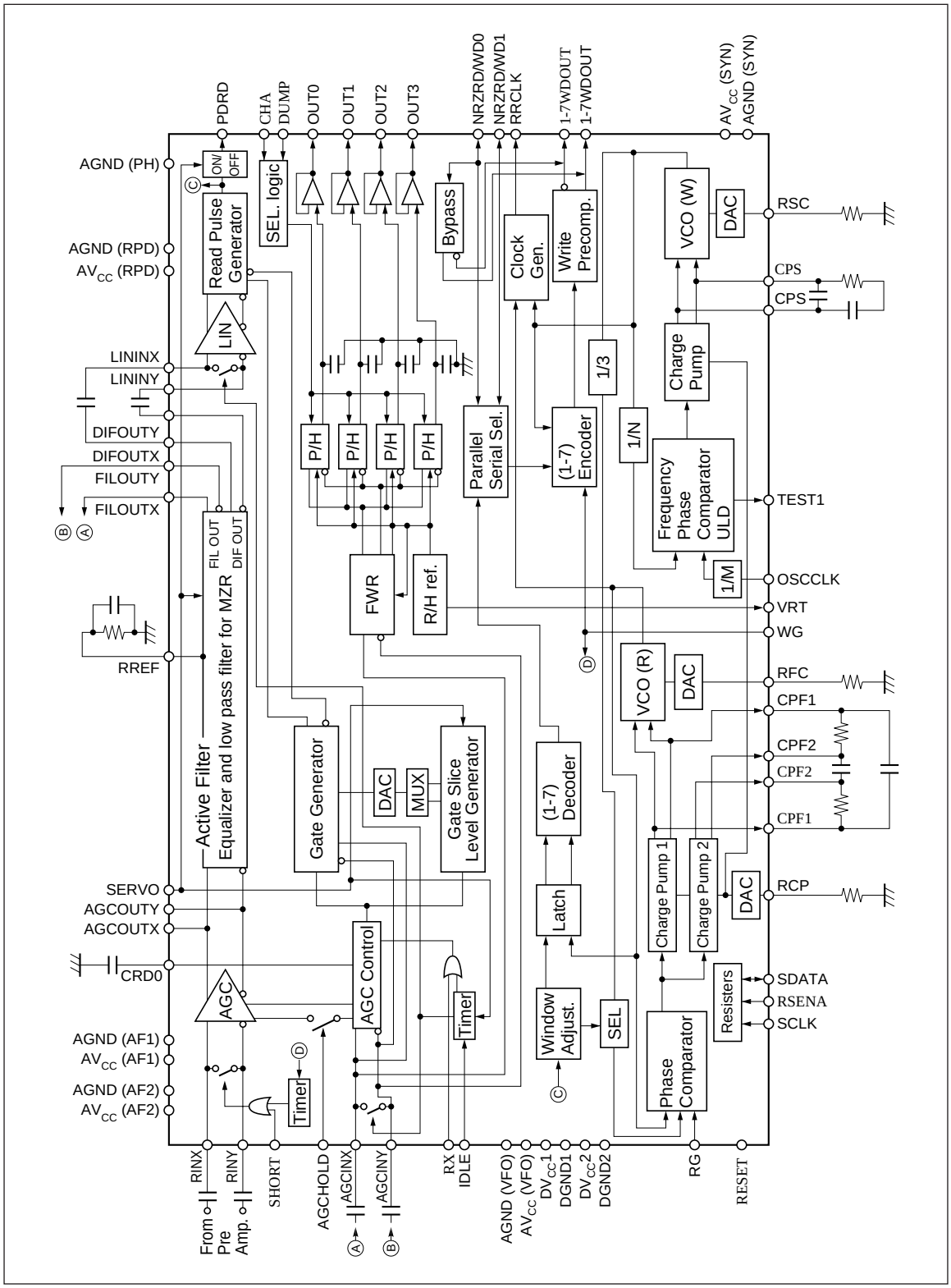
- IBM 1,7RLL code.
- 2 bits parallel NRZ bus.
- Bypass encoder function.
- 1,7 data to be written to disk can be programmed to be differential pseudo-ECL or TTL pair for high speed transfer without timing error.
- On chip write precompensation function with programmable delay line.

Pin Arrangement



(Top view)

Block Diagram



Pin Functions

Pin Name	Pin No.	Type	Function
RINX RINY	62 63	Differential input	Differential input lines for the read signal from the recording medium.
AGCOUTX AGCOUTY	59 58	Differential output	Differential output lines for monitor from the AGC amplifier. The outputs are open-emitter type and would need external 3.9 kΩ pull down resistors.
CRD0	56	External component required	The charge/discharge current output line for the AGC control circuit.
FILOUTX FILOUTY	47 46	Differential output	Differential output line from Active Filter. Connect to AGCINX, Y through bypass capacitors.
DILOUTX DILOUTY	50 49	Differential output	Differential output line from Active Filter. Connect to LININX, Y through bypass capacitors.
AGCINX AGCINY	53 54	Differential input	Differential input lines to the AGC output amplitude detector. Connect to FILOUTX/Y outputs of the Active Filter with bypass capacitors.
LININX LININY	51 52	Differential input	Differential input lines for the zero-crossing comparator. Normally connect to DIFOUTX/Y of the Active Filter with bypass capacitors.
RREF	60	External component required	Connect to a resistor to set the reference current for the Active Filter's DAC.
CPF1 CPF1 CPF2 CPF2	42 41 39 40	External component required	Current output to the external loop filter for read PLL.
RCP	43	External component required	Connect to a resistor to set the charge pump output current for the decode clock generator's VFO and write clock synthesizer. The charge pump current level is set by HCR [3:0], NCR[3:0], NCW[3:0] and NCS[3:0] registers.
RFC	38	External component required	Connect to a resistor to set the center frequency of the VCO in the decode clock generator's VFO. This pin must connect to 3.6 kΩ resistor.
RSC	10	External component required	Connect to a resistor to set the center frequency of the VCO in the encode clock generator's frequency synthesizer. This pin must connect to 3.6 kΩ resistor.
CPS CPS	8 9	External component required	Current output to an external loop filter for write clock synthesizer.
OSCCLK (Oscillator clock)	22	In (TTL)	Clock synthesizer's reference clock input. The frequency synthesizer generates encode clock frequencies from the input on this line. Data writing is synchronized with the encode clock. When not reading data, the decode clock generator's VFO is also synchronized to this frequency (1.5 times the data transfer rate).

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
TEST1 (ULD function output)	28	Out (TTL)	Error output from the encode clock generator's frequency synthesizer. TEST1 goes low to indicate that the PLL in the encode clock generator's frequency synthesizer has lost lock. The disk controller should immediately half the write operation. Data must be written again from the beginning.
SHORT	29	In (TTL)	When this terminal is "L", RINX and RINY are shorted together. This short timing can be generated both by the internal short pulse generate circuit or direct input by this pin.
RX	23	In (TTL)	TTL-level input that switches the AGC loop on or off. When RX signal turn Low to High, AGC gain starts from maximum gain. HD153044TF has internal automatic RX pulse generate circuit.
AGCHOLD	31	In (TTL)	TTL-level input that locks the AGC amplifier gain. When AGCHOLD goes High, the gain is locked at its immediately preceding value.
SERVO	19	In (TTL)	"H" : Servo mode, "L" : Read mode. In the servo mode, "CFCS" register set the A/F's cut-off frequency and VGLS/ VGHS register set the gate slice level. In the read mode, "CFCR" register set the A/F's cut-off frequency and VGLR/ VGHR register set the gate slice level.
OUT0, OUT1, OUT2, OUT3	3, 4, 5, 6	Analog outputs	Servo burst's peak and hold outputs. Connect to A/D converter. Holding capacitors resides inside the chip with buffered outputs.
VRT	2	Analog outputs	Servo reference voltage output.
CHA	21	In (TTL)	Input pin of the sampling control signal for Servo Peak/Hold circuit (TTL level). Position signal is sampled by CHA = "L".
DUMP	20	In (TTL)	Input pin of the discharge control signal of Servo Peak/Hold circuit (TTL level). DUMP = "L" is for discharge.
PDRD	27	Out (TTL)	Output line for the data read from disk as reshaped into digital data by the read pulse detector. When SERVO (pin19) goes high, PDRD outputs read data pulse. When SERVO goes low, PDRD is disable.
WG	36	In (TTL)	Write gate input signal. Set this pin high during writing.
RG (Read Gate)	30	In (TTL)	High level at this input selects read mode. This signal switches the clock for counters and internal circuits, and begins phase synchronization of the decode clock generator's VFO with the 1-7 decode data.

RX input	AGC loop
High	AGC loop closed
Low	AGC loop open

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
NRZRD/WD1	26	In/Out (TTL)	The parallel data I/O pin of NRZ signal.
NRZRD/WD0	25	In/Out (TTL)	The parallel data I/O pin of NRZ signal. When the bypass encoder mode, provide the 1-7 write into this pin. Write data will be directory output from 1-7WDOUT and 1-7WDOUT.
RRCLK	24	Out (TTL)	Read reference clock output (TTL level). At read time, this pin provides a clock which is synchronized with the converted NRZRD signal. This controller should read NRZRD by this clock. Other than read mode, reference clock is provided to disk controller.
1-7WDOUT 1-7WDOUT (Write data outputs)	35 34	Out (TTL/ECL)	1-7 RLL Write Data Differential Output. Pseudo ECL/TTL are available by bit 6 of register "$h05". When this bit is "H", these outputs are ECL. When this bit is "L", these outputs are TTL. These pin provide the 1-7 write data that goes to the Read/Write amplifier after the write pre-compensation. When WG goes high, 1-7WDOUT and 1-7WDOUT pin are output mode.
RESET	12	In (TTL)	Low input initializes internal logic circuits and registers. When input low level, registers are initialized default value.
RSENA	13	In (TTL)	This active low input selects the device and enables the serial port.
SCLK	14	In (TTL)	This is the serial clock sent in by the hard disk controller or other ASIC device. For either read or write transfer, a 16 clock burst is required for proper operation. Data is latched in during write or sent out during read at the rising edge of the SCLK.
SDATA	15	In/Out (TTL)	Data is transmitted in 16-bit packet MSB first. The first 2 bits is used to determine the read or write mode, the next 5 bits are for the register address, followed by 1 "Don't Care" bit, then the last 8 bits are for the Write or Read Data.
IDLE	18	In (TTL)	The input is used in combination with the two mode bits in the PCNT register to reduce power consumption in the Idle mode. When PCNT = 00, device is in the R/W normal mode, all circuits are ON. When PCNT = 11, device is in the Sleep mode, all circuits are OFF except the I/O and register. When PCNT = 10, then depending on the logic level of the IDLE pin; if it is High, then chip is in the Idle mode and all circuits are OFF except for the I/O, register, and the bias circuits; if it is low, then the device is in the Servo mode and the I/O, logic, bias circuits, AGC, Active Filter, Read Pulse Detector, and Servo circuit will be ON with only the RDVFO and the WR synthesizer being OFF.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
$DV_{CC}1$ $DV_{CC}2$	17 32	Power	Digital V_{CC} power supply.
DGND1 DGND2	16 33	Ground	Digital ground.
AV_{CC}(AF1) AV_{CC}(AF2)	64 45	Power	Analog V_{CC} power supplies for active filter.
AGND(AF1) AGND(AF2)	61 48	Ground	Analog ground for active filter.
AV_{CC}(RPD)	57	Power	Analog V_{CC} power supply for read pulse detector.
AGND(RPD)	55	Ground	Analog ground for read pulse detector.
AGND(P/H)	1	Ground	Analog ground for peak hold.
AV_{CC}(VFO)	44	Power	Analog V_{CC} power supply for synchronizer.
AGND(VFO)	37	Ground	Analog ground for synchronizer.
AV_{CC}(SYN)	7	Power	Analog V_{CC} power supply for synthesizer.
AGND(SYN)	11	Ground	Analog ground for synthesizer.

Registers

Address	Name	Abbreviation	Note
00h	Low pass filter cut-off frequency control register (Read Mode)	CFCR register	fc = 6 to 33 MHz
01h	Low pass filter cut-off frequency control register (Servo Mode)	CFCS register	fc = 6 to 33 MHz
02h	Reserve address		
03h	Low pass filter boost level control register (Read Mode)	BLCR register	0 to 10 dB
	Write precompensation delay control register (Value E)	WPE register	
04h	Low pass filter boost level control register (Servo Mode)	BLCS register	0 to 10 dB
	Write precompensation delay control register (Value E1)	WPE1 register	
05h	Write precompensation delay control register (Value L1)	WPL1 register	
	Write precompensation delay control register (Value L)	WPL register	
	1-7 write data output type control register	WDS register	Pseudo ECL or TTL
	1-7 write data 1/2 divide mode select register	DWD17 register	
06h	Write PLL charge pump gain control register	NCS register	
	Write precompensation delay control register (Value N)	WPN register	
	Bypass encoder mode select register	BPE register	
07h	Read PLL (Synchronizer) charge pump gain control register	HCR register	High gain Mode
	Read PLL (Synchronizer) damping factor gain control register	HDR register	High gain Mode
08h	Read PLL (Synchronizer) charge pump gain control register	NCR register	Normal gain Mode
	Read PLL (Synchronizer) damping factor gain control register	NDR register	Normal gain Mode
09h	Read PLL (Synchronizer) charge pump gain control register	NCW register	Write clock Ref. Mode
	Read PLL (Synchronizer) damping factor gain control register	NDW register	Write clock Ref. Mode
0Ah	Pre-Scaler of write clock synthesizer control register (Value M)	PSM register	
0Bh	Pre-Scaler of write clock synthesizer control register (Value N)	PSN register	
0Ch	VCO center frequency control register	VFC register	
	Unlock detect sensitivity control register	ULD register	
0Dh	Envelope / DC level slice control register	EVSL register	
	Servo circuit's charge rate control register	PHG register	×1.0, ×1.5, ×2.5
0Eh	Decode window adjustment register	WAJ register	
	PDRD non-hysteresis mode control register	NHYSMD register	
	PDRD pulse width control register	PW register	
0Fh	Half window delay adjustment register	WTS register	
	ECL output buffer internal load connect control register	ELS register	
	PDRD polarity control register	RDS0 register	
	PDRD composite / non-composite control register	RDS1 register	

Registers (cont)

Address	Name	Abbreviation	Note
10h	AGC loop amplitude setting register	AVP register	
	AGC super discharge time control register	SDT register	
11h	AGC amp. short timing control register	AGST register	
	AGC output enable register	AGCOE register	
	PDRD enable register	PDE register	
12h	Internal RX pulse gen. enable register	RXPE register	
	Internal RX pulse width control register	RXPA register	
	AGC Det. charge discharge ratio setting register	CDR register	
	AGC Det. charge discharge current control register	CDC register	
13h	Internal RX pulse width control register	RXPB register	
	Internal RX pulse width control register	RXPC register	
	Recovery register	REC register	
14h	Gate slice level setting register (Read Mode)	VGLR / VGHR register	
15h	Gate slice level setting register (Servo Mode)	VGLS / VGHS register	
16h	Negate counter setting register	RGN register	
	Sync. byte counter setting register	SYC register	
	Power management control register	PCNT register	
17h	Reserve address		
18h	AGC low slice level (VSL) ratio control register	SLV register	

Mode Control Register Map

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Resister Functions
0 0 0 0 0	" 0"	CFCR6*	CFCR5	CFCR4	CFCR3	CFCR2	CFCR1*	CFCR0*	CFCR: Active frequency cut-off for read mode
0 0 0 0 1	POLO	CFCS6	CFCS5	CFCS4	CFCS3*	CFCS2*	CFCS1	CFCS0	CFCS: Active frequency cut-off for servo mode POLO: Polarity signal output control
0 0 0 1 0	" 0"	" 0"	" 0"	" 0"	" 0"	" 0"	" 0"	" 0"	Reserve address
0 0 0 1 1	WPE2	WPE1	WPE0	BLCR4	BLCR3	BLCR2	BLCR1	BLCR0	BLCR: Active boost level for read mode WPE: Write precomp. delay (E)
0 0 1 0 0	WPE12	WPE11	WPE10	BLCS4	BLCS3	BLCS2	BLCS1	BLCS0	BLCS: Active boost level for servo mode WPE1: Write precomp. delay (E1)
0 0 1 0 1	DWD17	WDS	WPL2	WPL1	WPL0	WPL12	WPL11	WPL10	WPL1: Write precomp. delay (L1) WPL: Write precomp. delay (L) WDS: 17WD PECL/ TTL sel. DWD17: 17WD divide mode sel.
0 0 1 1 0	BPE	WPN2	WPN1	WPN0	NCS3	NCS2	NCS1	NCS0	NCS: Write charge pump current WPN: Write precomp. delay (N) BPE: Bypass encoder sel.
0 0 1 1 1	HDR3	HDR2	HDR1	HDR0	HCR3	HCR2	HCR1	HCR0	HCR: High pump current for read mode HDR: High gain PLL's damping factor for read mode
0 1 0 0 0	NDR3	NDR2	NDR1	NDR0	NCR3	NCR2	NCR1	NCR0	NCR: Normal pump current for read mode NDR: Normal gain PLL's damping

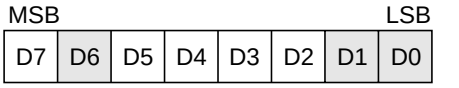
									factor for read mode
0 1 0 0 1	NDW3	NDW2	NDW1	NDW0	NCW3	NCW2	NCW1	NCW0	NCW: Normal charge pump gain current for Ref. mode NDW: Normal gain PLL's damping factor for Ref. mode
0 1 0 1 0	PSM7	PSM6	PSM5	PSM4	PSM3	PSM2	PSM1	PSM0	PSM: Write clock synthesizer's M divide value
0 1 0 1 1	PSN7	PSN6	PSN5	PSN4	PSN3	PSN2	PSN1	PSN0	PSN: Write clock synthesizer's N divide value
0 1 1 0 0	ULD1	ULD0	VFC5*	VFC4	VFC3	VFC2	VFC1	VFC0	VFC: Read and write PLL center frequency ULD: Unlock detector sensitivity
0 1 1 0 1	EVSL	" 0"	" 0"	" 0"	" 0"	" 0"	PHG1	PHG0	PHG: P / H sampling gain control level EVSL: Envelope / DC slice control
0 1 1 1 0	PW	NHYSMD		WAJ5	WAJ4*	WAJ3	WAJ2*	WAJ1	WAJ0 WAJ: Decode window adjustment NHYSMD: PDRD non hysteresis mode PW: PDRD pulse width

Note: * These bits are set "1" when register will be reseted.

Register Descriptions

Read Mode AF Cut-Off Frequency Register (CFCR)

Address : $00 (at write="C0" hex, at read="80" hex)



CFCR register

Select the cut-off frequency for the active filter in the normal data read mode. (when SERVO = "L")

CFCR [6:0]

0 0 0 1 1 0 0 Minimum (≈ 6MHz)

•

•

•

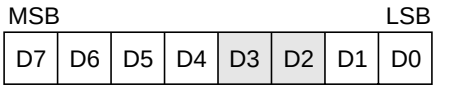
294 kHz/step

1 1 0 1 0 0 0 Maximum (≈ 33MHz)

Unused bit, must be "0" when written.

Servo Mode AF Cut-Off Frequency Register (CFCS)

Address : $01 (at write="C2" hex, at read="82" hex)



CFCS register

Select the cut-off frequency for the active filter in the Servo mode. (when SERVO = "H")

CFCS [6:0]

0 0 0 1 1 0 0 Minimum (≈ 6MHz)

•

•

294 kHz/step

1 1 0 1 0 0 0 Maximum (≈ 33MHz)

POLO register

POLO

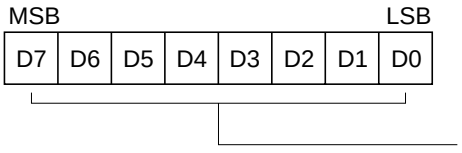
POLO = "0" : TEST1 is ULD signal output mode
POLO = "1" : TEST1 is POL signal output mode

POLO is the polarity signal for read signal from disk drive.

POL and PDRD output mode control				Output signal	
PDE	WG	SERVO	RG	TEST1(POLO=1)	PDRD
0	0	0	0	0	Z
0	0	0	1	POL	Z
0	0	1	*	POL	PDRD
0	1	0	*	0	Z
0	1	1	*	0	0 or 1
1	0	0	0	0	0 or 1
1	0	0	1	POL	PDRD
1	0	1	*	POL	PDRD
1	1	*	*	0	0 or 1

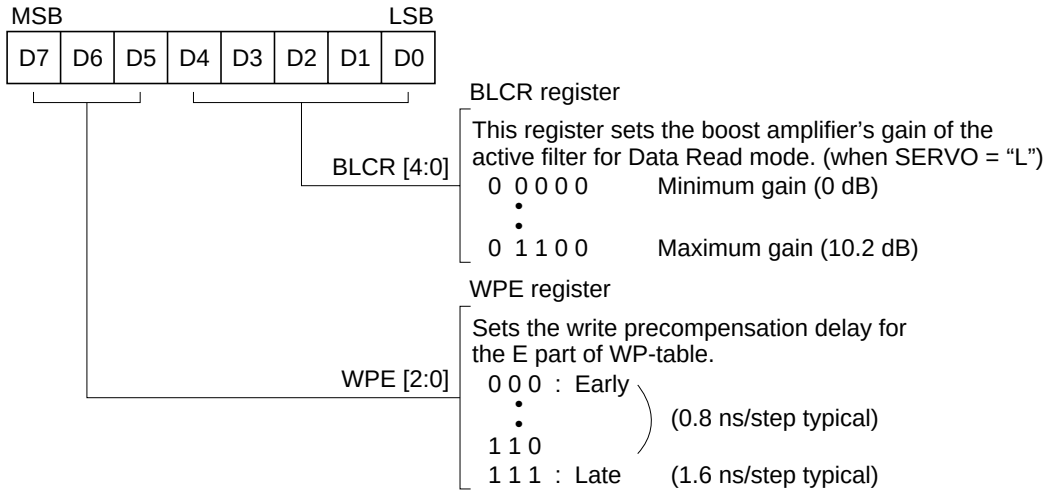
* : don't care Z : high impedance

Address : $02 (at write="C4" hex, at read="84" hex)



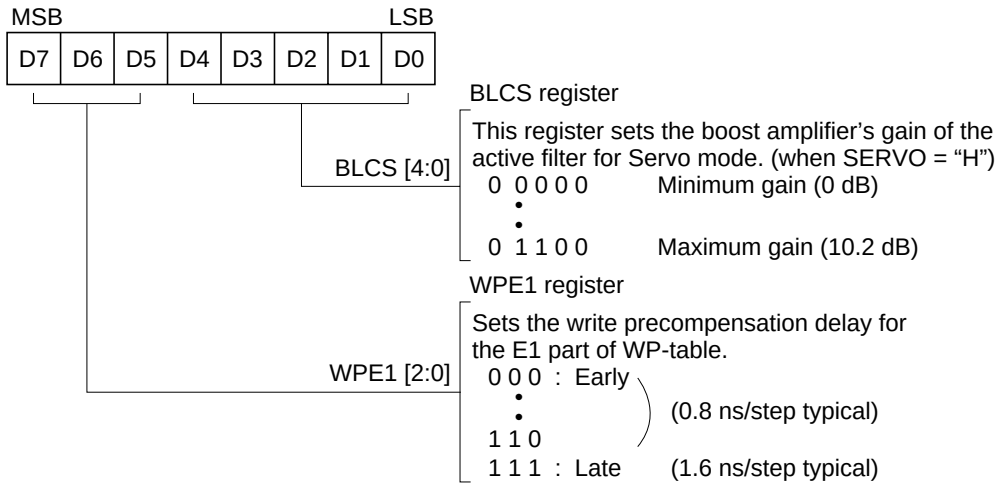
Read Mode AF Boost Level Control Register (BLCR)
Write Precompensation Delay Control Register (WPE)

Address : $03 (at write="C6" hex, at read="86" hex)



Servo Mode AF Boost Level Control Register (BLCS)
Write Precompensation Delay Control Register (WPE1)

Address : $04 (at write="C8" hex, at read="88" hex)



Write Precompensation Delay Control Register (WPL1)
Write Precompensation Delay Control Register (WPL)
1-7Write Data Output Type Select Register (WDS)
1-7Write Data Divide Mode Select Register (DWD17)

Address : $05 (at write="CA" hex, at read="8A" hex)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

WPL1 register

Sets the write precompensation delay for the L1 part of WP-table.

WPL1 [2:0]

0 0 0 : Early
•
•
1 1 0 (0.8 ns/step typical)
1 1 1 : Late (1.6 ns/step typical)

WPL register

Sets the write precompensation delay for the L part of WP-table.

WPL [2:0]

0 0 0 : Early
•
•
1 1 0 (0.8 ns/step typical)
1 1 1 : Late (1.6 ns/step typical)

WDS register

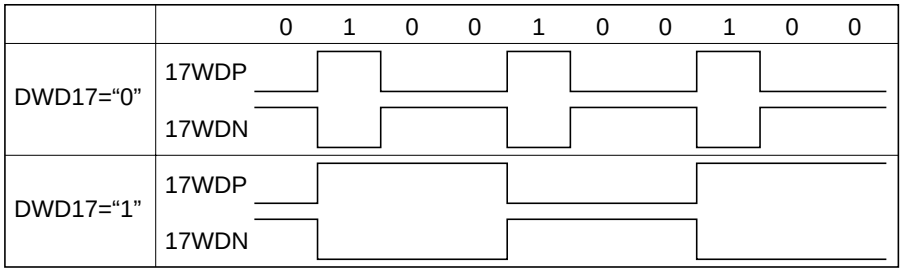
WDS

When WDS="0" : TTL output mode
When WDS="1" : pseudo ECL output mode

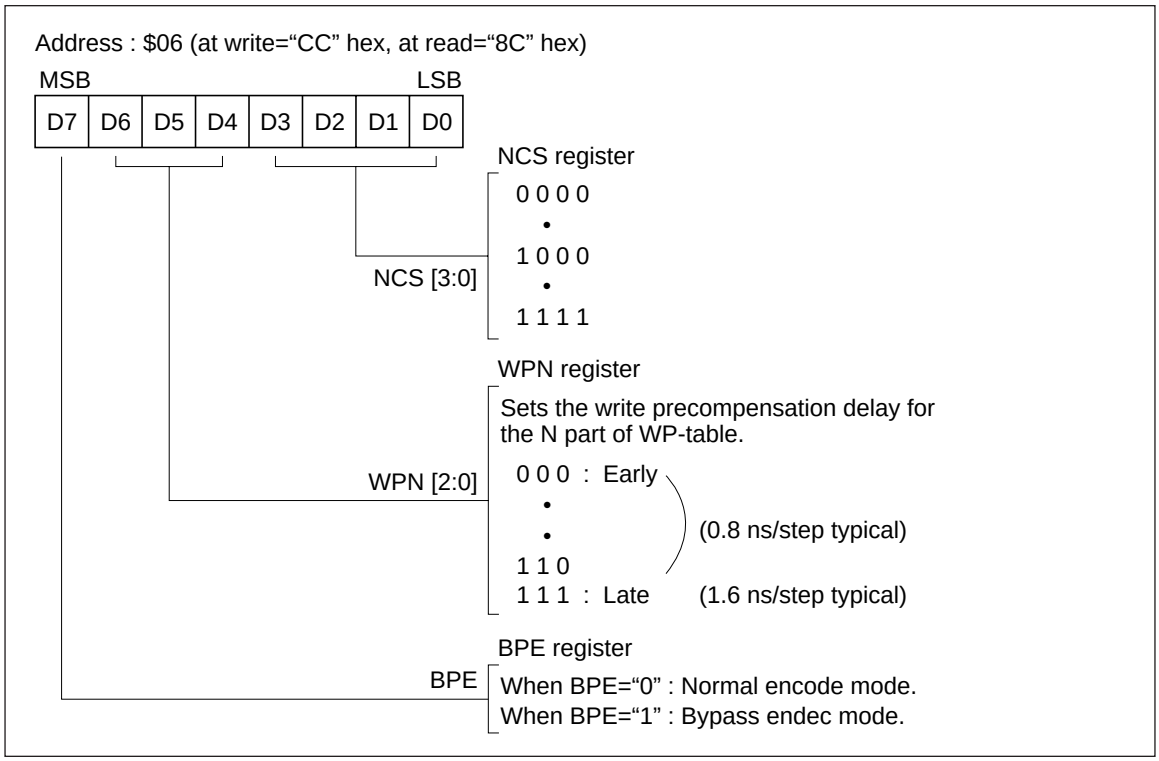
DWD17 register

DWD17

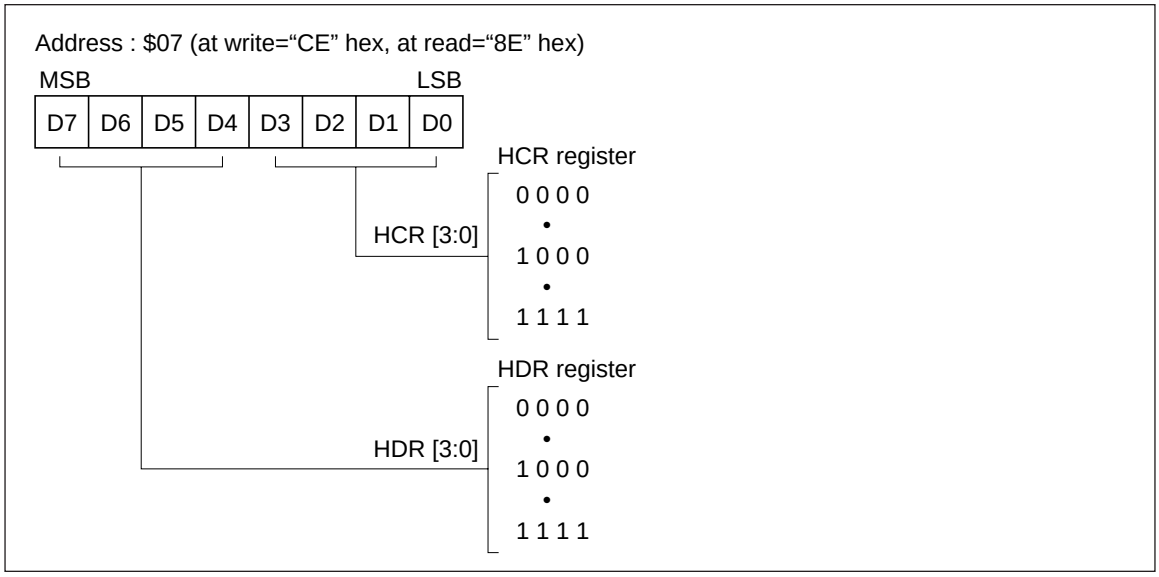
When DWD17="0" : 1-7 write data will not be divided.
When DWD17="1" : 1-7 write data will be divided.



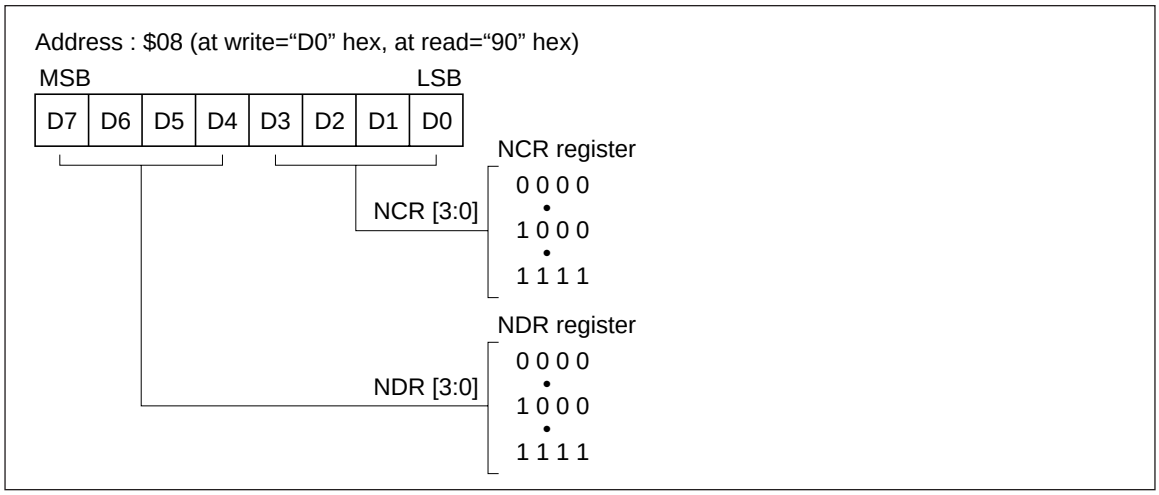
Write Synthesizer's Charge Pump Output Current Control Register (NCS)
Write Precompensation Delay Control Register (WPN)
Bypass Encoder Mode Select Register (BPE)



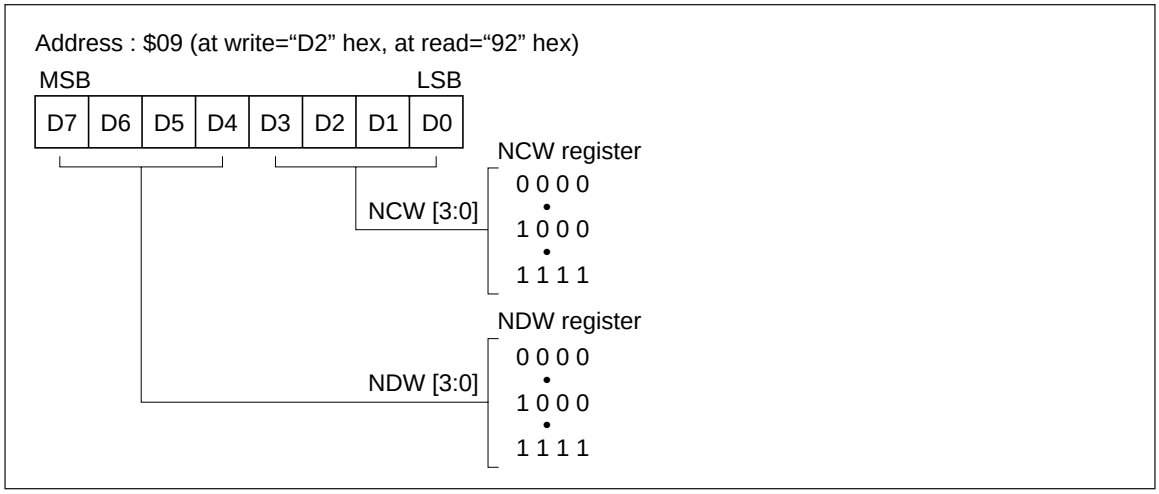
Read PLL's Charge Pump Output Current Control Register for High Gain Mode (HCR)
Read PLL's Damping Factor Control Register for High Gain Mode (HDR)



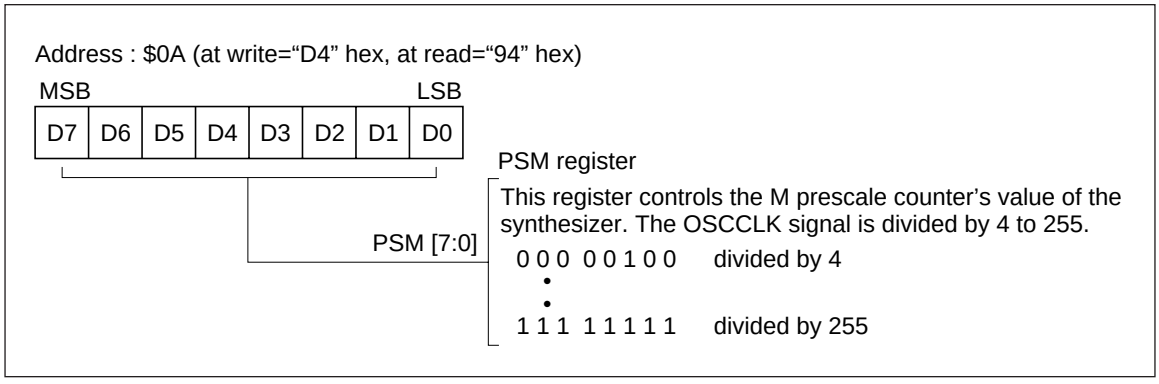
Read PLL's Charge Pump Output Current Control Register for Normal Gain Mode (NCR)
Read PLL's Damping Factor Control Register for Normal Gain Mode (NDR)



Read PLL's Charge Pump Output Current Control Register for Write Clock Reference Mode (NCW)
Read PLL's Damping Factor Control Register for Write Clock Reference Mode (NDW)

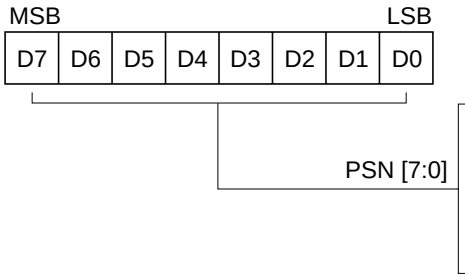


Prescaler of the Synthesizer Control Register (PSM) [M value]



Prescaler of the Synthesizer Control Register (PSN) [N value]

Address : $0B (at write="D6" hex, at read="96" hex)



PSN register

This register controls the N divide counter's value of the synthesizer. The VCO clock signal is divided by 4 to 255.

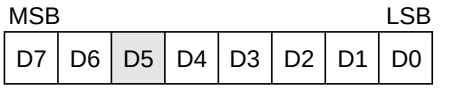
0 0 0 0 0 1 0 0 divided by 4

•
•

1 1 1 1 1 1 1 1 divided by 255

VCO Center Frequency Control Register (VFC)
Unlock Detector Sensitivity Control Register (ULD)

Address : $0C (at write="D8" hex, at read="98" hex)



VFC register

This register is used in multiple-zone recording to set the center frequency of the decode clock generator's VCO and the oscillation frequency of the decode clock generator's frequency synthesizer. Bit D5 is set "1" when reset pin is asserted.

VFC [5:0]

Resistors connected to the RFC and RSC lines set these values for the maximum data transfer rate. The VFC register decrease these values in step of 1.59%, permitting 42 settings down to a minimum transfer rate 0.35 times of the maximum rate.

0 1 0 1 1 0 Minimum transfer rate

•
•
•

1 1 1 1 1 1 1 Maximum transfer rate

ULD register

Select the unlocked detect gain for the synthesizer to activate the TEST1 output when unlock condition occurs.

ULD [1:0]

0 0 : 2 OSCCLK
0 1 : 4 OSCCLK
1 0 : 6 OSCCLK
1 1 : 8 OSCCLK

Servo Circuits Control Register (PHG), Envelope Control Register (EVSL)

Address : $0D (at write="DA" hex, at read="9A" hex)

MSB							LSB
0	0	0	0	0	0	D1	D0

PHG register

This register controls the charge rate of the peak and hold circuit in the servo circuit.

PHG [1:0]

- 0 0 ×2.5 charge rate (0.8µs at Typ. condition)
- 0 1 ×1.5 charge rate (1.5µs at Typ. condition)
- 1 0 ×1.0 charge rate (2.0µs at Typ. condition)

Unused bits, must be "0" when written.

EVSL register

EVSL

EVSL="0" : DC slice level setting mode for gate slice level. (read and servo mode)

EVSL="1" : Envelope slice mode for gate slice level. (read mode)
DC slice level mode for gate slice level. (servo mode)

Decode Window Adjustment Register (WAJ), PDRD Non-Hysteresis Mode Control Register (NHYSMD) PDRD Pulse Width Control Register (PW)

Address : $0E (at write="DC" hex, at read="9C" hex)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

WAJ register

This register adjusts the setting of the window. Window centering can be adjusted to 41 positions by on-chip delay.

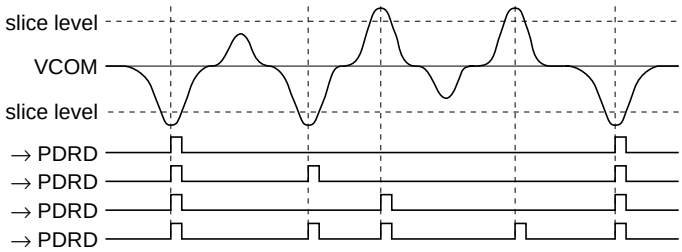
WAJ [5:0]

- 0 0 0 0 0 0 : (–) negative 50% adjustment
- •
- 0 1 0 1 0 0 : Center (Typ.)
- •
- 1 0 1 0 0 0 : (–) positive 50% adjustment

NHYSMD register

NHYSMD

NHYSMD="0" PDRD hysteresis mode
NHYSMD="1" PDRD non-hysteresis mode



NHYSMD	RDS1
0	0
1	0
0	1
1	1

(when RDS0=0)

PW register

PW

PDRD(Pin 27) pulse width control register

- 0 : 11.0ns typ.
- 1 : 6.0ns typ.

Half Window Delay Adjustment Register (WTS),
ECL Output Buffer Internal Load Connect Control Register (ELS)
PDRD Signal Polarity Select Register (RDS0), PDRD Composite Polarity Register (RDS1)

Address : $0F (at write="DE" hex, at read="9E" hex)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

WTS register

This register selects the step's value of the half window delay. Normally this register will be set according to the following.

WTS [4:0]

Data Rate	WTS Register	N_{WTS}
90 to 75 Mbps	0 0 0 1 1	3
75 to 60 Mbps	0 0 1 0 0	4
60 to 50 Mbps	0 0 1 0 1	5
50 to 42 Mbps	0 0 1 1 0	6
42 to 32 Mbps	0 0 1 1 1	7

ELS register

ELS

When 1-7WDOUT, 1-7WDOUT are ECL output mode (when WDS="1"), the following is valid.

"0" : ECL output buffer internal load non-connect mode

"1" : ECL output buffer internal load connect mode (pull-down current 10mA)

RDS register

RDS [1:0]

RDS0 selects PDRD signal polarity

"0" : Signal value "1" = "H" (active high)

"1" : Signal value "1" = "L" (active low)

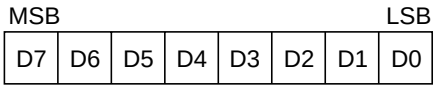
RDS1 composite polarity signal

"0" : Non-composite (one side polarity output)

"1" : Composite (both polarity output)

AGC Super Discharge Time Control Register (SDT)
AGC Loop's Amplitude Control Register (AVP)

Address : $10 (at write="E0" hex, at read="A0" hex)



SDT register

This register controls the period of the super discharge function on AGC control circuits. When SDT register will be selected, AGC control circuits will operate on constant discharge current. (see Figure 1)

SDT [3:0]

0 0 0 0 : 0 count (N_{SDT} = 0)
0 0 0 1 : 16 counts (N_{SDT} = 16)
0 0 1 0 : 24 counts (N_{SDT} = 24)
0 0 1 1 : 32 counts (N_{SDT} = 32)
•
•
• : 8 counts / SDT register bit
1 1 1 1 : 128 counts (N_{SDT} = 128)

AVP register

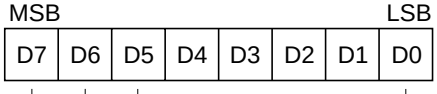
This register sets the amplitude of the AGC loop's output. The amplitude is FILOUT pin's differential voltage (Vppdiff).

AVP [3:0]

0 0 0 0 : 0.45 Vppdiff
•
•
• : 0.05 Vpp / AVP register bit
•
1 1 1 1 : 1.2 Vppdiff

AGC Amp. Short Time Control Register (AGST), AGCOUT Enable Register (AGCOE)
PDRD Output Enable Control Bit (PDE)

Address : $11 (at write="E2" hex, at read="A2" hex)



AGST register

This register controls the internal short timing generator. The input stage of the AGC amp.(RINX/Y) will be shorted when this register will be selected. The shorted period will be according to this register's value. When the NAGST = 0, internal short timer is disenable and only SHORT (Pin 29) is valid. SHORT pin and internal short gen. are connected OR logic.

AGST [5:0]

0 0 0 0 0 0 : 0 count (N_{AGST} = 0)
0 0 0 0 0 1 : 3 counts (N_{AGST} = 3)
0 0 0 0 1 0 : 4 counts (N_{AGST} = 4)
•
1 0 0 0 0 0 : 34 counts (N_{AGST} = 34)
•
1 1 1 1 1 1 : 65 counts (N_{AGST} = 65)
(see Figure 2)

AGCOE register

AGCOE

AGCOE = "0" AGCOUTX/Y (Pin 59, 58) are disenable
AGCOE = "1" AGCOUTX/Y (Pin 59, 58) are enable

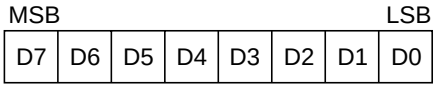
PDE register

PDE

When this bit sets "1", PDRD output is enable

Internal RX Pulse Ganerator Enable Register (RXPE),
Internal RX Pulse Width Control Register A (RXPA)
AGC Control Circuit's Charge & Discharge Current Ratio Setting Register (CDR)
AGC Control Circuit's Charge & Discharge Current Setting Register (CDC)

Address : $12 (at write="E4" hex, at read="A4" hex)



RXPE register

This register controls the internal RX pulse generator. RX (Pin 23) pin and internal RX pulse gen. are connected OR logic.

RXPE [2:0]

- 0 0 0 : External RX pin mode.
- 0 0 1 : Internal RX pulse generate mode. RX pulse is generated from falling edge of SERVO (Pin 19) signal. Pulse width is determined RXPA register.
- 0 1 0 : Internal RX pulse generate mode. RX pulse is generated from rising edge of SERVO (Pin 19) signal. Pulse width is determined RXPB register.
- 0 1 1 : Internal RX pulse generate mode. RX pulse is generated from both rising & falling edge of SERVO (Pin 19) signal. Pulse width are determined RXPA and RXPB register.
- 1 0 0 : Internal RX pulse generate mode. Pulse width is determined RXPC register. (see Figure 3)

RXPA register

This register sets the internal RX pulse width what is generated by RX pulse generator.

RXPA [2:0]

- 0 0 0 : 0 count (N_{RXPA} = 0)
- 0 0 1 : 5 counts (N_{RXPA} = 5)
- 0 1 0 : 7 counts (N_{RXPA} = 7)
- • : 2 counts / RXPA register bit
- 1 1 1 : 17 counts (N_{RXPA} = 17) (see Figure 3)

CDR register

CDR

- "0" : Charge : Discharge = 5 : 1
- "1" : Charge : Discharge = 20 : 1

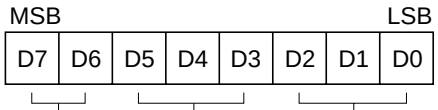
CDC register

CDC

- "0" : Charge current is 500μA
- "1" : Charge current is 250μA

Internal RX Pulse Width Control Register B (RXPB),
Internal RX Pulse Width Control Register C (RXPC)

Address : $13 (at write="E6" hex, at read="A6" hex)



RXPB register

This register sets the internal RX pulse width what is generated by RX pulse generator. (see Figure 3)

RXPB [2:0]

0 0 0 : 0 count (N_{RXPB} = 0)
0 0 1 : 5 counts (N_{RXPB} = 5)
0 1 0 : 7 counts (N_{RXPB} = 7)
•
• : 2 counts / RXPB register bit
•
1 1 1 : 17 counts (N_{RXPB} = 17)

RXPC register

This register sets the internal RX pulse width what is generated by RX pulse generator. (see Figure 3)

RXPC [2:0]

0 0 0 : 0 count (N_{RXPC} = 0)
0 0 1 : 5 counts (N_{RXPC} = 5)
0 1 0 : 7 counts (N_{RXPC} = 7)
•
• : 2 counts / RXPC register bit
•
1 1 1 : 17 counts (N_{RXPC} = 17)

REC register

This register sets the internal RX pulse width what is generated by RX pulse generator. (see Figure 3)

REC [1:0]

	recovery from idle	recovery from sleep
0 0	62 counts (N_{REC} = 62)	126 counts (N_{REC} = 126)
0 1	94 counts (N_{REC} = 94)	126 counts (N_{REC} = 126)
1 0	126 counts (N_{REC} = 126)	126 counts (N_{REC} = 126)
1 1	0 count (N_{REC} = 0)	0 count (N_{REC} = 0)

Low Gate Slice Level Register for Read Mode (VGLR)
High Gate Slice Level Register for Read Mode (VGHR)

Address : $14 (at write="E8" hex, at read="A8" hex)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

VGLR register

These are input to the internal DAC using VCOM as reference source to generate the low-slice level for the pulse detection circuit in the read mode. (when SERVO = "L")

VGLR [3:0]

		EVSL="1"	EVSL="0"
0 0 0 0	Minimum low-slice level	8% of V-peak	0.04V
•		•	•
•		•	•
1 1 1 1	Maximum low-slice level	71% of V-peak	0.36V

VGHR register

These are input to the internal DAC using VCOM as reference source to generate the high-slice level for the pulse detection circuit in the read mode. (when SERVO = "L")

VGHR [3:0]

		EVSL="1"	EVSL="0"
0 0 0 0	Minimum high-slice level	29% of V-peak	0.15V
•		•	•
•		•	•
1 1 1 1	Maximum high-slice level	92% of V-peak	0.46V

Low Gate Slice Level Register for Servo Mode (VGLS)
High Gate Slice Level Register for Servo Mode (VGHS)

Address : $15 (at write="EA" hex, at read="AA" hex)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

VGLS register

These are input to the internal DAC using VCOM as reference source to generate the low-slice level for the pulse detection circuit in the servo mode. (when SERVO = "H")

VGLS [3:0]

0 0 0 0 Minimum low-slice level 0.04V
•
•
1 1 1 1 Maximum low-slice level 0.36V

VGHS register

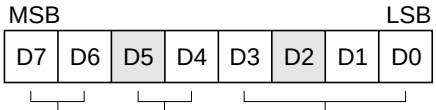
These are input to the internal DAC using VCOM as reference source to generate the high-slice level for the pulse detection circuit in the servo mode. (when SERVO = "H")

VGHS [3:0]

0 0 0 0 Minimum high-slice level 0.15V
•
•
1 1 1 1 Maximum high-slice level 0.46V

Negate Counter Setting Register (RGN), Sync. Control Register (SYC), Power Control Register (PCNT)

Address : $16 (at write="EC" hex, at read="AC" hex)



RGN register

This register sets the negate period of the refference data on read phase comparator. If t_{RGL} (period of RG="L") ≤ t_{RGN}, refference data of read phase comparator will not be switched from read data to 1/3 write clock.

RGN [3:0]

0 0 0 0 : 12 W-VCO counts (t_{RGN} = 1 byte)
0 0 0 1 : 24 W-VCO counts (t_{RGN} = 2 bytes)
0 0 1 0 : 36 W-VCO counts (t_{RGN} = 3 bytes)
0 0 1 1 : 48 W-VCO counts (t_{RGN} = 4 bytes)
0 1 0 0 : 60 W-VCO counts (t_{RGN} = 5 bytes)
•
1 0 0 1 : 120 W-VCO counts (t_{RGN} = 10 bytes)
1 0 1 0
•
1 1 1 1
These value must not write.

SYC register

This SYC register controls the high gain period of sync. counter.

SYC [1:0]

1 0 6 bytes
1 1 8 bytes

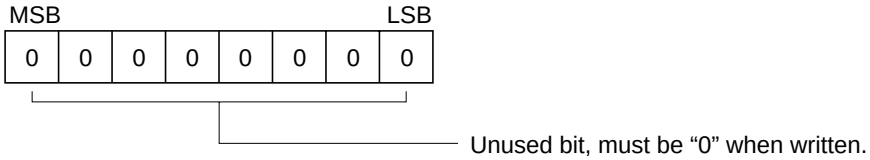
PCNT register

PCNT [1:0]

0 0 : Normal mode. All circuitries are powered.
1 0 : Power save mode. In this mode, IDLE pin will valid which of the two power save modes to be used. If IDLE = 1 then idle mode is selected and all modules will be powered down expect for the I/O, logic, and the bias circuitries. If IDLE = 0 then Servo mode will be selected and all blocks will be kept on except the clock sythesizer (WR PLL) and the synchronizer (RD PLL).
1 1 : Sleep mode. Everythings powered down expect the I/O and the logic section of the chip.

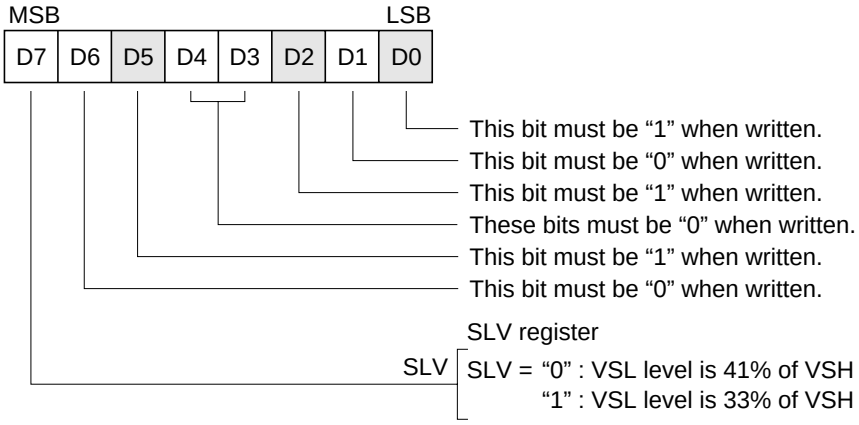
	Mode	A16h D7, 6	IDLE pin	I/O	ENDEC	Register	Bias	RDPLL	WRPLL	AGC	AF	RPD	Servo
	Normal	00	X	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
Power Save	Servo	10	0	ON	ON	ON	ON			ON	ON	ON	ON
	Idle	10	1	ON	ON	ON	ON						
	Sleep	11	X	ON		ON							

Address : $17 (at write="EE" hex, at read="AE" hex)

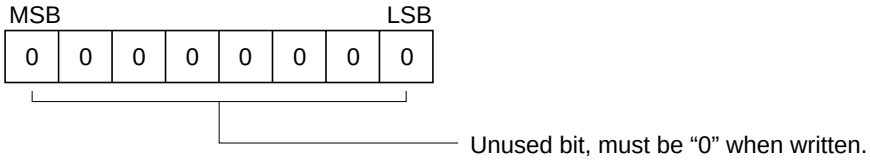


AGC Low Slice Level Ratio Control Register (SLV)

Address : $18 (at write="F0" hex, at read="B0" hex)



Address : $19 (at write="F2" hex, at read="B2" hex)



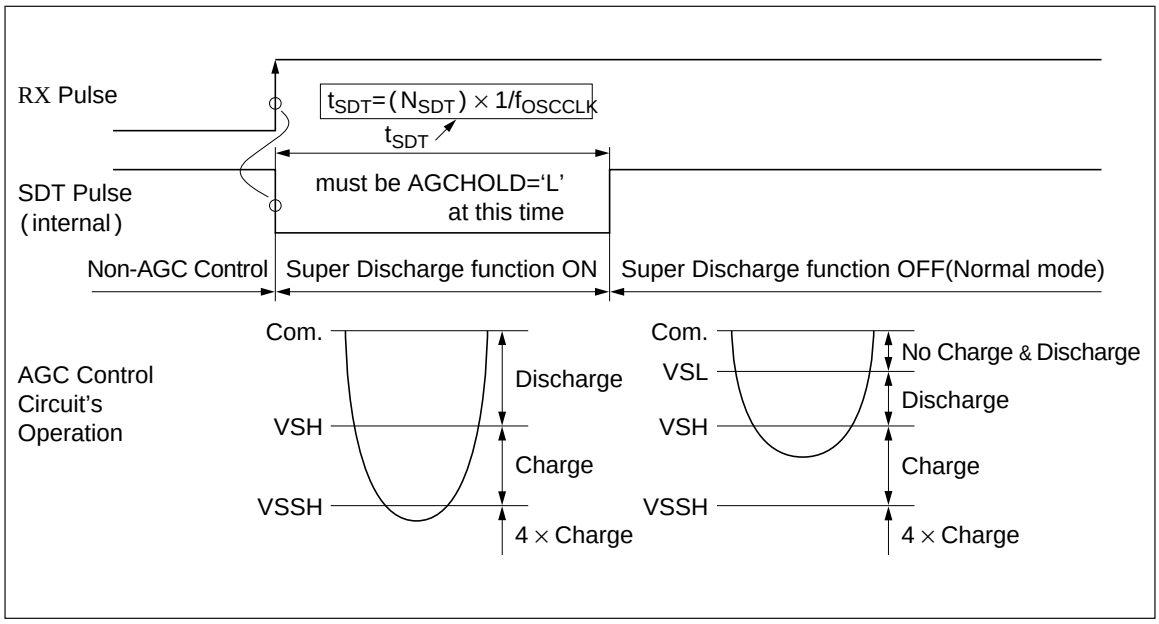


Figure 1 Super Discharge Function of the AGC Control Circuits

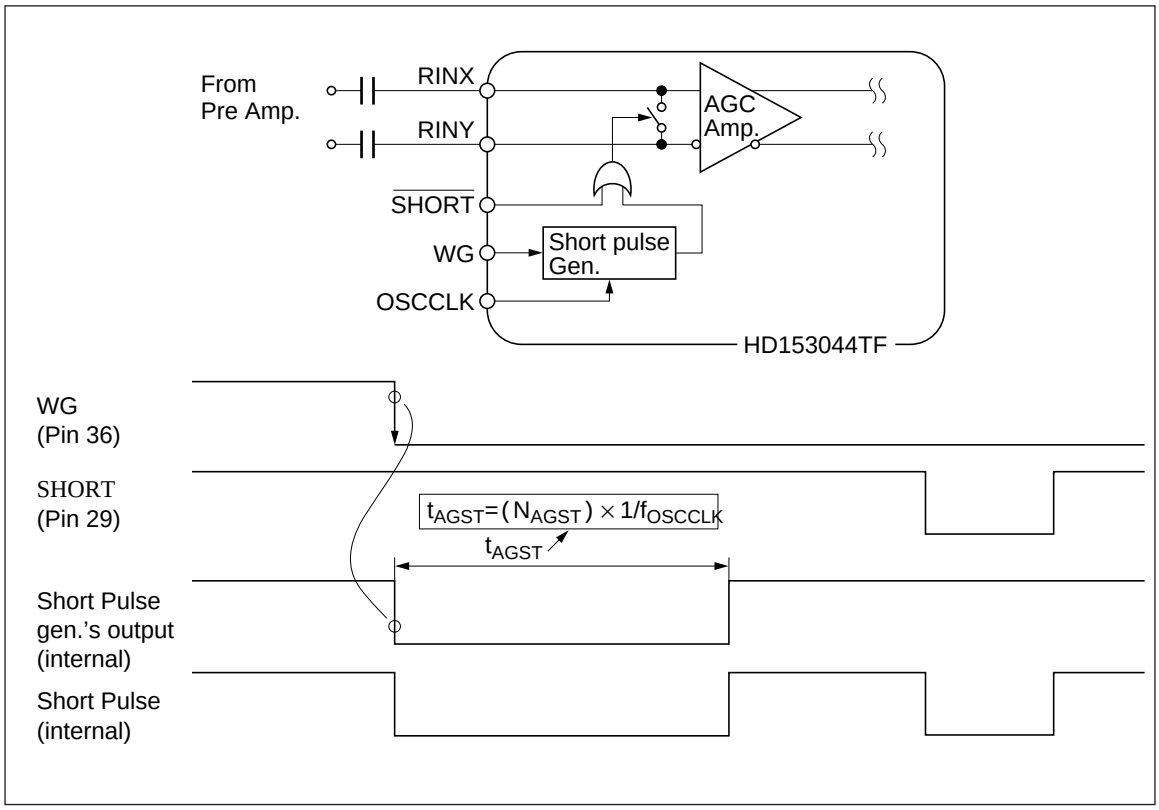
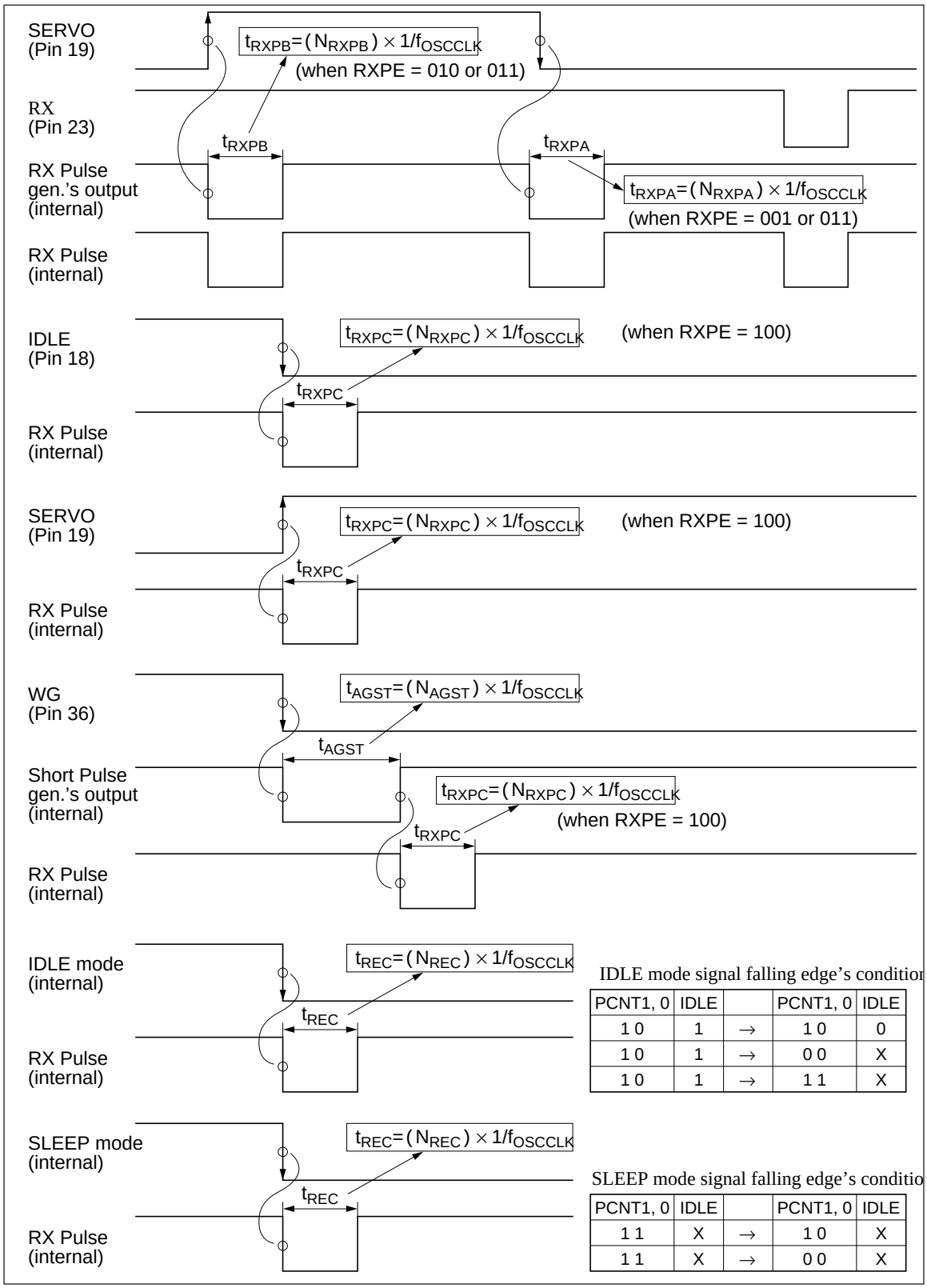


Figure 2 Short Timing Generate Function



IDLE mode signal falling edge's condition

PCNT1, 0	IDLE		PCNT1, 0	IDLE
1 0	1	→	1 0	0
1 0	1	→	0 0	X
1 0	1	→	1 1	X

SLEEP mode signal falling edge's condition

PCNT1, 0	IDLE		PCNT1, 0	IDLE
1 1	X	→	1 0	X
1 1	X	→	0 0	X

Figure 3 RX Pulse Generate Function

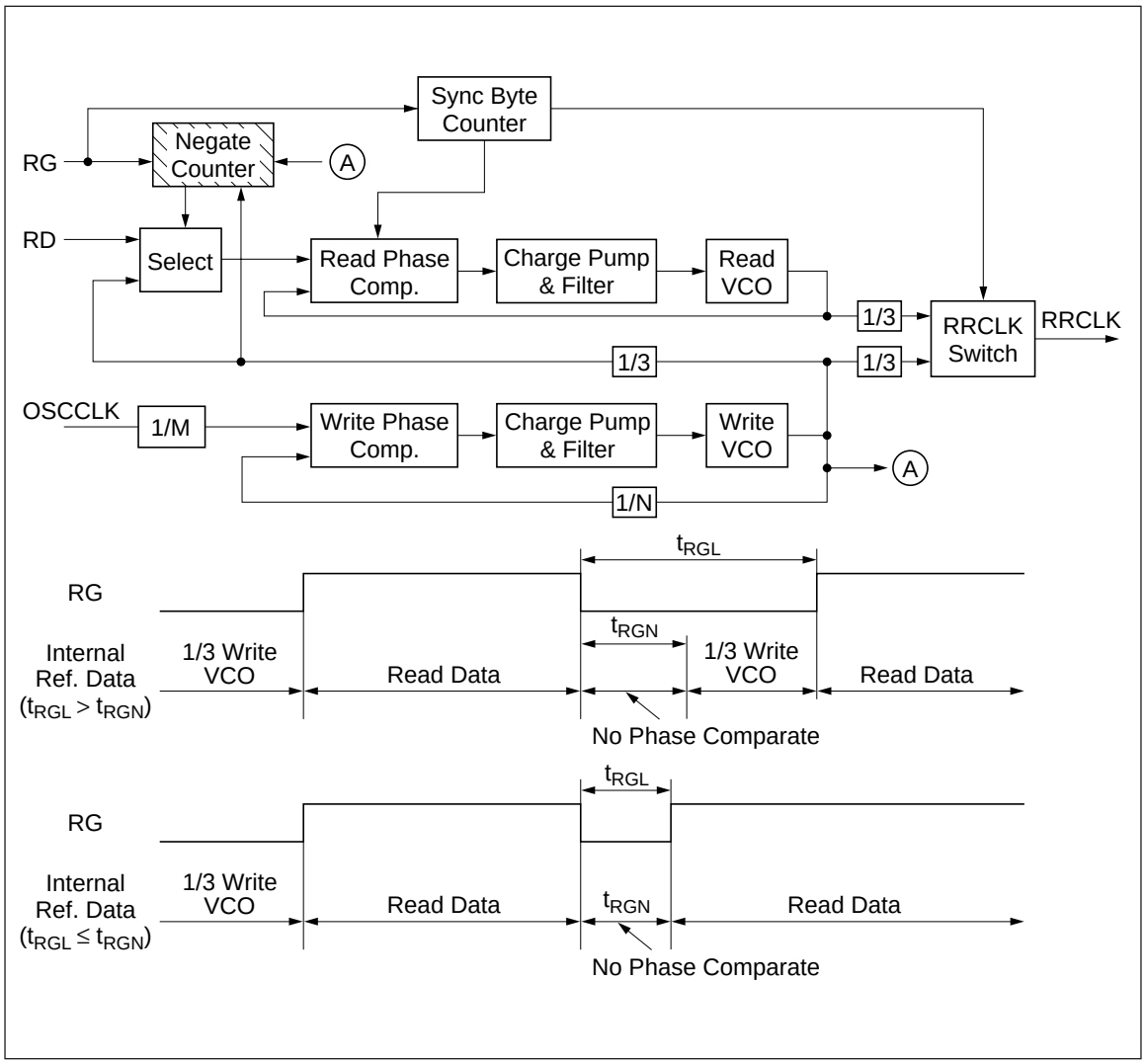
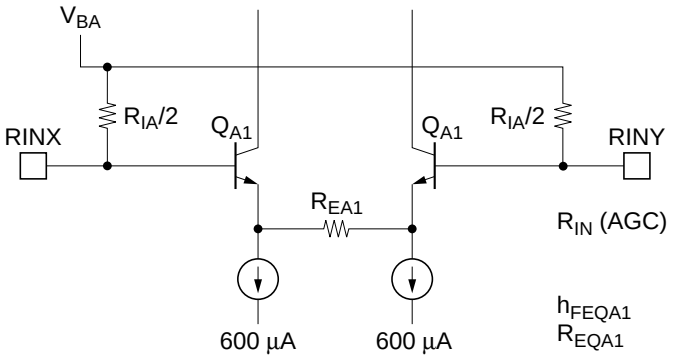


Figure 4 Read / Write PLL's Block Diagram & Negate Count Function

Input / Output Impedance of the Read Pulse Detector's Amplifier

• AGC amplifier

Input impedance

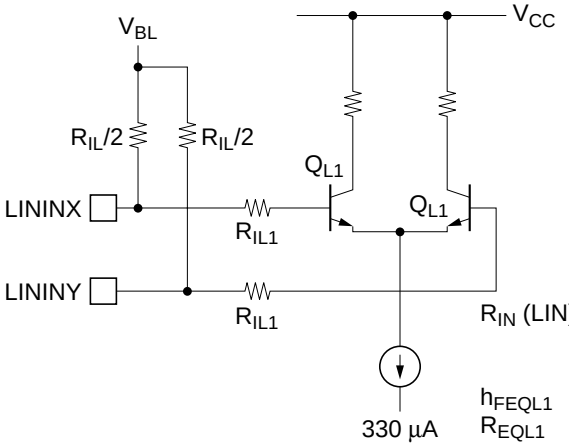


$R_{IA}/2$	1.5 kΩ
R_{EA1}	333 Ω
R_{EQA1}	43.33 Ω
h_{FEQA1}	80

R_{IN} (AGC) $\cong R_{IA}/2 \,//\, h_{FEQA1} \times (R_{EA1}/2 + R_{EQA1})$
$\cong$ 1.5 kΩ // 16.8 kΩ
$\cong$ 1.377 kΩ
h_{FEQA1} : h_{FE} of Q_{A1}
R_{EQA1} : Emitter resistance of Q_{A1}

• LIN amplifier

Input impedance



$R_{IL}/2$	1.5 kΩ
R_{EL1}	100 Ω
R_{EQL1}	157.58 Ω
h_{FEQL1}	80

R_{IN} (LIN) $\cong R_{IL}/2 \,//\, (R_{IL1} + h_{FEQL1} \times R_{EQL1})$
$\cong$ 1.5 kΩ // 12.706 kΩ
$\cong$ 1.341 kΩ
h_{FEQL1} : h_{FE} of Q_{L1}
R_{EQL1} : Emitter resistance of Q_{L1}

P/H Circuit for Servo

The P/H circuits consists of a full-wave rectifier, sample and hold, followed by a gain stage that drives internal capacitors through switches. Four outputs are made available to enable detection for four channel servo. When, the DUMP signal goes low, all holding capacitors are discharged. Then, the CHA signal is activated producing a succession of four negative pulses.

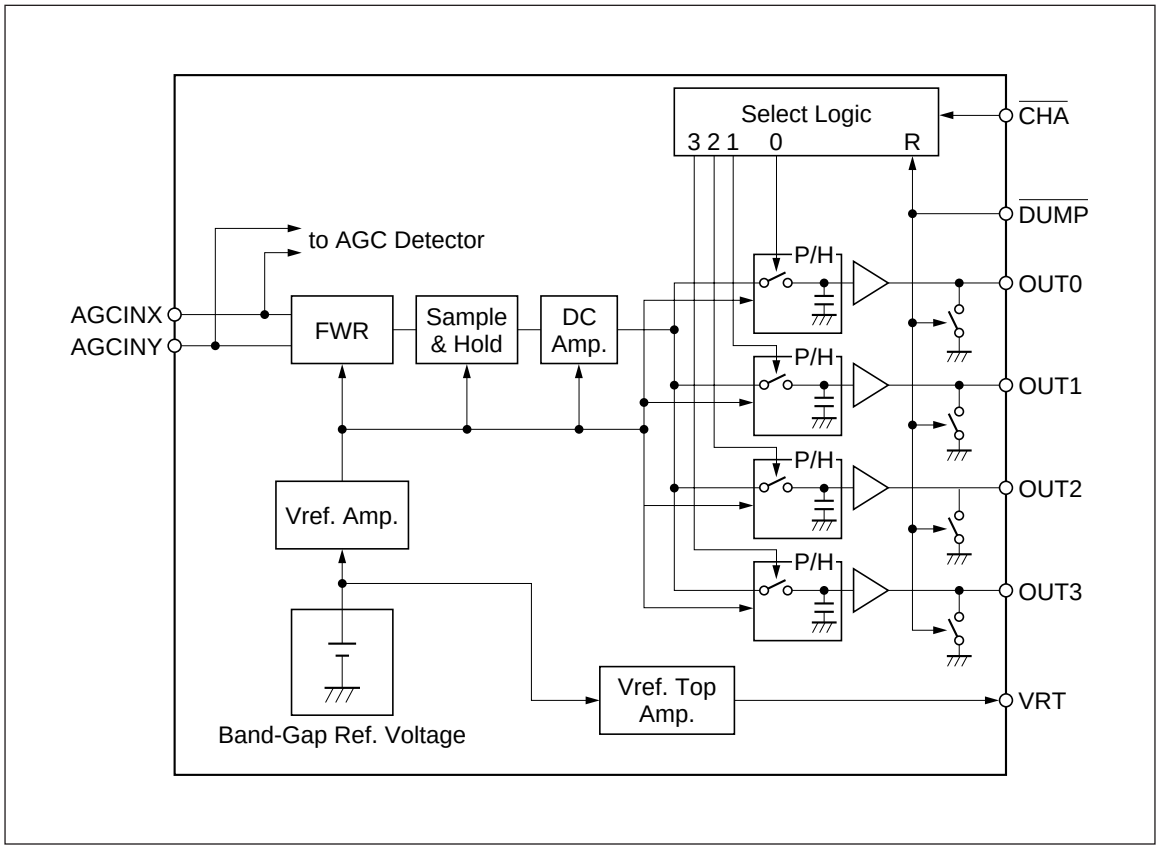


Figure 5 Servo Peak & Hold Circuit Block Diagram

AGC (Automatic Gain Control) Amplifier Circuit

The AGC amplifier is a two-stage differential amplifier. The first stage has variable gain and the second stage has fixed gain. The AGC block consists of the first stages. The output of the active filter (FILOUT and DIFOUT) stage is the second gain stage of the AGC block.

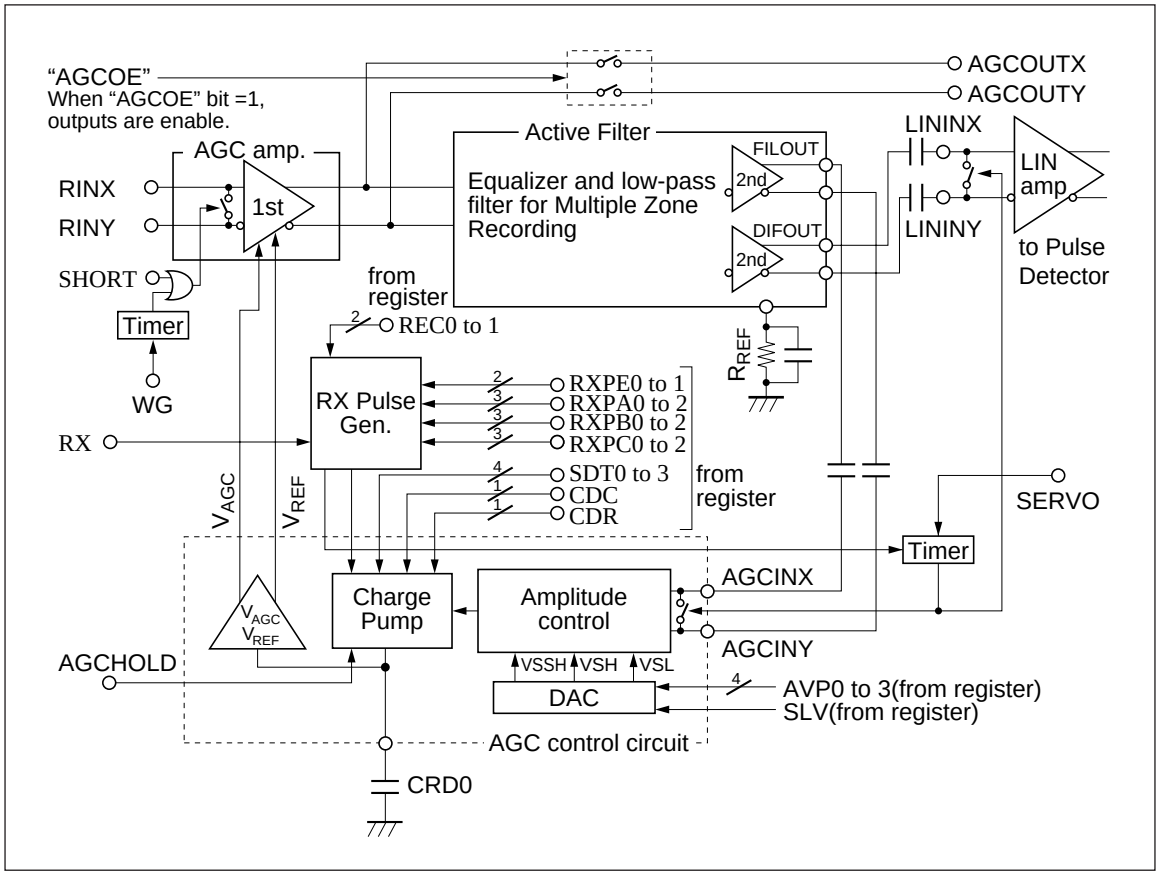


Figure 6 AGC Block Diagram

The first-stage gain can be controlled in the range from – ∞ to approximately 17 dB by an amplitude control signal (VAGC) from the AGC control circuit. The first-stage gain is given by the following formula.

$$A_V = K_1 \cdot \left(\frac{1}{1 + \exp\ (qV_C / kT)} \right)$$

$K_1 = 7.08$

$V_C = V_{AGC} - V_{REF}$

q: unit electrical charge

k: Bolzmann constant

T: absolute temperature

The second-stage amplifier within the active filter has fixed gains of 26 dB (at the outputs of FILOUT).

The AGC full gain is 142 V/V (=43 dB).

When bit 6 of register address "10001" (AGCOE bit) is set to "1", AGCOUTX and AGCOUTY pins can be used to monitor the output of the AGC amplifier. These pins are open emitter type. When monitor them, please terminate to ground by 3.9 kΩ resistor.

Bit 6 of register address "10010" (CDR register) determines the AGC control current ratio. When CDR will be set to "0", Charge: Discharge ratio will be 5 : 1. When CDR will be set to "1", Charge: Discharge ratio will be 20 : 1.

Bit 7 of register address "10010" (CDC register) determines charge current of AGC. When CDC will be set to "0", the charge current will be 500 µA. When CDC will be set to "1", the charge current will be 250 µA.

Input - Short - Circuit

The HD153044TF has a built-in Input-Short-Circuit for high speed acquisition (AGC control and LINAMP). These are controled by the register, RXPA, RXPB and RXPC, and can be selected independently for Mode Changes (SERVO to READ, READ to SERVO).
(Default value of SHORT-TIME are 5 counts of oscillator clock.) See figure 7.

RXPE	RXPA	RXPB	RXPC	t_{SRSHTf} Servo to Read		t_{SRSHTr} Read to Servo	
				$N_{RXPA}=0$	$N_{RXPA}\neq0$	$N_{RXPB}=0$ $N_{RXPC}=0$	$N_{RXPB}\neq0$ $N_{RXPC}\neq0$
0 0 0	N_{RXPA}	N_{RXPB}	*	$5\times(1/f_{OSCCLK})$	$(N_{RXPA}+2)\times(1/f_{OSCCLK})$	$5\times(1/f_{OSCCLK})$	$(N_{RXPB}+2)\times(1/f_{OSCCLK})$
0 0 1	N_{RXPA}	N_{RXPB}	*	$5\times(1/f_{OSCCLK})$	$(N_{RXPA}+2)\times(1/f_{OSCCLK})$	$5\times(1/f_{OSCCLK})$	$(N_{RXPB}+2)\times(1/f_{OSCCLK})$
0 1 0	N_{RXPA}	N_{RXPB}	*	$5\times(1/f_{OSCCLK})$	$(N_{RXPA}+2)\times(1/f_{OSCCLK})$	$5\times(1/f_{OSCCLK})$	$(N_{RXPB}+2)\times(1/f_{OSCCLK})$
0 1 1	N_{RXPA}	N_{RXPB}	*	$5\times(1/f_{OSCCLK})$	$(N_{RXPA}+2)\times(1/f_{OSCCLK})$	$5\times(1/f_{OSCCLK})$	$(N_{RXPB}+2)\times(1/f_{OSCCLK})$
1 0 0	N_{RXPA}	*	N_{RXPC}	$5\times(1/f_{OSCCLK})$	$(N_{RXPA}+2)\times(1/f_{OSCCLK})$	$5\times(1/f_{OSCCLK})$	$(N_{RXPC}+2)\times(1/f_{OSCCLK})$

Note: * Must be “0”.

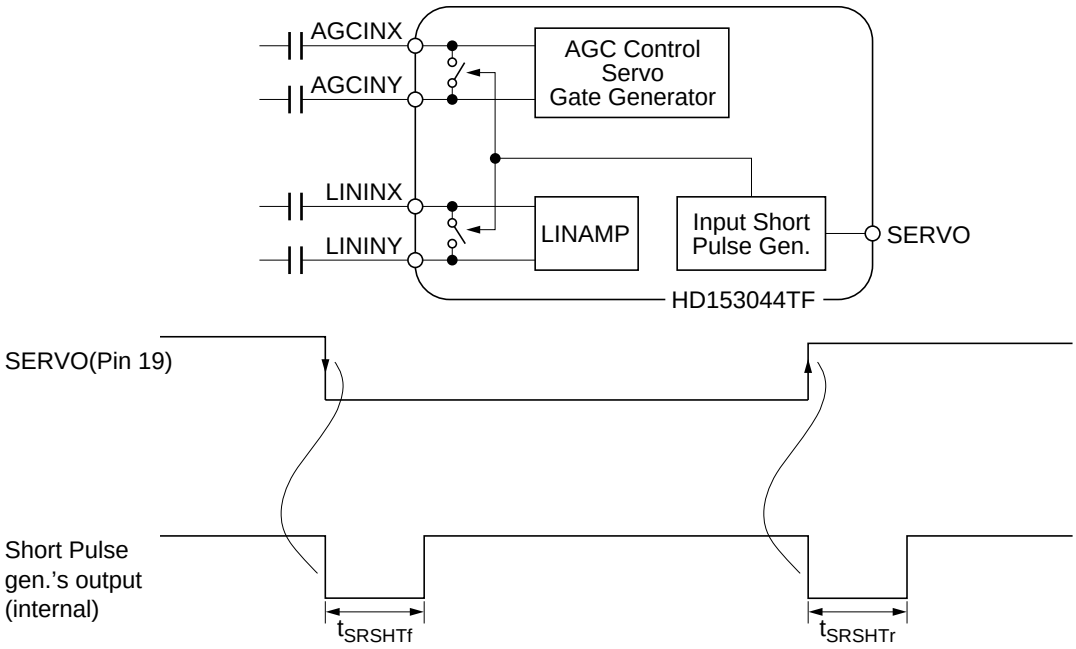


Figure 7 Input Short Pulse Genarate Function

Table 1 Charge, Discharge Current of AGC Amp. vs. CDC, CDR Register

Register "10010"

CDC	CDR	Charge Current	Discharge Current
"0"	"0"	500 µA	100 µA
"0"	"1"	500 µA	25 µA
"1"	"0"	250 µA	50 µA
"1"	"1"	250 µA	12.5 µA

The AGC amplifier gain control system is shown in figure 6. The AGC amplifier output is amplified by the post-amplifier then passed through a low-pass filter. The low-pass filter output is connected to the differentiating amplifier, and is also feedback to the AGC control circuit. Here it is compared with reference voltages V_{SH} and V_{SL} that are set internally (V_{SL} is 41 % or 33 % of V_{SH}: selectable), then the external capacitor (CRD) are charged or discharged. The charging and discharging of the external capacitor varies the control signal V_{AGC} which directly affects the gain of the AGC amplifier. The final amplitude V_P (of the AGCINX and AGCINY waveforms) in this control system can be calculated from the following equations, assuming sine waveforms:

$$T_1 \times Ich = T_2 \times Idis \quad (1)$$

$$T_1 = \left(1 - \frac{2}{\pi} \sin^{-1} \frac{V_{COM} - V_{SH}}{V_P}\right) \times T \quad (2)$$

$$T_2 = \left(1 - \frac{2}{\pi} \sin^{-1} \frac{V_{COM} - V_{SL}}{V_P}\right) \times T \quad (3)$$

From equations (1), (2) and (3):

$$\sin^{-1} \frac{V_{COM} - V_{SH}}{V_P} - \frac{Idis}{Ich} \sin^{-1} \frac{V_{COM} - V_{SL}}{V_P} = \frac{\pi}{2}\left(1 - \frac{Idis}{Ich}\right) \quad (4)$$

The final amplitude of the AGC amplifier loop is determined mainly by the V_{SH} bias level. If appropriate values are set for V_{SL}, Ich and Idis, then from the preceding equations the final differential peak voltage V_{PDF} is:

$$V_{PDF} = 4\,(V_{COM} - V_{SH}) \times m \quad (5)$$

where m = 1.00 to 1.05

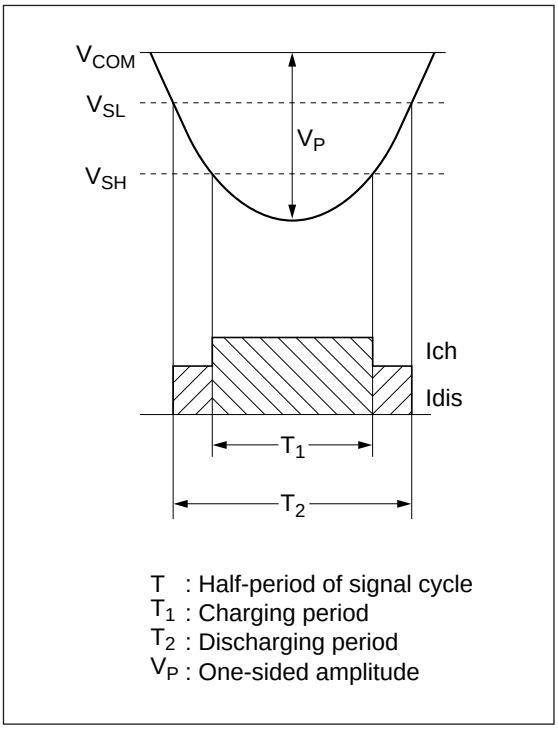


Figure 8 Charge / Discharge Timing

Programmable Active Filter Circuit

Active filter consists of equalizer and electronic filter. Electronic filter is 7-pole, equiripple-type, low-pass filter and can be used in multiple zone recording (MZR) design. Cut-off frequency of filter is set by writing to register CFCR and CFCS. The equalizer is double differentiation pulse sliming equalization. The boost level is set by writing to register BLCR and BLCS.

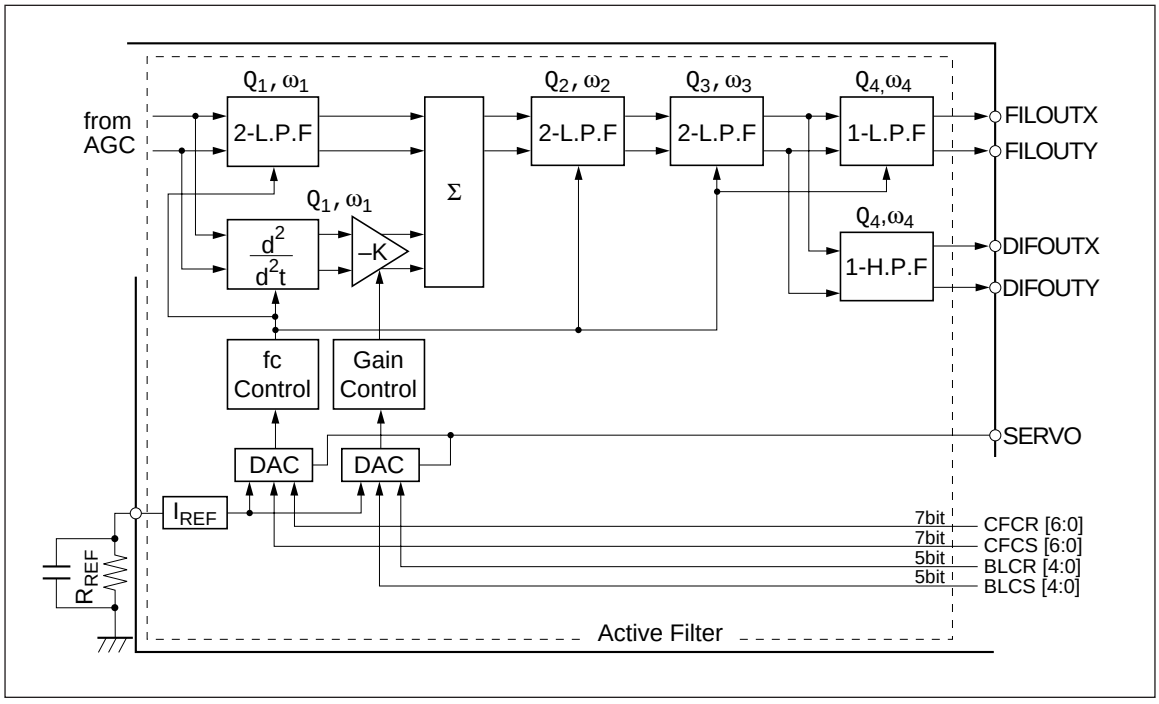
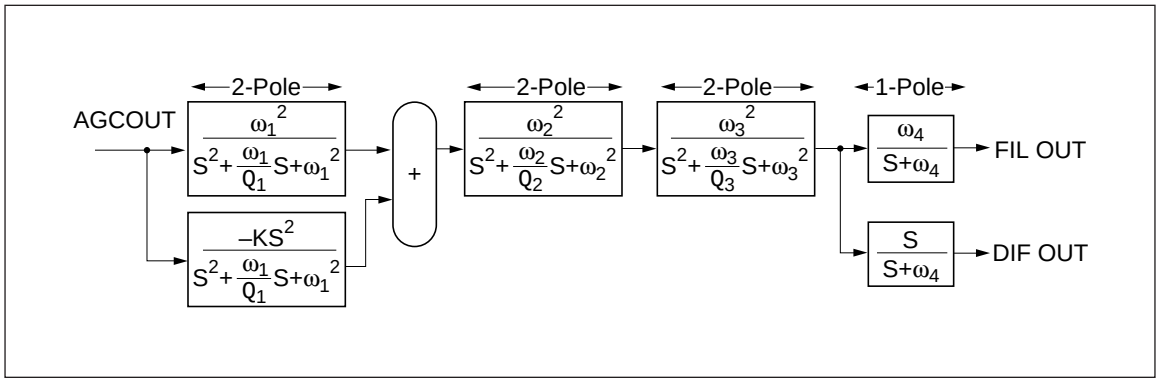


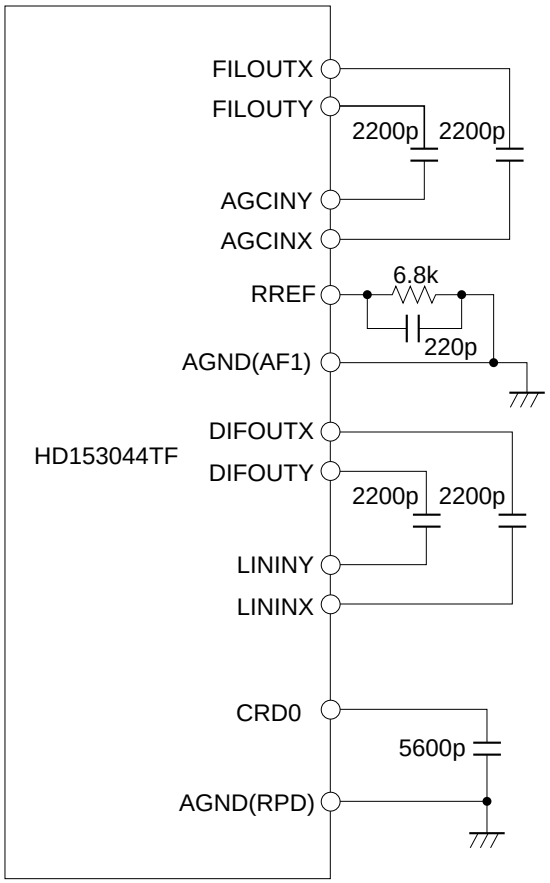
Figure 9 Active Filter Block Diagram

Transfer Function



Example of External Components Connected to the RPD

These values are tentative.



Unit R: Ω
C: F

AGC (Automatic Gain Control) Amplifier Circuit

The AGC amplifier is a two-stage differential amplifier. The first stage has variable gain and the second stage has fixed gain. The AGC block consists of the first stages. The output of the active filter (FILOUT and DIFOUT) stage is the second gain stage of the AGC block.

Figure 6 AGC Block Diagram

The first-stage gain can be controlled in the range from $-\infty$ to approximately 17 dB by an amplitude control signal (VAGC) from the AGC control circuit. The first-stage gain is given by the following formula.

$K_1 = 7.08$
$V_C = V_{AGC} - V_{REF}$
q: unit electrical charge
k: Bolzmann constant
T: absolute temperature

The second-stage amplifier within the active filter has fixed gains of 26 dB (at the outputs of FILOUT).

The AGC full gain is 142 V/V (=43 dB).
When bit 6 of register address “10001” (AGCOE bit) is set to “1”, AGCOUTX and AGCOUTY pins can be used to monitor the output of the AGC amplifier. These pins are open emitter type. When monitor them, please terminate to ground by 3.9 kΩ resistor.
Bit 6 of register address “10010” (CDR register) determines the AGC control current ratio. When CDR will be set to “0”, Charge: Discharge ratio will be 5 : 1. When CDR will be set to “1”, Charge: Discharge ratio will be 20 : 1.
Bit 7 of register address “10010” (CDC register) determines charge current of AGC. When CDC will be set to “0”, the charge current will be 500 µA. When CDC will be set to “1”, the charge current will be 250 µA.

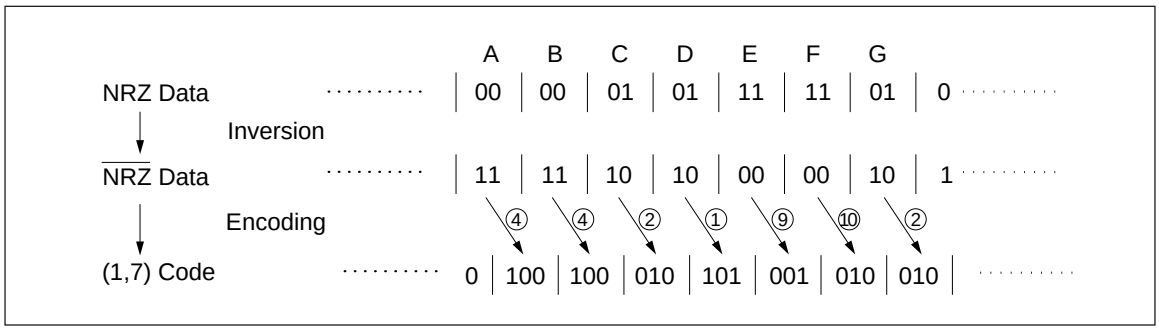


Figure 10 Shows an Example of NRZ to (1, 7) Code Conversion

Table 3 Decoding Table ((1, 7) Code to NRZ)

	(1, 7) Code Bits										
No.	**Previous**			**Current**			**Next**			**NRZ Data Bit**	
1	X	1	0	0	0	0	X	X	X	0	0
2	X	0	0	0	0	0	X	X	X	0	1
3	X	X	X	1	0	0	X	X	X	1	1
4	X	X	0	0	1	0	$\overline{0}$	$\overline{0}$	X	1	0
5	X	X	0	0	1	0	0	0	X	1	1
6	X	X	X	1	0	1	X	X	X	1	0
7	X	0	0	0	0	1	X	X	X	0	1
8	X	1	0	0	0	1	X	X	X	0	0
9	X	X	1	0	0	1	X	X	X	0	0
10	X	X	1	0	1	0	$\overline{0}$	$\overline{0}$	X	0	0
11	X	X	1	0	1	0	0	0	X	0	1
12	X	X	1	0	0	0	X	X	X	0	1

00 : Anything other than 00
X: Don't care

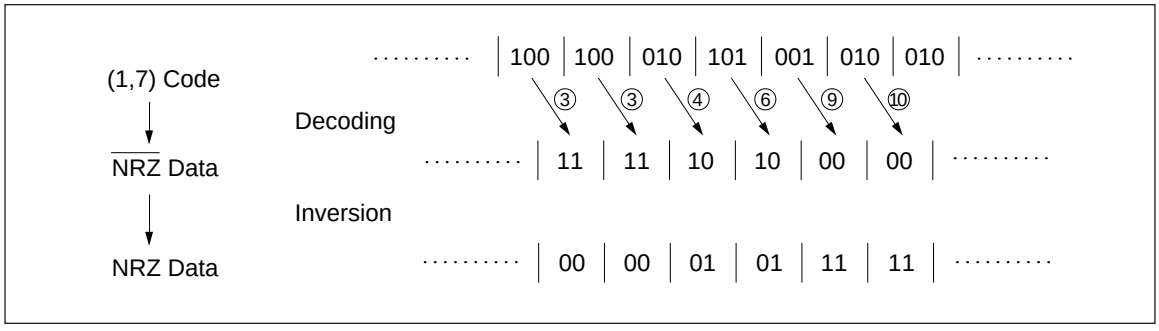
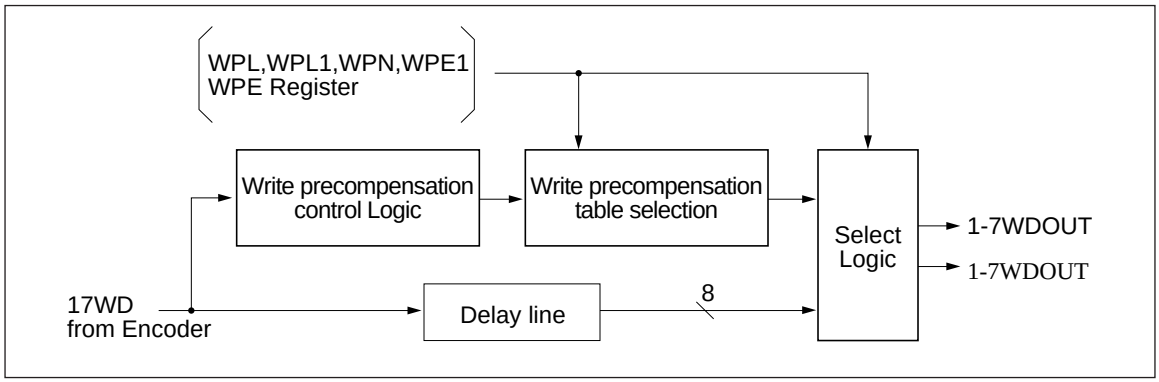


Figure 11 (1, 7) Code to NRZ Decoding Example

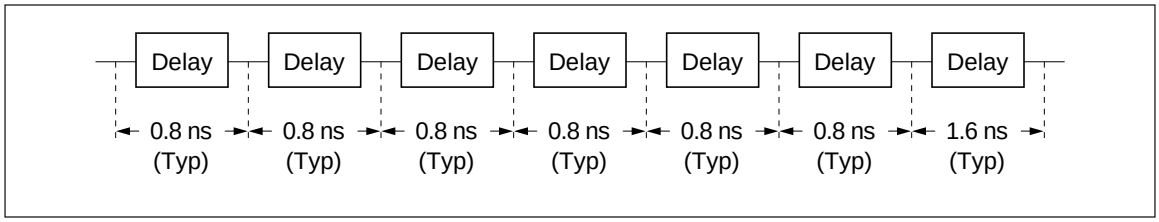
Write Precompensation Circuit

The HD153044TF has a built-in synchronous write precompensation circuit, and the 5 matrix delay levels from the write precompensation table shown below can be selected independently for the NORMAL (N), EARLY (E, E1) and LATE (L, L1) sides. Each delay group of the table can select delay value independently.

(1) Circuit Configuration

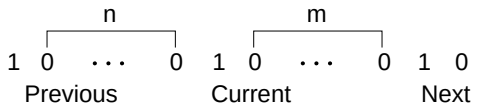


(2) Programmable Delay Line



(3) Table

n \ m	1	2	3	4	5	6	7
1	N	E					
2	L	N	E1				
3		L1	N				
4							
5							
6							
7							



n : The number of zero's between the current 1 bit and the previous 1 bit

m : The number of zero's between the current 1 bit and the next 1 bit

The precompensation delay time for each the 5 matrix entries in the precompensation table (see Table) can be set independently.
The delay time (8 levels) is selected by the each part of register.

Decode Window Adjustment Circuits

The delay value of T/2 delay and adjustment delay (WAJ = "010100") are always 1/2 VCO clock period, when VFC register and WTS register are setting.

When window center adjustment mode, the latch input data's delay will be controlled by WAJ register. The width of the window adjustment is –50 % to +50 %, and resolution is 3 % per step of T/2.

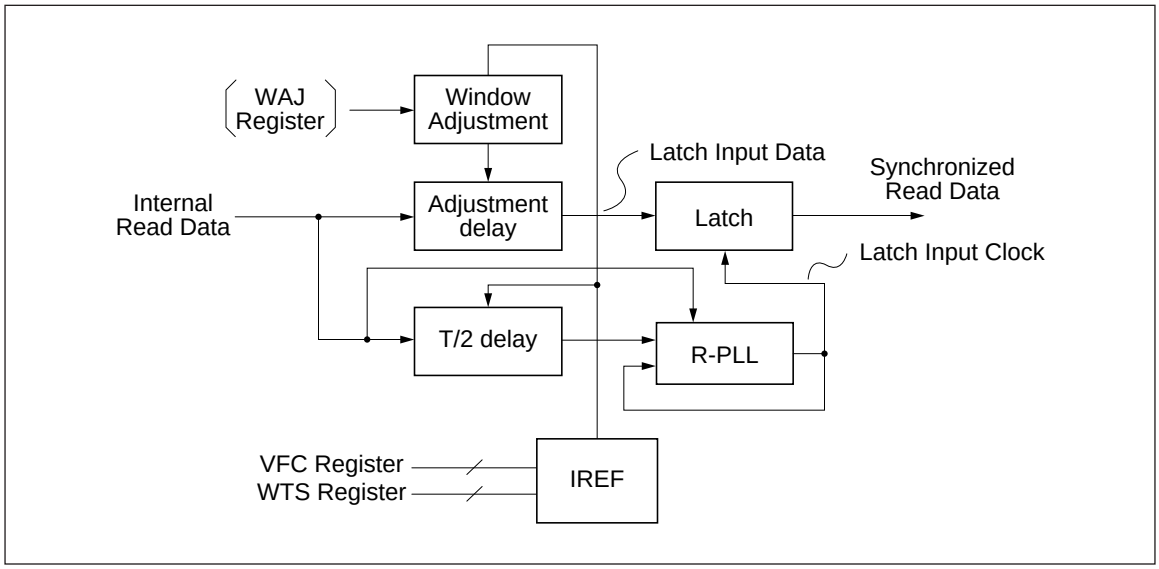


Figure 12 Window Adjustment Circuit Block Diagram

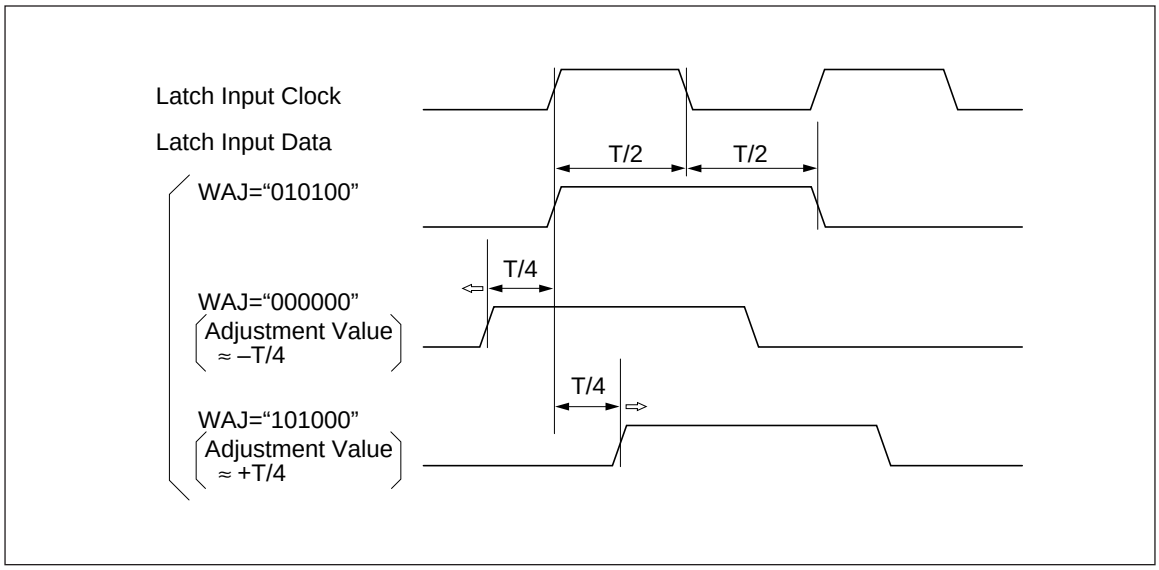
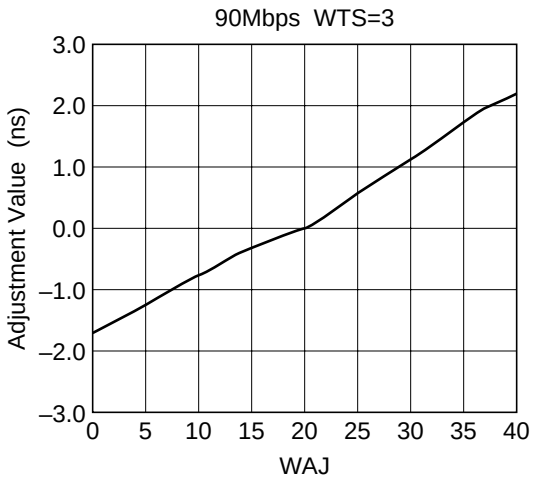
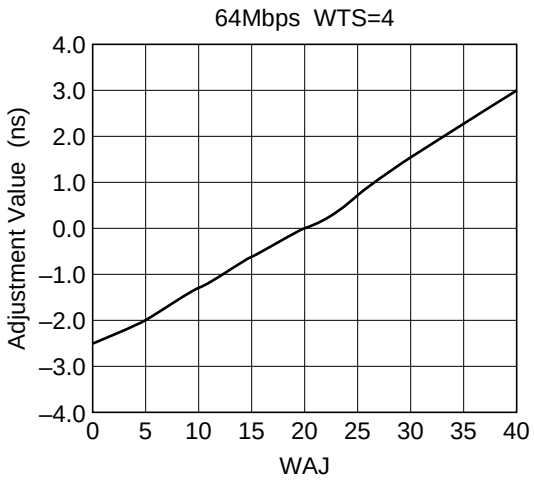
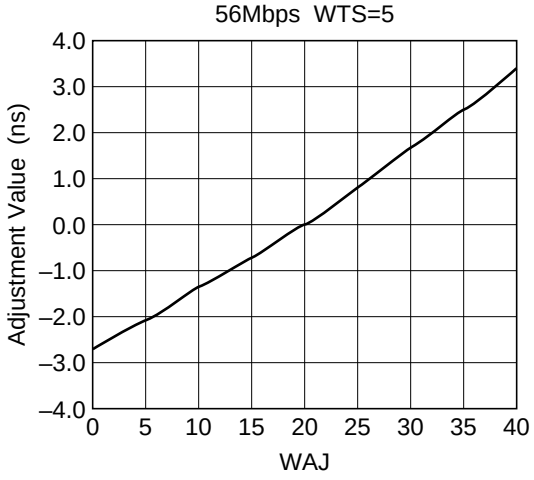


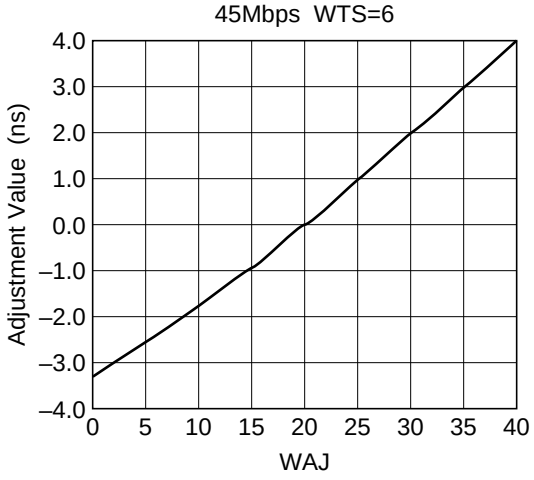
Figure 13 Window Adjustment Timing Waveform

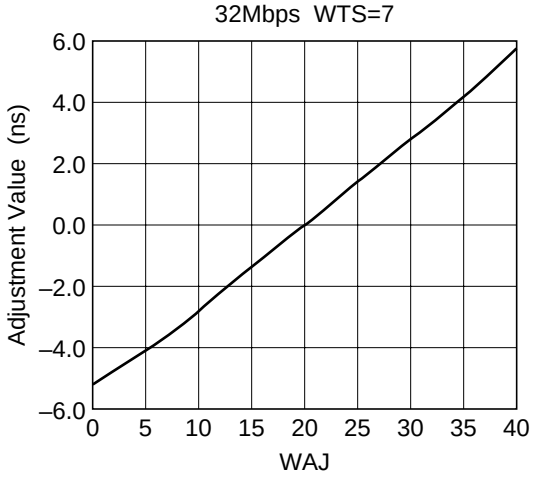
The Relation Between WAJ Register and Window Adjustment Value











Sync Field Detection

By using an internal counter to the transition (24 or 32 pulses), the HD153044TF RD-PLL can operate in the high-gain mode immediatly after RG is asserted, then automatically switched over to the normal-gain mode after the counter counts 24 or 32 transitions (4×6 or 4×8).

It is recommended that the sync field should be of 3T pattern, and that a minimum of "6-NRZ-byte" period is allowed for proper RD-PLL phase locking.

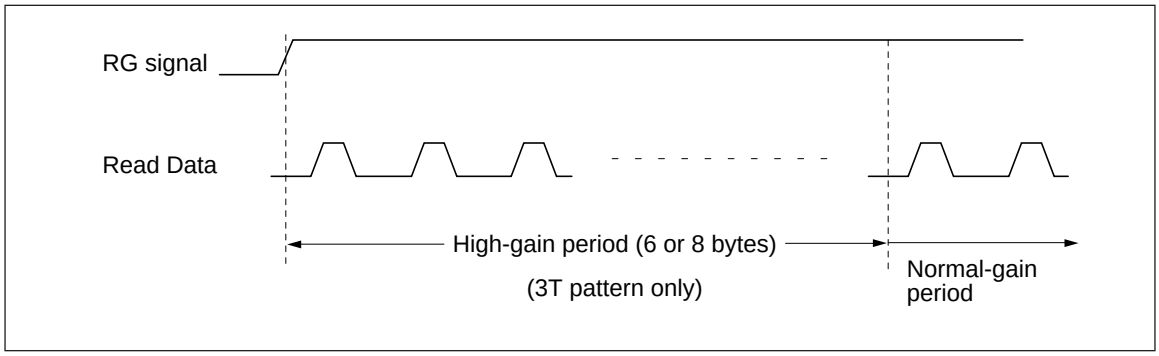


Figure 14 Sync Field Detection Timing

Read and Write Mode

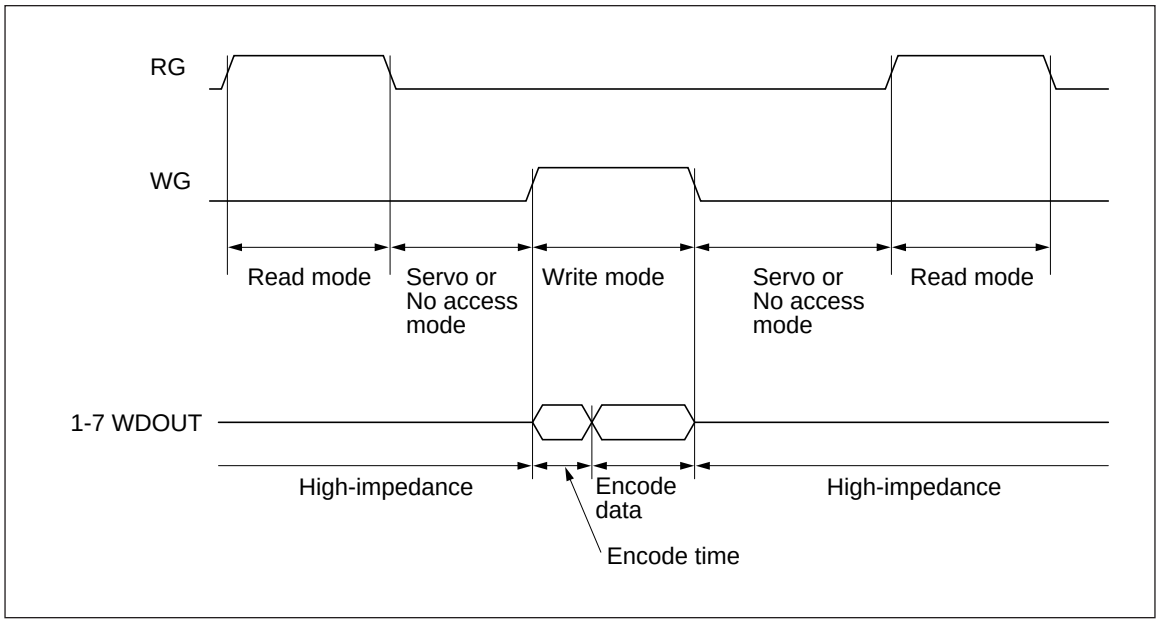
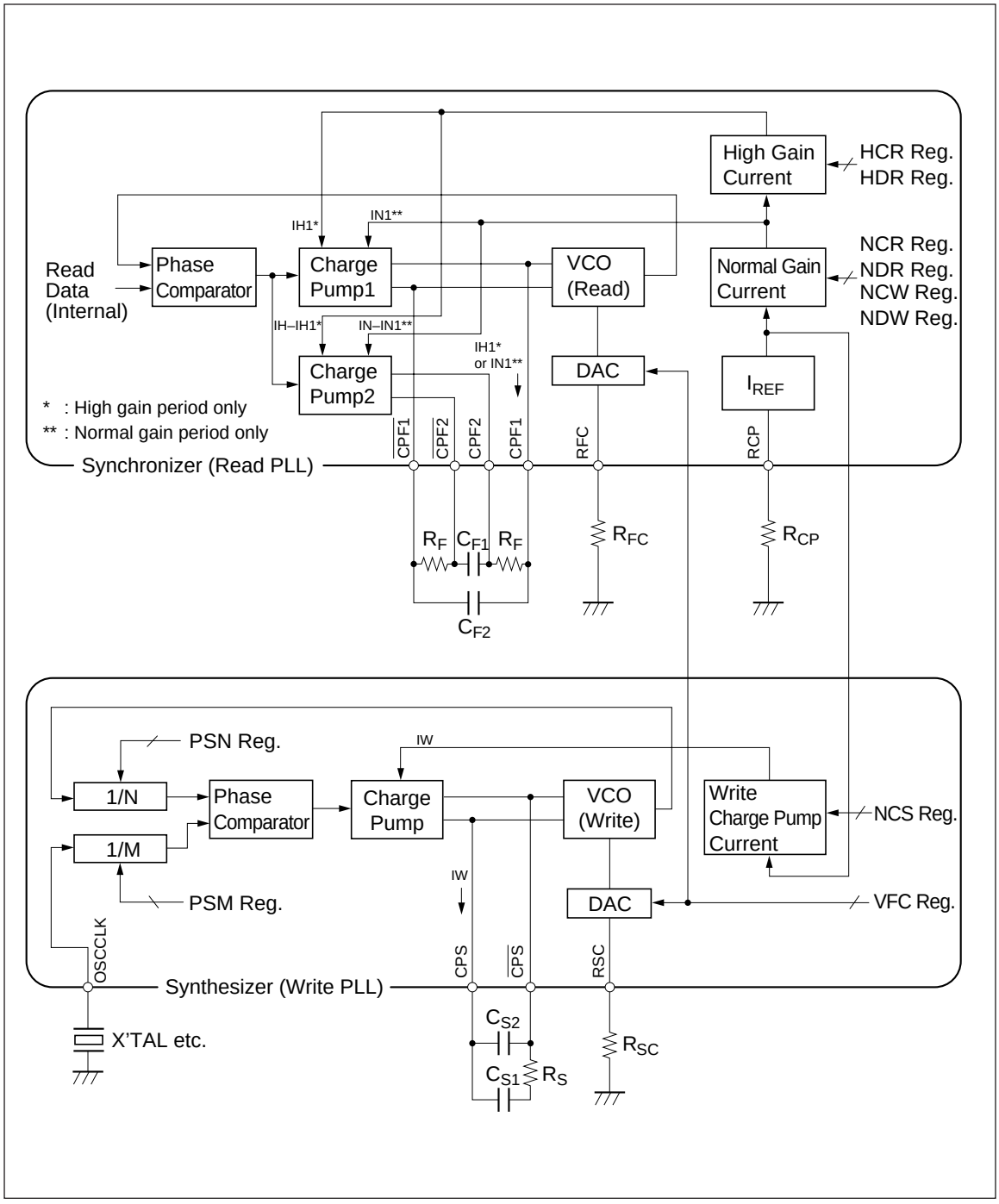


Figure 15 Read and Write Mode Timing

Read and Write PLL Block Diagram



Calculation of PLL Constants

1. Encode Clock Generator's Frequency Synthesizer (W-PLL)

1. VCO center frequency f_{CW}

$$f_{CW} = \frac{(7.714 \times 10^9) \cdot L}{R_{SC}} \text{ (Hz)} \quad (1\text{-}1)$$

where $22 \le L \le 63$ (L : VFC register value)

2. VCO oscillation frequency f_{OW}

$$f_{OW} = \frac{N}{M} \cdot f_{OSC} \text{ (Hz)} \quad (1\text{-}2)$$

where $4 \le M \le 255$ (M : PSM register value)
where $4 \le N \le 255$ (N : PSN register value)
fosc : Oscclk's input frequency

3. VCO gain K_{OW}

$$K_{OW} = (1.74 \times 10^9) \cdot \sqrt{\frac{L}{R_{SC}}} \left(\frac{\text{rad}}{\text{sec} \cdot \text{V}}\right) \quad (1\text{-}3)$$

where $22 \le L \le 63$ (L : VFC register value)

4. Charge pump current I_W

$$I_W = (9.75 \times 10^{-2}) \cdot \frac{NCS + 1}{R_{CP}} \text{ (A)} \quad (1\text{-}4)$$

where $0 \le NCS \le 15$ (NCS : NCS register value)

5. Characteristics frequency ω_{nW}

$$\omega_{nW} = \sqrt{\frac{K_{OW} \cdot I_W}{2\pi \cdot N \cdot (C_{S1} + C_{S2})}} \left(\frac{\text{rad}}{\text{sec}}\right) \quad (1\text{-}5)$$

where $4 \le N \le 255$ (N : PSN register value)

6. Attenuation ζ_W

$$\zeta_W = \frac{1}{2} \cdot C_{S1} \cdot R_S \cdot \omega_{nW} \quad (1\text{-}6)$$

2. Decode Clock Generator's VFO

1. VCO center frequency f_{CR}

$$f_{CR} = \frac{(7.714 \times 10^9) \cdot L}{R_{FC}} \text{ (Hz)} \quad (2\text{-}1)$$

where $22 \le L \le 63$ (L : VFC register value)

2. VCO gain K_{OR}

$$K_{OR} = (6.07 \times 10^9) \cdot \sqrt{\frac{L}{R_{FC}}} \left(\frac{\text{rad}}{\text{sec} \cdot \text{V}}\right) \quad (2\text{-}2)$$

where $22 \le L \le 63$ (L : VFC register value)

3. Charge pump normal gain current I_N, I_{N1}

$$I_N = (9.75 \times 10^9) \cdot \frac{NCR + 1}{R_{CP}} \text{ (A)} \quad (2\text{-}3)$$

where $0 \le NCR \le 15$ (NCR : NCR register value)

$$I_{N1} = \frac{NDR + 1}{16} \cdot I_N \text{ (A)} \quad (2\text{-}4)$$

where $0 \le NDR \le 15$ (NDR : NDR register value)

4. Charge pump high gain current I_H, I_{H1}

$$I_H = \frac{HCR + 3}{2} \cdot I_N \text{ (A)} \quad (2\text{-}5)$$

where $0 \le HCR \le 15$ (HCR : HCR register value)

$$I_{H1} = \frac{HDR}{32} (I_H - I_N) + I_{N1} \text{ (A)} \quad (2\text{-}6)$$

where $0 \le HDR \le 15$ (HDR : HDR register value)

5. Charge pump reference gain current I_R, I_{R1}

$$I_R = (9.75 \times 10^{-2}) \cdot \frac{NCW + 1}{R_{CP}} \text{ (A)} \quad (2\text{-}7)$$

where $0 \le NCW \le 15$ (NCW : NCW register value)

$$I_{R1} = \frac{NDW + 1}{16} \cdot I_R \text{ (A)} \quad (2\text{-}8)$$

where $0 \le NDW \le 15$ (NDW : NDW register value)

6. Characteristic frequency (high gain) ω_{nRH}

$$\omega_{nRH} = \sqrt{\frac{K_{OR} \cdot I_H}{2\pi \cdot 3 \cdot (C_{F1} + C_{F2})}} \left(\frac{rad}{sec}\right) \quad (2\text{-}9)$$

7. Characteristic frequency (normal gain) ω_{nRN}

$$\omega_{nRN} = \sqrt{\frac{K_{OR} \cdot I_N}{2\pi \cdot 4 \cdot (C_{F1} + C_{F2})}} \left(\frac{rad}{sec}\right) \quad (2\text{-}10)$$

8. Characteristic frequency (reference gain) ω_{nRR}

$$\omega_{nRR} = \sqrt{\frac{K_{OR} \cdot I_R}{2\pi \cdot 3 \cdot (C_{F1} + C_{F2})}} \left(\frac{rad}{sec}\right) \quad (2\text{-}11)$$

9. Attenuation (high gain) ζ_{RH}

$$\zeta_{RH} = C_{F1} \cdot R_F \cdot \omega_{nRH} \cdot \frac{I_{H1}}{I_H} \quad (2\text{-}12)$$

10. Attenuation (normal gain) ζ_{RN}

$$\zeta_{RN} = C_{F1} \cdot R_F \cdot \omega_{nRN} \cdot \frac{I_{N1}}{I_N} \quad (2\text{-}13)$$

11. Attenuation (reference gain) ζ_{RR}

$$\zeta_{RR} = C_{F1} \cdot R_F \cdot \omega_{nRR} \cdot \frac{I_{R1}}{I_R} \quad (2\text{-}14)$$

Calculation Example of HD153044TF W-PLL Constants

Transfer rate ; 90 Mbps, 64 Mbps, 32 Mbps 3 zones

(1) R_{SC} = 3.6 k
VCO center frequency = 135 MHz (L = 63)

(2) PSM register, PSN register (M, N)

where Transfer rate = $\frac{2}{3} \times f_{OW}$,

$f_{OW} = \frac{N}{M} \cdot f_{OSC}$

$\therefore$ Transfer rate = $\frac{2}{3} \times \frac{N}{M} \cdot f_{OSC}$

where fosc = 20 MHz,
Transfer rate resolution = 0.5 Mbps

$\therefore M = \frac{2}{3} \times \frac{f_{OSC}}{0.5 \times 10^6} = 27$

$\therefore$ Transfer rate = $\frac{2}{3} \times \frac{N}{27} \times 20 \times 10^6$ bps

$\therefore$ 90Mbps $N_{90} = \frac{90 \times 10^6}{20 \times 10^6} \times \frac{3}{2} \times 27 = 182$

64Mbps $N_{64} = \frac{64 \times 10^6}{20 \times 10^6} \times \frac{3}{2} \times 27 = 130$

32Mbps $N_{32} = \frac{32 \times 10^6}{20 \times 10^6} \times \frac{3}{2} \times 27 = 65$

(3) C_{S1}, C_{S2} (calculate from max. transfer rate)

where $\omega_n \leq \frac{1}{30} \times 2\pi \times \frac{f_{OSC}}{M}$

$\omega_n = \frac{1}{40} \times 2\pi \times \frac{20 \times 10^6}{27} = 116.4$krad / s

Max. transfer rate = $\frac{2}{3} \times \frac{182}{27} \times 20 \times 10^6$
= 89.88Mbps

where I_W = max. (NCS = 15)

$I_W = (9.75 \times 10^{-2}) \cdot \frac{15 + 1}{3.9 \times 10^3} = 400\mu A$

where calculate VCO gain from L

$89.88 \times 10^6 \times \frac{3}{2} = \frac{7.714 \times 10^9}{3.6 \times 10^3} \times L$

$\therefore L = 63$

$\therefore K_{OW90} = 1.74 \times 10^9 \sqrt{\frac{63}{3.6 \times 10^3}}$
= 230.2Mrad / s · V

where $C_{S2} = \frac{C_{S1}}{40}$

$116.4 \times 10^3 = \sqrt{\frac{400 \times 10^{-6} \times 230.2 \times 10^6}{2\pi \times 182 \times 41 / 40\ C_{S1}}}$

$\therefore C_{S1}$ = 5600pF C_{S2} = 150pF

ω_{nW90} = 118.3krad / s

(4) R_S (calculate from max. transfer rate)
where ζ_{W90} = 1.0

$1.0 = \frac{1}{2} \times 5600 \times 10^{-12} \times R_S \times 118.3 \times 10^3$

$\therefore R_S$ = 3.0k ζ_{W90} = 0.9937

(5) 64 Mbps

Transfer rate = $\frac{2}{3} \times \frac{130}{27} \times 20 \times 10^6$
= 64.20Mbps

where calculate VCO gain from L

$64.20 \times 10^6 \times \frac{3}{2} = \frac{7.714 \times 10^9}{3.6 \times 10^3} \times L$

$\therefore L = 45$

$\therefore K_{OW45} = 1.74 \times 10^9 \sqrt{\frac{45}{3.6 \times 10^3}}$
= 194.5Mrad / s · V

where $\omega_{nW90} = \omega_{nW64}$

$118.3 \times 10^3 = \sqrt{\frac{I_W \times 194.5 \times 10^6}{2\pi \times 130 \times 5750 \times 10^{-12}}}$

$\therefore I_W$ = 347.8µA

$347.8 \times 10^{-6} = 9.75 \times 10^{-2} \times \frac{NCS + 1}{3.9 \times 10^3}$

$\therefore$ NCS = 13 I_W = 350µA

ω_{nW64} = 120.4krad / s

$\therefore \zeta_{W64} = \frac{1}{2} \times 5600 \times 10^{-12} \times 3.0 \times 10^3$
$\times 120.4 \times 10^3 = 1.011$

(6) 32 Mbps

$$\text{Transfer rate} = \frac{2}{3} \times \frac{65}{27} \times 20 \times 10^6$$
$$= 32.10\text{Mbps}$$

where calculate VCO gain from L

$$32.10 \times 10^6 \times \frac{3}{2} = \frac{7.714 \times 10^9}{3.6 \times 10^3} \times L$$

$$\therefore L = 22$$

$$\therefore K_{OW32} = 1.74 \times 10^9 \sqrt{\frac{22}{3.6 \times 10^3}}$$
$$= 136.0\text{Mrad / s} \cdot \text{V}$$

where $\omega_{nW90} = \omega_{nW32}$

$$118.3 \times 10^3 = \sqrt{\frac{I_W \times 136.0 \times 10^6}{2\pi \times 65 \times 5750 \times 10^{-12}}}$$

$$\therefore I_W = 241.7\mu\text{A}$$

$$241.7 \times 10^{-6} = 9.75 \times 10^{-2} \times \frac{NCS + 1}{3.9 \times 10^3}$$

$$\therefore NCS = 9, I_W = 250\mu\text{A},$$
$$\omega_{nW32} = 120.3\text{krad / s}$$

$$\therefore \zeta_{W32} = \frac{1}{2} \times 5600 \times 10^{-12} \times 3.0 \times 10^3$$
$$\times 120.3 \times 10^3 = 1.011$$

Calculation Example of HD153044TF R-PLL Constants

Transfer rate ; 90 Mbps, 64 Mbps, 32 Mbps 3 zones

(1) R_{FC} = 3.6 kΩ VCO center frequency = 135 MHz (L = 63)

(2) R_{CP} = 3.9 kΩ

(3) VCO gain K_{0R}

$$K_{OR90} = 6.07 \times 10^9 \sqrt{\frac{63}{3.6 \times 10^3}} = 803.0\text{Mrad / s} \cdot \text{V}$$

$$K_{OR64} = 6.07 \times 10^9 \sqrt{\frac{45}{3.6 \times 10^3}} = 678.6\text{Mrad / s} \cdot \text{V}$$

$$K_{OR32} = 6.07 \times 10^9 \sqrt{\frac{22}{3.6 \times 10^3}} = 474.5\text{Mrad / s} \cdot \text{V}$$

(4) C_{F1}, C_{F2} (calculate from max. transfer rate's high gain)

where $\omega_n \cdot T_{aq90} = 30$

$$T_{aq90} = \frac{8}{90 \times 10^6} \cdot 4.9 \text{ bytes} = 436\text{ns}$$

(Register setting ; 6 bytes)

ω_{nRH90} = 6.88 Mrad/s

where $C_{F2} = \frac{C_{F1}}{200}$ α I_H (max.) = 1.1mA C

3T sync pattern

$$6.88 \times 10^6 = \sqrt{\frac{1.1 \times 10^{-3} \times 803.0 \times 10^6}{2\pi \times 3 \times 201 / 200\ C_{F1}}}$$

$\therefore C_{F1}$ = 1000pF α C_{F2} = 5pF

(5) R_F (calculate from min. transfer rate's normal gain)

where NDR = 15 (max.)

where $\omega_n \cdot T_{aq32} = 3.0$

$$T_{aq32} = \frac{8}{32 \times 10^6} \cdot 4.9 \text{ bytes} = 1225\text{ns}$$

(Register setting ; 6 bytes)

ω_{nRH32} = 2.45 Mrad/s

$$2.45 \times 10^6 = \sqrt{\frac{I_H \times 474.5 \times 10^6}{2\pi \times 3 \times 1005 \times 10^{-12}}}$$

$\therefore I_H = 240\mu\text{A}$

where HCR = 3

$$I_N = \frac{2}{3+3} \times 240 \times 10^{-6} = 80.0\mu\text{A}$$

$$80.0 \times 10^{-6} = 9.75 \times 10^{-2} \times \frac{\text{NCR} + 1}{3.9 \times 10^3}$$

$\therefore$ NCR = 2 α I_N = 75.0μA

$$I_{N1} = \frac{15+1}{16} \times 75 \times 10^{-6} = 75.0\mu\text{A}$$

$$\omega_{nRN32} = \sqrt{\frac{75 \times 10^{-6} \times 474.5 \times 10^6}{2\pi \times 4 \times 1005 \times 10^{-12}}} = 1.19\text{Mrad / s}$$

$$\zeta_{RN32} = 1000 \times 10^{-12} \times R_F \times 1.19 \times 10^6 \times \frac{75 \times 10^{-6}}{75 \times 10^{-6}}$$

where ζ_{RN32} = 1.0

$$1.0 = 1000 \times 10^{-12} \times R_F \times 1.19 \times 10^6 \times \frac{75 \times 10^{-6}}{75 \times 10^{-6}}$$

$\therefore R_F$ = 820Ω α ζ_{RN32} = 0.9758

(6) 90 Mbps normal gain

from the above ω_{nRN32}

$$\omega_{nRN90} = 1.19 \times 10^6 \times \frac{90 \times 10^6}{32 \times 10^6} = 3.35\text{Mrad / s}$$

$$3.35 \times 10^6 = \sqrt{\frac{I_N \times 803.0 \times 10^6}{2\pi \times 4 \times 1005 \times 10^{-12}}}$$

$\therefore I_N = 353\mu\text{A}$

$$353 \times 10^{-6} = 9.75 \times 10^{-2} \times \frac{\text{NCR} + 1}{3.9 \times 10^3}$$

$\therefore$ NCR = 13, I_N = 350μA,

ω_{nRN90} = 3.34Mrad / s

where $\zeta_{RN90} = 1.0$

$$1.0 = 1000 \times 10^{-12} \times 820 \times 3.34 \times 10^{6} \times \frac{I_{N1}}{350 \times 10^{-6}}$$

$$\therefore I_{N1} = 127.8\mu A$$

$$127.8 \times 10^{-6} = \frac{NDR + 1}{16} \times 350 \times 10^{-6}$$

$$\therefore NDR = 5 \quad \alpha_{N1} = 131.25\mu A$$

$$\zeta_{RN90} = 1000 \times 10^{-12} \times 820 \times 3.34 \times 10^{6} \times \frac{5 + 1}{16}$$

$$\therefore \zeta_{RN90} = 1.027$$

(7) 90 Mbps high gain

$\omega_{nRH90} = 6.88$ Mrad/s

$$6.88 \times 10^{6} = \sqrt{\frac{I_H \times 803.0 \times 10^{6}}{2\pi \times 3 \times 1005 \times 10^{-12}}}$$

$$\therefore I_H = 1.12mA$$

$$1.12 \times 10^{-3} = \frac{HCR + 3}{2} \times 350 \times 10^{-6}$$

$$\therefore HCR = 3 \quad \alpha_H = 1.05mA \quad C$$

$$\omega_{nRH90} = 6.67 Mrad/s$$

where $\zeta_{RH90} = 1.2$

$$1.2 = 1000 \times 10^{-12} \times 820 \times 6.67 \times 10^{6} \times \frac{I_{H1}}{1.05 \times 10^{-3}}$$

$$\therefore I_{H1} = 230.4\mu A$$

$$230.4 \times 10^{-6} = \frac{HDR}{32} \times \left\{(1.05 \times 10^{-3}) - (350 \times 10^{-6})\right\} + 131.25 \times 10^{-6}$$

$$\therefore HDR = 5 \quad \alpha_{H1} = 240.63\mu A$$

$$\zeta_{RH90} = 1000 \times 10^{-12} \times 820 \times 6.67 \times 10^{6} \times \frac{240.63 \times 10^{-6}}{1.05 \times 10^{-3}}$$

$$\therefore \zeta_{RH90} = 1.253$$

(8) 90 Mbps reference gain

where $\omega_{nRR90} = \omega_{nRN90}$

$$3.34 \times 10^{6} = \sqrt{\frac{I_R \times 803.0 \times 10^{6}}{2\pi \times 3 \times 1005 \times 10^{-12}}}$$

$$\therefore I_R = 263.2\mu A$$

$$263.2 \times 10^{-6} = 9.75 \times 10^{-2} \times \frac{NCW + 1}{3.9 \times 10^{3}}$$

$$\therefore NCW = 10 \quad \alpha_R = 275\mu A \quad C$$

$$\omega_{nRR90} = 3.41 Mrad/s$$

where $\zeta_{RR90} = 1.0$

$$1.0 = 1000 \times 10^{-12} \times 820 \times 3.41 \times 10^{6} \times \frac{I_{R1}}{275 \times 10^{-6}}$$

$$\therefore I_{R1} = 98.3\mu A$$

$$98.3 \times 10^{-6} = \frac{NDW + 1}{16} \times 275 \times 10^{-6}$$

$$\therefore NDW = 5 \quad \alpha_{R1} = 103.13\mu A$$

$$\zeta_{RR90} = 1000 \times 10^{-12} \times 820 \times 3.41 \times 10^{6} \times \frac{5 + 1}{16}$$

$$\therefore \zeta_{RR90} = 1.049$$

(9) 64 Mbps normal gain

from the above ω_{nRN32}

$$\zeta_{nRN64} = 1.19 \times 10^{6} \times \frac{64 \times 10^{6}}{32 \times 10^{6}} = 2.38 Mrad/s$$

$$2.38 \times 10^{6} = \sqrt{\frac{I_N \times 678.6 \times 10^{6}}{2\pi \times 4 \times 1005 \times 10^{-12}}}$$

$$\therefore I_N = 210.8\mu A$$

$$210.8 \times 10^{-6} = 9.75 \times 10^{-2} \times \frac{NCR + 1}{3.9 \times 10^{3}}$$

$$\therefore NCR = 7 \quad \alpha_N = 200\mu A \quad C$$

$$\omega_{nRN64} = 2.32 Mrad/s$$

where $\zeta_{RN64} = 1.0$

$$1.0 = 1000 \times 10^{-12} \times 820 \times 2.32 \times 10^{6} \times \frac{I_{N1}}{200 \times 10^{-6}}$$

$$\therefore I_{N1} = 105.1\mu A$$

$$105.1 \times 10^{-6} = \frac{NDR + 1}{16} \times 200 \times 10^{-6}$$

$$\therefore NDR = 7 \quad \alpha_{N1} = 100\mu A$$

$$\zeta_{RN64} = 1000 \times 10^{-12} \times 820 \times 2.32 \times 10^{6} \times \frac{7 + 1}{16}$$

$$\therefore \zeta_{RN64} = 0.9512$$

(10) 64 Mbps high gain

where $\omega_n \cdot T_{aq64} = 3.0$

$$T_{aq64} = \frac{8}{64 \times 10^{6}} \cdot 4.9 \text{ byte} = 613ns$$

(Register setting ; 6.0 bytes)

$\omega_{nRH64} = 4.89$Mrad / s

$$4.89 \times 10^{6} = \sqrt{\frac{I_H \times 678.6 \times 10^{6}}{2\pi \times 3 \times 1005 \times 10^{-12}}}$$

$$\therefore I_H = 668mA$$

$$668 \times 10^{-6} = \frac{HCR + 3}{2} \times 200 \times 10^{-6}$$

$$\therefore HCR = 4 \quad \alpha_H = 700\mu A \quad C$$

$\omega_{nRH64} = 5.01$Mrad / s

where $\zeta_{RH64} = 1.2$

$$1.2 = 1000 \times 10^{-12} \times 820 \times 5.01 \times 10^{6} \times \frac{I_{H1}}{700 \times 10^{-6}}$$

$$\therefore I_{H1} = 204.5\mu A$$

$$204.5 \times 10^{-6} = \frac{HDR}{32} \times \left\{(700 \times 10^{-6}) - (200 \times 10^{-6})\right\} + 100 \times 10^{-6}$$

$$\therefore HDR = 7 \quad \alpha_{H1} = 209.38\mu A$$

$$\zeta_{RH64} = 1000 \times 10^{-12} \times 820 \times 5.01 \times 10^{6} \times \frac{209.38 \times 10^{-6}}{700 \times 10^{-6}}$$

$$\therefore \zeta_{RH64} = 1.229$$

(11) 64 Mbps reference gain

where $\omega_{nRR64} = \omega_{nRN64}$

$$2.32 \times 10^{6} = \sqrt{\frac{I_R \times 678.6 \times 10^{6}}{2\pi \times 3 \times 1005 \times 10^{-12}}}$$

$$\therefore I_R = 150.3\mu A$$

$$150.3 \times 10^{-6} = 9.75 \times 10^{-2} \times \frac{NCW + 1}{3.9 \times 10^{3}}$$

$$\therefore NCW = 5 \quad \alpha_R = 150\mu A \quad C$$

$\omega_{nRR64} = 2.32$Mrad / s

where $\zeta_{RR64} = 1.0$

$$1.0 = 1000 \times 10^{-12} \times 820 \times 2.32 \times 10^{6} \times \frac{I_{R1}}{150 \times 10^{-6}}$$

$$\therefore I_{R1} = 78.8\mu A$$

$$78.8 \times 10^{-6} = \frac{NDW + 1}{16} \times 150 \times 10^{-6}$$

$$\therefore NDW = 7 \quad \alpha_{R1} = 75\mu A$$

$$\zeta_{RR64} = 1000 \times 10^{-12} \times 820 \times 2.32 \times 10^{6} \times \frac{7 + 1}{16}$$

$$\therefore \zeta_{RR64} = 0.9512$$

(12) 32 Mbps normal gain

$\omega_{nRN32} = 1.19$ Mrad/s

NCR = 2, $I_N = 75.0\ \mu A$

NDR = 15, $I_{N1} = 75.0\ \mu A$

$\zeta_{RN32} = 0.9758$

(13) 32 Mbps high gain

$\omega_{nRH32} = 2.45$ Mrad/s

$$\therefore I_H = 239.6\mu A$$

$$239.6 \times 10^{-6} = \frac{HCR + 3}{2} \times 75 \times 10^{-6}$$

$$\therefore HCR = 3 \quad \alpha_H = 255\mu A \quad C$$

$\omega_{nRH32} = 2.37$Mrad / s

where $\zeta_{RH32} = 1.2$

$$1.2 = 1000 \times 10^{-12} \times 820 \times 2.37 \times 10^{6} \times \frac{I_{H1}}{225 \times 10^{-6}}$$

$$\therefore I_{H1} = 138.9\mu A$$

$$138.9 \times 10^{-6} = \frac{HDR}{32} \times \left\{(225 \times 10^{-6}) - (75 \times 10^{-6})\right\} + 75 \times 10^{-6}$$

$$\therefore HDR = 14 \quad \alpha_{N1} = 140.63\mu A$$

$$\zeta_{RH32} = 1000 \times 10^{-12} \times 820 \times 2.37 \times 10^{6} \times \frac{140.63 \times 10^{-6}}{225 \times 10^{-6}}$$

$$\therefore \zeta_{RH32} = 1.215$$

(14) 32 Mbps reference gain

where $\omega_{nRR32} = \omega_{nRN32}$

$$1.19 \times 10^{6} = \sqrt{\frac{I_R \times 474.5 \times 10^{6}}{2\pi \times 3 \times 1005 \times 10^{-12}}}$$

$$\therefore I_R = 56.5\mu A$$

$$56.5 \times 10^{-6} = 9.75 \times 10^{-2} \times \frac{NCW + 1}{3.9 \times 10^{3}}$$

$$\therefore NCW = 1 \quad \alpha_R = 50\mu A \quad C$$

$$\omega_{nRR32} = 1.12 Mrad / s$$

$$1.0 = 1000 \times 10^{-12} \times 820 \times 1.12 \times 10^{6} \times \frac{I_{R1}}{50 \times 10^{-6}}$$

$$\therefore I_{R1} = 54.4\mu A$$

$$54.4 \times 10^{-6} = \frac{NDW + 1}{16} \times 50 \times 10^{-6}$$

$$\therefore NDW = 15 \quad \alpha_{R1} = 50\mu A$$

$$\zeta_{RR32} = 1000 \times 10^{-12} \times 820 \times 1.12 \times 10^{6} \times \frac{15 + 1}{16}$$

$$\therefore \zeta_{RR32} = 0.9184$$

where $\zeta_{RR32} = 1.0$

Sync Field Detection

By using an internal counter to the transition (24 or 32 pulses), the HD153044TF RD-PLL can operate in the high-gain mode immediatly after RG is asserted, then automatically switched over to the normal-gain mode after the counter counts 24 or 32

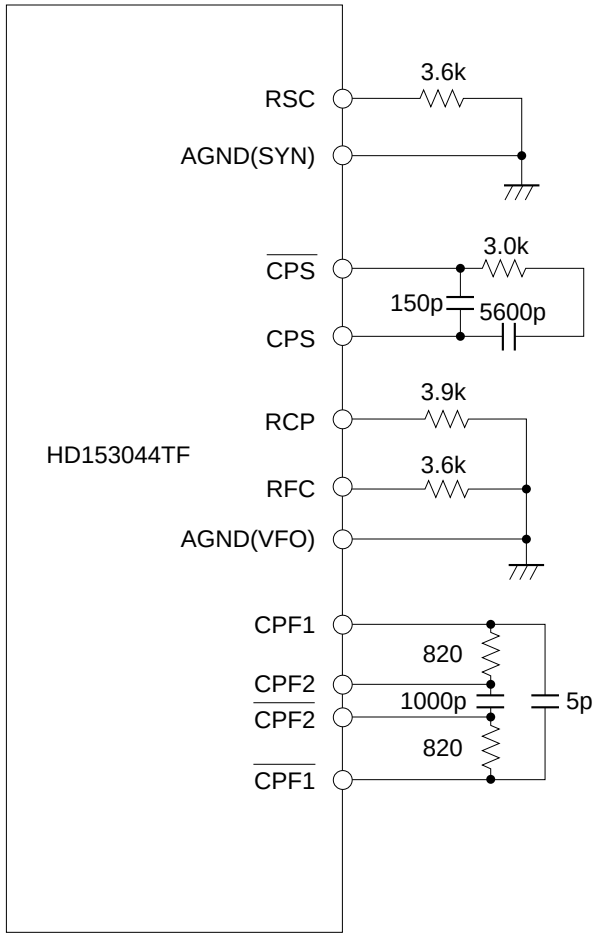
transitions (4×6 or 4×8).
It is recommended that the sync field should be of 3T pattern, and that a minimum of “6-NRZ-byte” period is allowed for proper RD-PLL phase locking.

Figure 14 Sync Field Detection Timing

Read and Write Mode

Figure 15 Read and Write Mode Timing

Example of External Components Connected to the R-PLL & W-PLL



Unit R: Ω
C: F

Calculation of PLL Constants

1. Encode Clock Generator's Frequency Synthesizer (W-PLL)

1. VCO center frequency f_{CW}

(1-1)

where $22 \leq L \leq 63$ (L : VFC register value)

2. VCO oscillation frequency f_{OW}

(1-2)

where $4 \leq M \leq 255$ (M : PSM register value)
where $4 \leq N \leq 255$ (N : PSN register value)
fosc : Oscclk's input frequency

3. VCO gain K_{OW}

(1-3)

where $22 \leq L \leq 63$ (L : VFC register value)

4. Charge pump current I_W

(1-4)

where $0 \leq NCS \leq 15$ (NCS : NCS register value)

5. Characteristics frequency ω_{nW}

(1-5)

where $4 \leq N \leq 255$ (N : PSN register value)

6. Attenuation ζ_W

(1-6)

2. Decode Clock Generator's VFO

1. VCO center frequency f_{CR}

(2-1)

where $22 \leq L \leq 63$ (L : VFC register value)

2. VCO gain K_{OR}

(2-2)

where $22 \leq L \leq 63$ (L : VFC register value)

3. Charge pump normal gain current I_N, I_{N1}

(2-3)

where $0 \leq NCR \leq 15$ (NCR : NCR register value)

(2-4)

where $0 \leq NDR \leq 15$ (NDR : NDR register value)

4. Charge pump high gain current I_H, I_{H1}

(2-5)

where $0 \leq HCR \leq 15$ (HCR : HCR register value)

(2-6)

where $0 \leq HDR \leq 15$ (HDR : HDR register value)

5. Charge pump reference gain current I_R, I_{R1}

(2-7)

where $0 \leq NCW \leq 15$ (NCW : NCW register value)

(2-8)

where $0 \leq NDW \leq 15$ (NDW : NDW register value)

6. Characteristic frequency (high gain) ω_{nRH}

(2-9)

7. Characteristic frequency (normal gain) ω_{nRN}

(2-10)

8. Characteristic frequency (reference gain) ω_{nRR}

(2-11)

9. Attenuation (high gain) ζ_{RH}

(2-12)

10. Attenuation (normal gain) ζ_{RN}

(2-13)

11. Attenuation (reference gain) ζ_{RR}

(2-14)

Calculation Example of HD153044TF W-PLL Constants

Transfer rate ; 90 Mbps, 64 Mbps, 32 Mbps 3 zones

(1) R_{SC} = 3.6 k
VCO center frequency = 135 MHz (L = 63)

(2) PSM register, PSN register (M, N)

where fosc = 20 MHz,
Transfer rate resolution = 0.5 Mbps

(3) C_{S1}, C_{S2} (calculate from max. transfer rate)

where I_W = max. (NCS = 15)

where calculate VCO gain from L

(4) R_S (calculate from max. transfer rate)
where $\zeta_{W90} = 1.0$

(5) 64 Mbps

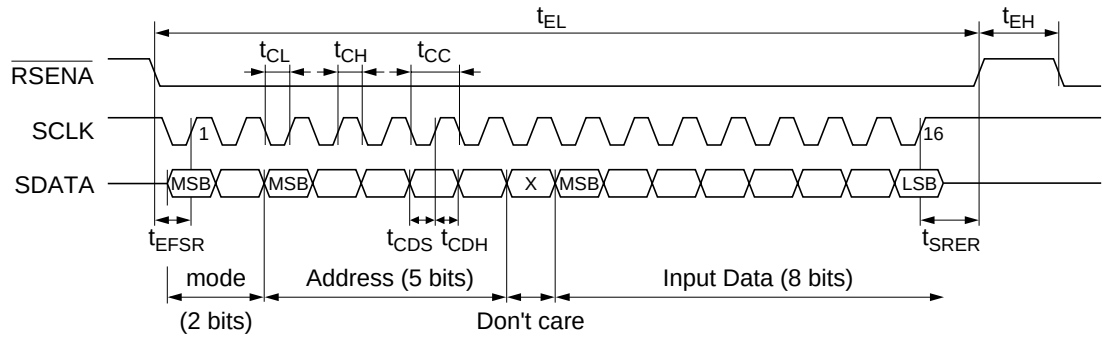
where calculate VCO gain from L

where $\omega_{nW90} = \omega_{nW64}$

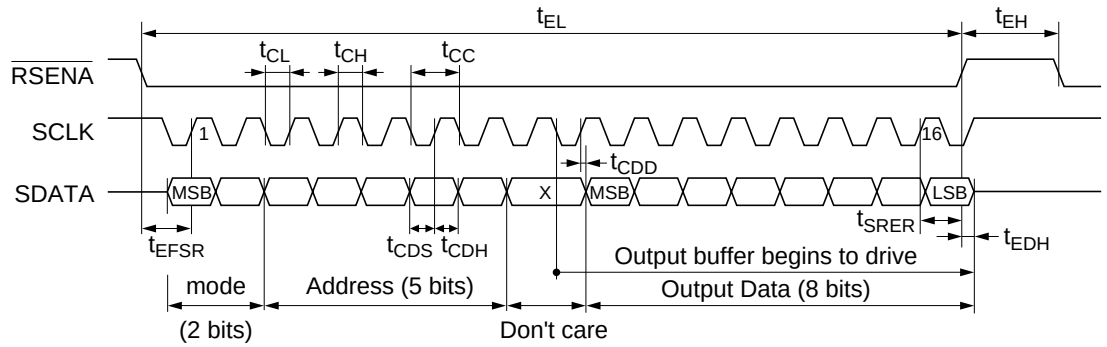
AC Timing Chart

(1) Register Read / Write

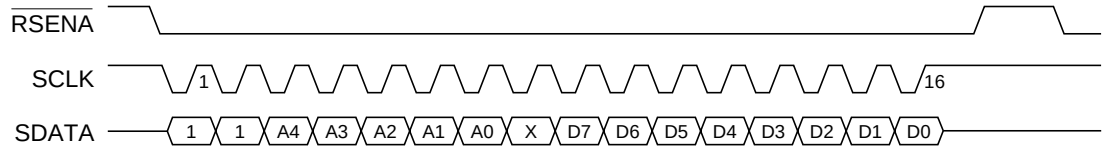
⟨Write⟩



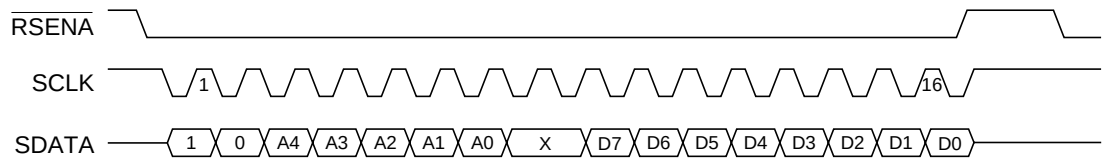
⟨Read⟩



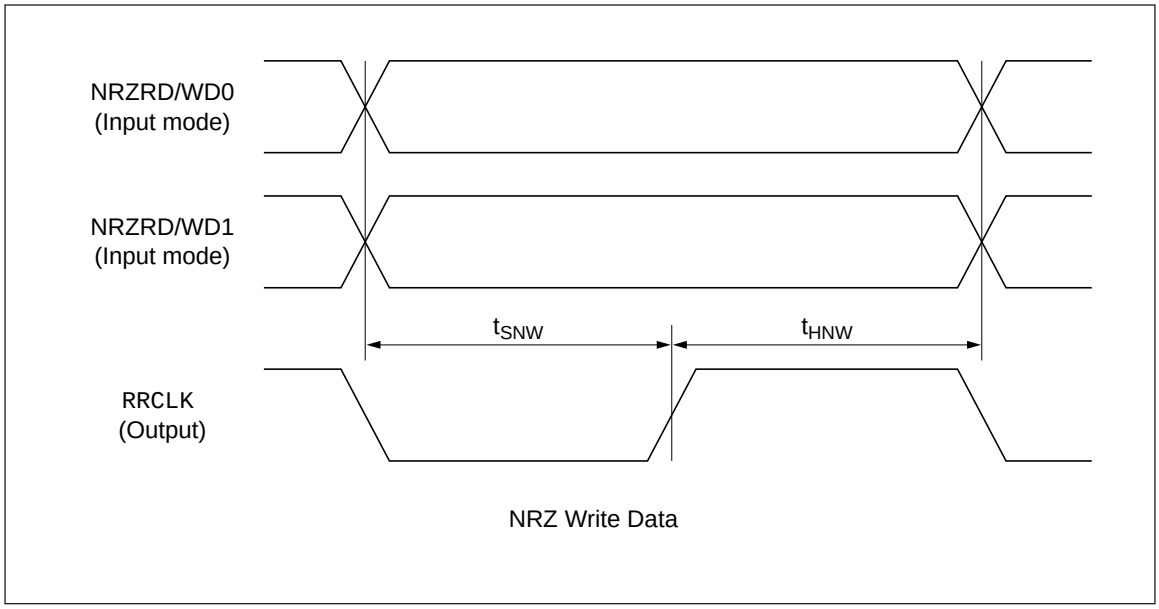
Write to Register



Read from Register

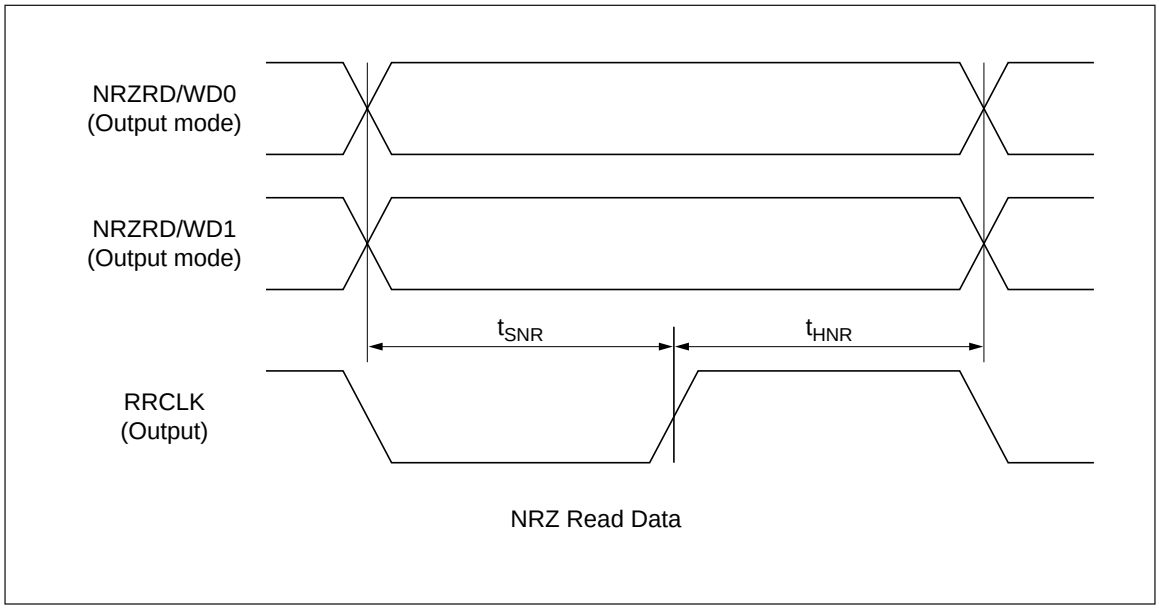


(2) Write for NRZ Data



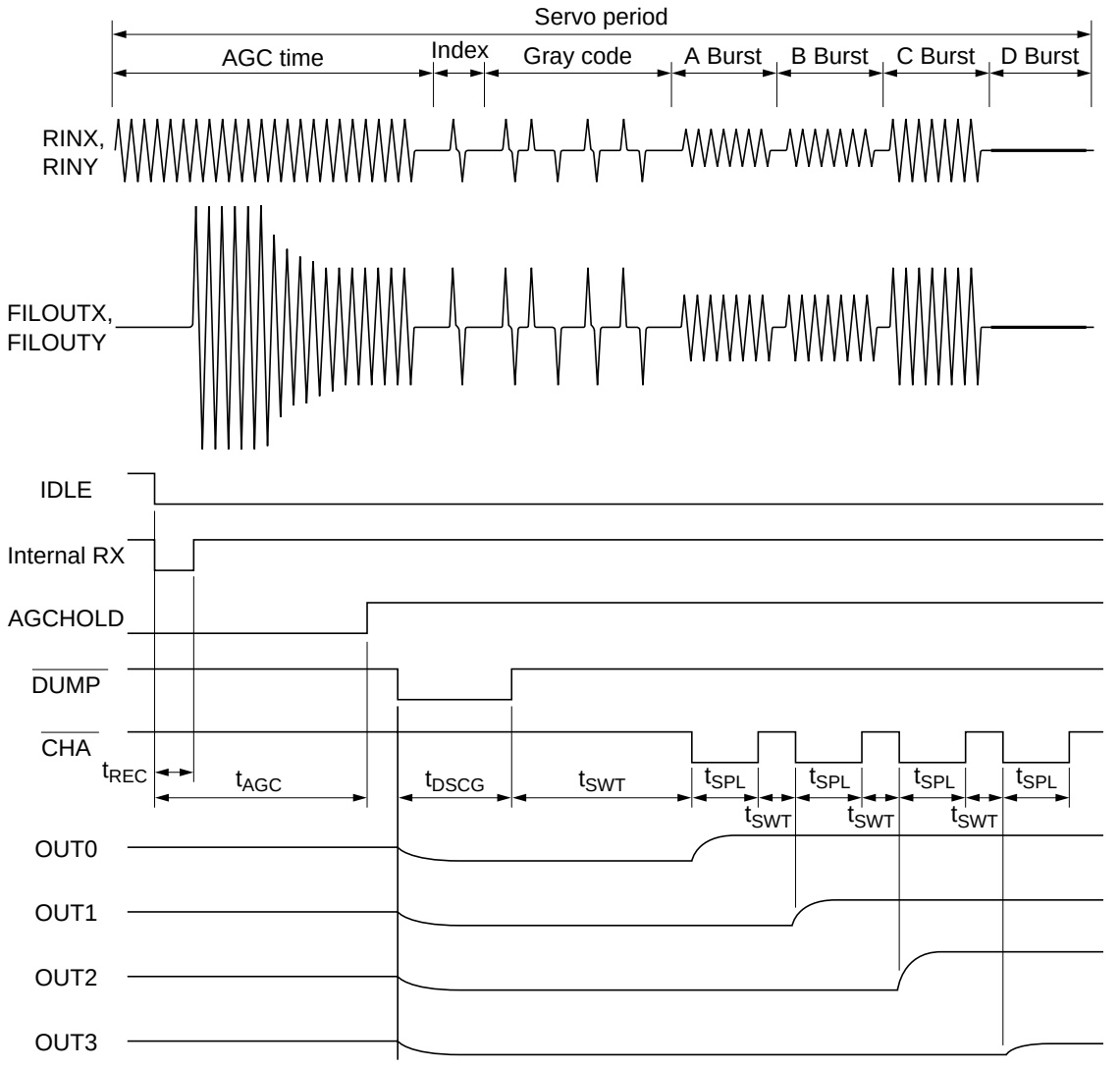
NRZ Write Data

(3) Read for NRZ Data



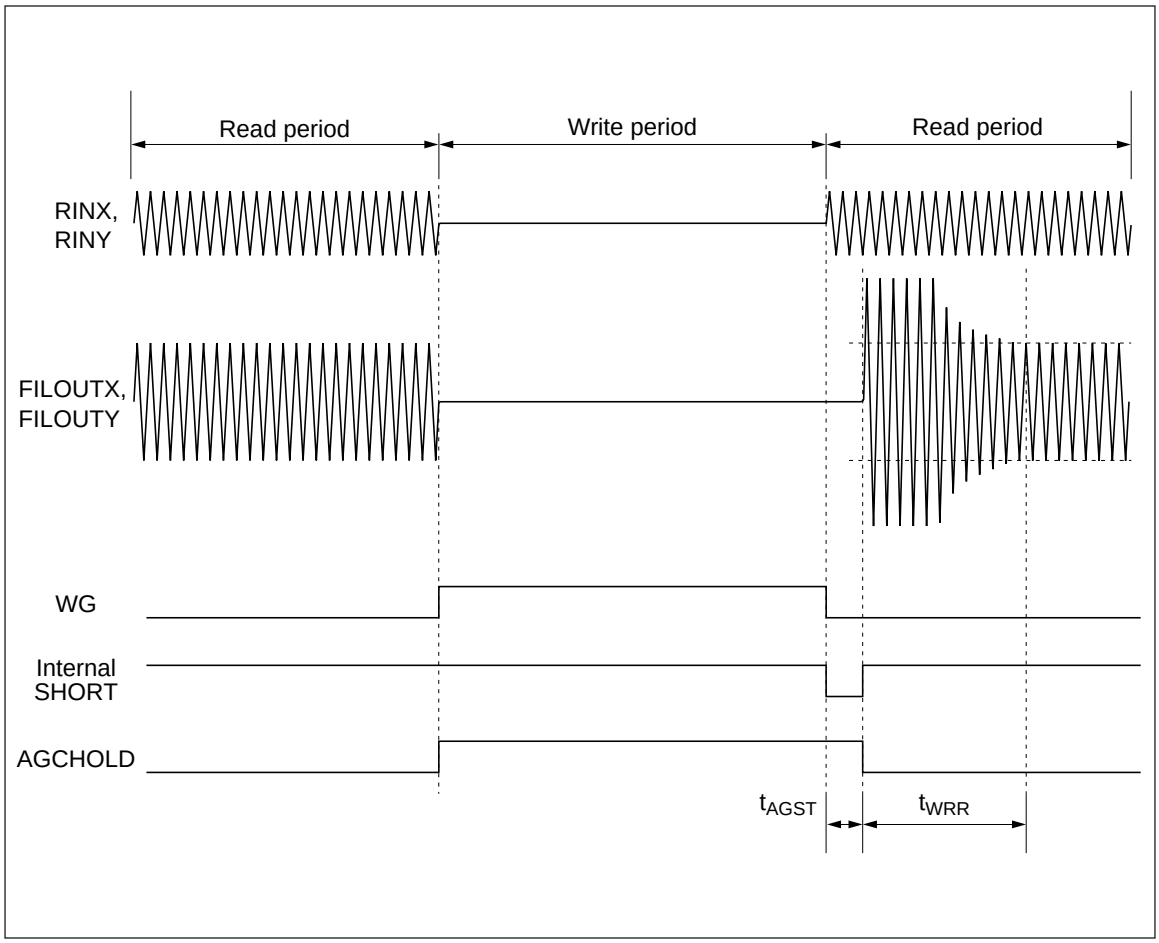
NRZ Read Data

Example of The Idle to Servo Mode Waveform



During D Burst, no signal coming out.

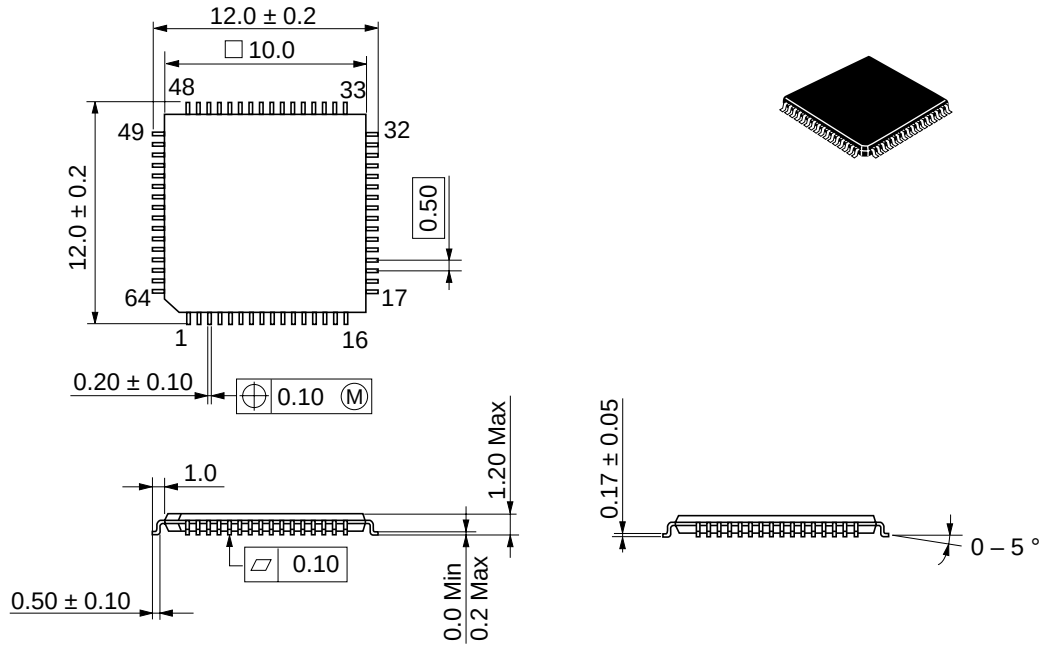
Example of The Write to Read Mode Waveform



Timing Diagram of Write to Read Function

Package Dimensions

Unit: mm



Hitachi Code	TFP-64B
EIAJ	—
JEDEC	—

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