PDSP16330/A/B

Pythagoras Processor

Supersedes version September 1996, DS3884 - 1.3

DS3884 - 2.1 November 1998

The PDSP16330 is a high speed digital CMOS IC that converts Cartesian data (Real and Imaginary) into Polar form (Magnitude and Phase), at rates up to 20MHz. Cartesian 16+16 bit 2's complement or Sign-Magnitude data is converted into 16 bit Phase format. The Magnitude output may be scaled in amplitude by powers of 2. The Phase output represents a full 2 x π field to eliminate phase ambiguities.

Polyimide is used as an inter-layer dielectric and as glassivation.

The PDSP16330 is offered in three speed grades: a basic 10MHz part (PDSP16330), a 20MHz version (PDSP16330A) and a 25MHz version (PDSP16330). A MIL-STD-883 version is also detailed in a separate datasheet.

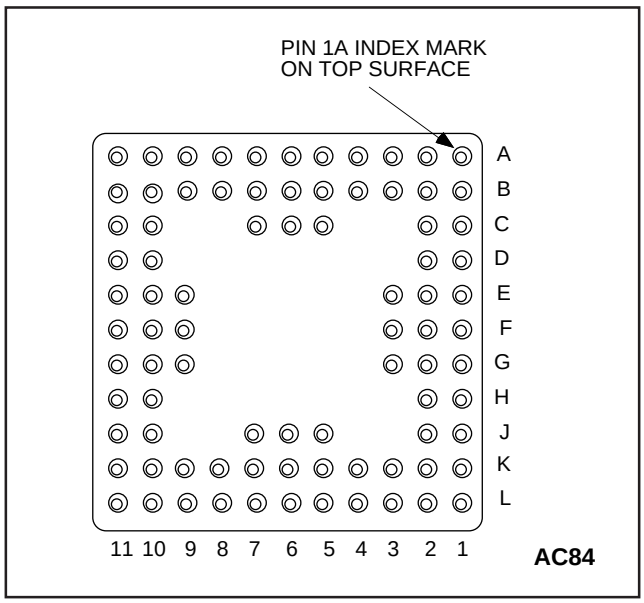


Fig.1 Pin connections - bottom view (PGA)

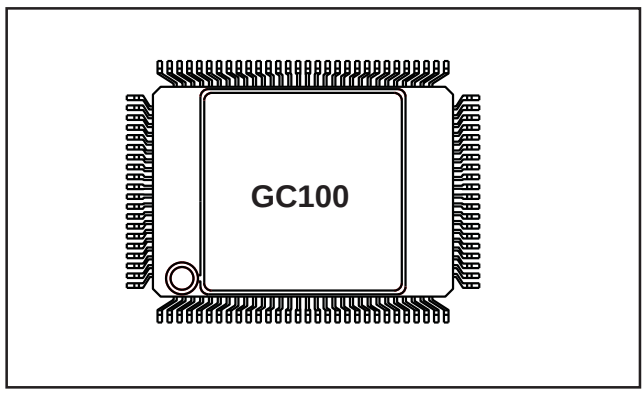


Fig.2 Pin connections - QFP Package

FEATURES

- 25MHz Cartesian to Polar Conversion
- 16-Bit Cartesian Inputs
- 16-Bit Magnitude Output
- 12-Bit Phase Output
- 2's Complement or Sign-Magnitude Input Formats
- Three-state Outputs and Independent Data Enables Simplify System Interfacing
- Magnitude Scaling Facility with Overflow Flag
- Less than 400 mW Power Dissipation at 10MHz
- 84-pin PGA or 100 pin QFP Package or 84 LCC

APPLICATIONS

- Digital Signal Processing
- Digital Radio
- Radar Processing
- Sonar Processing
- Robotics

ORDERING INFORMATION

Commercial (0°C to +70°C)

PDSP16330A CO AC	(20MHZ - PGA Package)
PDSP16330B CO AC	(25MHZ - PGA Package)

Industrial (-40°C to +85°C)

PDSP16330A BO AC	20MHZ - PGA Package
PDSP16330A/IG/GC1R	20MHZ - GC Package
PDSP16330B BO AC	25MHZ - PGA Package

Military (-55°C to +125°C)

PDSP16330A AO AC	20MHZ - PGA Package
PDSP16330/MC/GC1R	10MHz - GC Package Mil 883C Screened

ASSOCIATED PPODUCTS

PDSP16112	16 X 12 Complex Multiplier
PDSP16116	16 X 16 Complex Multiplier
PDSP16318	Complex Accumulator
PDSP16350	I/Q Splitter and NCO
PDSP16510A	Stand Alone FFT Processor

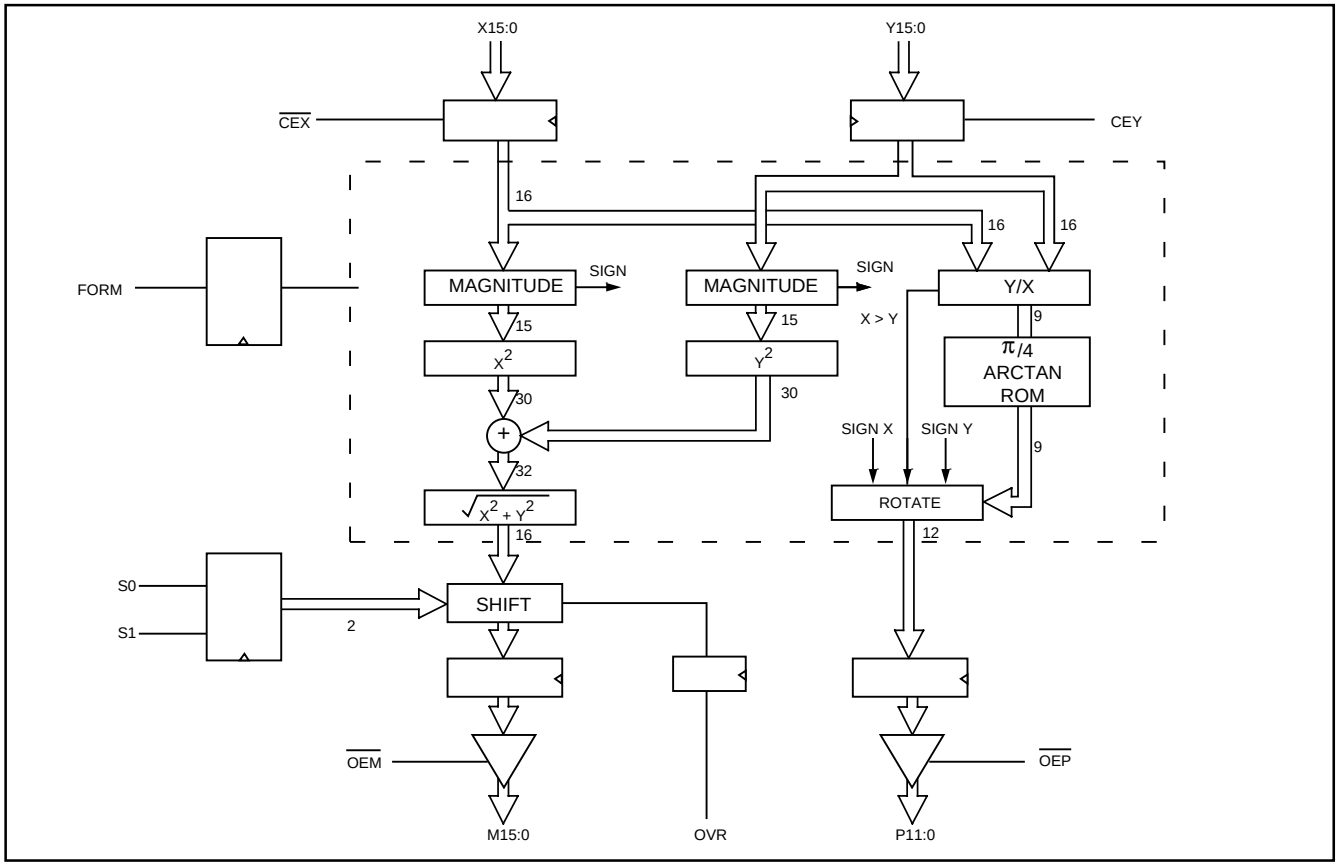


Fig.2 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16330 converts incoming Cartesian Data into the equivalent Polar Values. The device accepts new 16 + 16 bit complex data every cycle, and delivers a 16 bit + 12 bit Polar equivalent after 24 clock cycles.The input data can be in 2s' Complement or Sign Magnitude format selected via the FORM input. The output is in a magnitude format for both the Magnitude output and the Phase. Phase data is zero for data with a zero Y input and positive X, and is 400 hex for zero X data and positive Y, is 800 hex for zero Y data and negative X, and is C00 hex for zero X and negative Y. The LSB weighting (bit 0) is 2 x π/4096 radians. The 16 bit Magnitude result may be scaled by shifting one, two, or three places in the more significant direction, effectively multiplying the Magnitude result by 2,4 or 8 respectively. Any of these shifts can under certain conditions cause an invalid result to be output from the device. Under these circumstances the OVR output will become active. The PDSP16330 has independent clock enables and three state output controls for all ports.

FORM

This input selects the format of the X and Y input data**.** A low level on FORM indlcates that the Input data is twos' complement format (Note: input data 8000 hex is not valid in 2s' complement mode). This input refers to the format of the current Input data and may be changed on a per cycle basis if desired. The level of FORM is latched at the same time as the data to which it refers.

S1-0

These inputs select the scaling factor to be applied to the Magnitude output. They are latched by the rising edge of CLK and determine the scaling of the output in the cycle after they are loaded into the device. The scale factor applied is determined by the table. Should the scaling factor applied cause an invalid Magnitude result to be output on the M Port, then the OVR Flag will become active for the period that the M Port output is invalid.

S1	S0	Scaling Factor
0	0	x1
0	1	x2
1	0	x4
1	1	x8

The output number range is from 0 to 2 when the scaling factor is set at x1.

PIN DESCRIPTIONS

Symbol	Pin Name and Description
CLK	**Clock:** Common Clock to device Registers. Register contents change on the rising edge of clock. Both pins must be connected.
$\overline{CEX}$	**Clock Enable:** Clock Enable for X Port. The clock to the X port is enabled by a low level.
$\overline{CEY}$	**Clock Enable:** Clock Enable for Y Port The clock to the Y port is enabled by a low level.
X15-X0	**X Data Input** Data presented to this input is loaded into the device by the rising edge of CLK. X15 is the MSB
Y15-Y0	**Y Data Input** Data presented to this input is loaded into the device by the rising edge of CLK. Y15 is the MSB
M15-M0	**M Data Output:** Magnitude data generated by the device is output on this port. Data changes on the rising edge of CLK, M15 is the MSB. The weighting of M15 is determined by the Scale factor selected .
P11-P0	**P Data Output:** Phase data generated by the device is output on this port. Data changes on the rising edge of CLK, P11 is the MSB. The weighting of P11 is π radians.
$\overline{OEM}$	**Output Enable:** Output Enable for M Port. The M Port is in a high impedance state when this input is high.
$\overline{OEP}$	**Output Enable:** Output Enable for P Port. The P Port is in a high impedance state when this input is high.
FORM	**Format Select** This input selects the format of the Cartesian Data input on the X and Y ports. This input is latched by the rising edge of CLK, and is applied at the same time as the data to which it refers. A low !evel indicates that two's complement data is applied, a high indicates Sign-Magnitude
S1-S0	**Scaling Control:** Control input for scaling of Magnitude Data. This input is latched by the rising edge of CLK, and determines the scaling to be applied to the Magnitude result. The Scaling is applied to the output data in the cycle following the cycle in which the control was latched.
OVR	**Overflow:** Overflow flag. This signal becomes active if the scaling currently selected causes an invalid value to be presented to the Magnitude output.
Vcc	+**5V supply.** All Vcc pins must be connected.
GND	**0V supply.** All GND pins must be connected.

INPUT DATA RANGE

2's Complement	Sign Magnitude
7FFF	7FFF
.	.
.	.
.	.
0001	0001
0000	0000
FFFF	8000
.	.
.	.
.	.
8001	FFF

PIN FUNCTION

Pin No. AC	GC	Function	Pin No. AC	GC	Function	Pin No. AC	GC	Function
F3	91	M7	L9	23	YO	A9	59	X1
G3	92	M6	L10	24	$\overline{CEY}$	B8	60	X2
G1	93	M5	K9	25	CLK	A8	61	X3
G2	94	M4	L11	26	Vcc	B6	62	X4
F1	95	M3	K10	31	GND	B7	63	X5
H1	96	M2	J10	32	GND	A7	64	X6
H2	97	M1	K11	33	GND	C7	65	X7
J1	98	M0	J11	34	GND	C6	66	X8
K1	99	S0	H10	35	GND	A6	67	X9
J2	100	S1	H11	36	GND	A5	68	X10
L1	1	GND	F10	37	GND	B5	69	X11
K2	6	Vcc	G10	38	$\overline{OEP}$	C5	70	X12
K3	7	FORM	G11	39	P0	A4	71	X13
L2	8	Y15	G9	40	P1	B4	72	X14
L3	9	Y14	F9	41	P2	A3	73	X15
K4	10	Y13	F11	42	P3	A2	74	CLK
L4	11	Y12	E11	43	P4	B3	75	OVR
J5	12	Y11	E10	44	P5	A1	76	Vcc
K5	13	Y10	E9	45	P6	B2	81	GND
L5	14	Y9	D11	46	P7	C2	82	$\overline{OEM}$
K6	15	Y8	D10	47	P8	B1	83	M15
J6	16	Y7	C11	48	P9	C1	84	M14
J7	17	Y6	B11	49	P10	D2	85	M13
L7	18	Y5	C10	50	P11	D1	86	M12
K7	19	Y4	A11	51	GND	E3	87	M11
L6	20	Y3	B10	52	Vcc	E2	88	M10
L8	21	Y2	B9	57	$\overline{CEX}$	E1	89	M9
K8	22	Y1	A10	58	X0	F2	90	M8

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} (Commercial) = 0°C to + 70°C, T_{amb} (Industrial) = -40°C to + 85°C
V_{cc} (Commercial) = 5.0V $\pm$ 5%, V_{cc} (Industrial and Military) = 5.0V $\pm$ 1%, GND = 0V

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Sub-group	Conditions
		Min.	Typ.	Max.			
* Output high voltage	V_{OH}	2.4			V	1,2,3	IOH = 3.2mA
* Output low voltage	V_{OL}			0.6	V	1,2,3	IOL=-3.2mA
* Input high voltage (CMOS)	V_{IH}	3.0			V	1,2,3	Inputs $\overline{CEX}$, $\overline{CEY}$ and CLK only
* Input low voltage (CMOS)	V_{IL}			1.0	V	1,2,3	Inputs $\overline{CEX}$, $\overline{CEY}$ and CLK only
* Input high voltage (TTL)	V_{IH}	2.2			V	1,2,3	All other inputs
* Input low voltage (TTL)	V_{IL}			0.8	V	1,2,3	All other inputs
* Input leakage current (Note 1)	I_{IL}	-10		+ 120	µA	1,2,3	GND $\leq V_{IN} \leq V_{CC}$
† Input capacitance	C_{IN}		10		pF		
* Output leakage current	I_{oz}	-50		+ 50	µA	1,2,3	GND $\leq V_{IN} \leq V_{CC}$
† Output SC current	I_{OS}	-50		230	mA		V_{cc} = Max

NOTES
1. All inputs except clock inputs have high value pull-down resistors
2. All parameters marked * are tested during production. Parameters marked † are guaranteed by design and characterisation.

SWITCHING CHARACTERISTICS

	Characteristic	Value						Units	Conditions
		PDSP16330		PDSP16330A		PDSP16330B			
		Min.	Max.	Min.	Max.	Min.	Max.		
†	Input data setup to clock rising edge	15		12		12		ns	
†	Input data Hold after clock rising edge	2		2		2		ns	
†	$\overline{CEX}$, $\overline{CEY}$ Setup to clock rising edge	30		12		12		ns	
†	$\overline{CEX}$, $\overline{CEY}$ Hold aher clock rising edge	0		0		0		ns	
†	FORM, S1:0 Setup to clock rising edge	15		12		12		ns	
†	FORM, S1:0 Hold after clock rising edge	7		2		2		ns	
†	Clock rising edge to valid data	5	40	5	25	5	25	ns	2 x LSTTL + 20pF
*	Clock period	100		50		40		ns	
†	Clock high time	25		15		15		ns	
†	Clock low time	25		15		15		ns	
†	Latency	24	24	24	24	24	24	cycles	
†	$\overline{OEM}$, $\overline{OEP}$ low to data high data valid		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ low to data low data valid		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ high to data high impedance		30		25	25		ns	2 x LSTTL + 20pF
†	$\overline{OEM}$, $\overline{OEP}$ low to data high impedance		30		25	25		ns	2 x LSTTL + 20pF
†	Vcc current (TTL input levels)		110		180	225		mA	V_{CC} = Max Outputs unloaded Clock freq. = Max
†	Vcc current (CMOS input levels)		70		120	150		mA	V_{CC} = Max Outputs unloaded Clock freq. = Max

NOTES
1. LSTTL is equivalent to I_{OH} = 20µA, I_{OL} = -0.4mA
2. Current is defined as negative into the device
3. CMOS input levels are defined as: $V_{IH} = V_{DD}$ - 0.5V, V_{IL} = +0.5V
4. All parameters marked * are tested during production.
   Parameters marked † are guaranteed by design and characterisation.
5. All timings are dependent on silicon speed. This speed is tested by measuring clock period.
   This guarantees all other timings by characterisation and design.

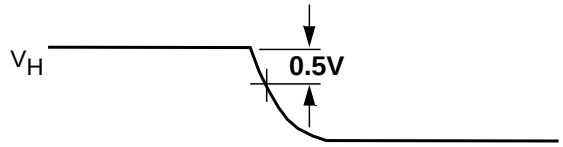
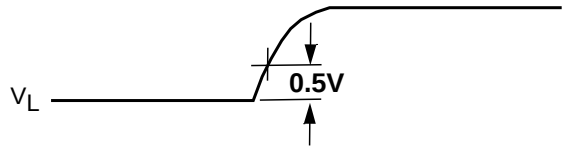
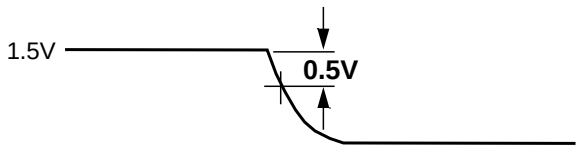
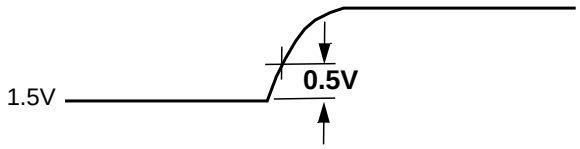
ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{cc}	-0.5V to + 7.0V
Input voltage, V_{IN}	-0.5V to VCC + 0.5V
Output voltage, V_{our}	-0.5V to VCC + 0.5V
Clamp diode current per pin, I_K (see Note 2)	±18mA
Static discharge voltage (HMB), V_{STAT}	500V
Storage temperature. T_{stg}	-65°C to + 150°C
Ambient temperature with power applied T_{amb}:	
Commercial	0°C to + 70°C
Industrial	-40°C to + 85°C
Military	-55 °C to + 125°C
Package power dissipation P_{TOT}	1200mW
Junction temperature	150°C

THERMAL CHARACTERISTICS

Package Type	θ_{JC}°C/W	θ_{JA}°C/W
AC	12	36
GC	12	35

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operatlon under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded; only one output to be tested at any one time.
3. Exposure to Absoulte Maximum Ratings for extended periods may affect device reliability.

Test	Waveform - measurement level
Delay from ouput high to output high impedance	
Delay from ouput low to output high impedance	
Delay from ouput high impedance to Output low	
Delay from ouput high impedance to Output high	

NOTES
1. V_H - Voltage reached when output driven high
2. V_L - Voltage reached when output driven low

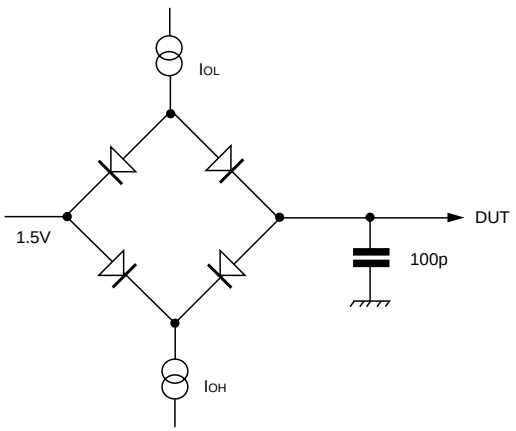
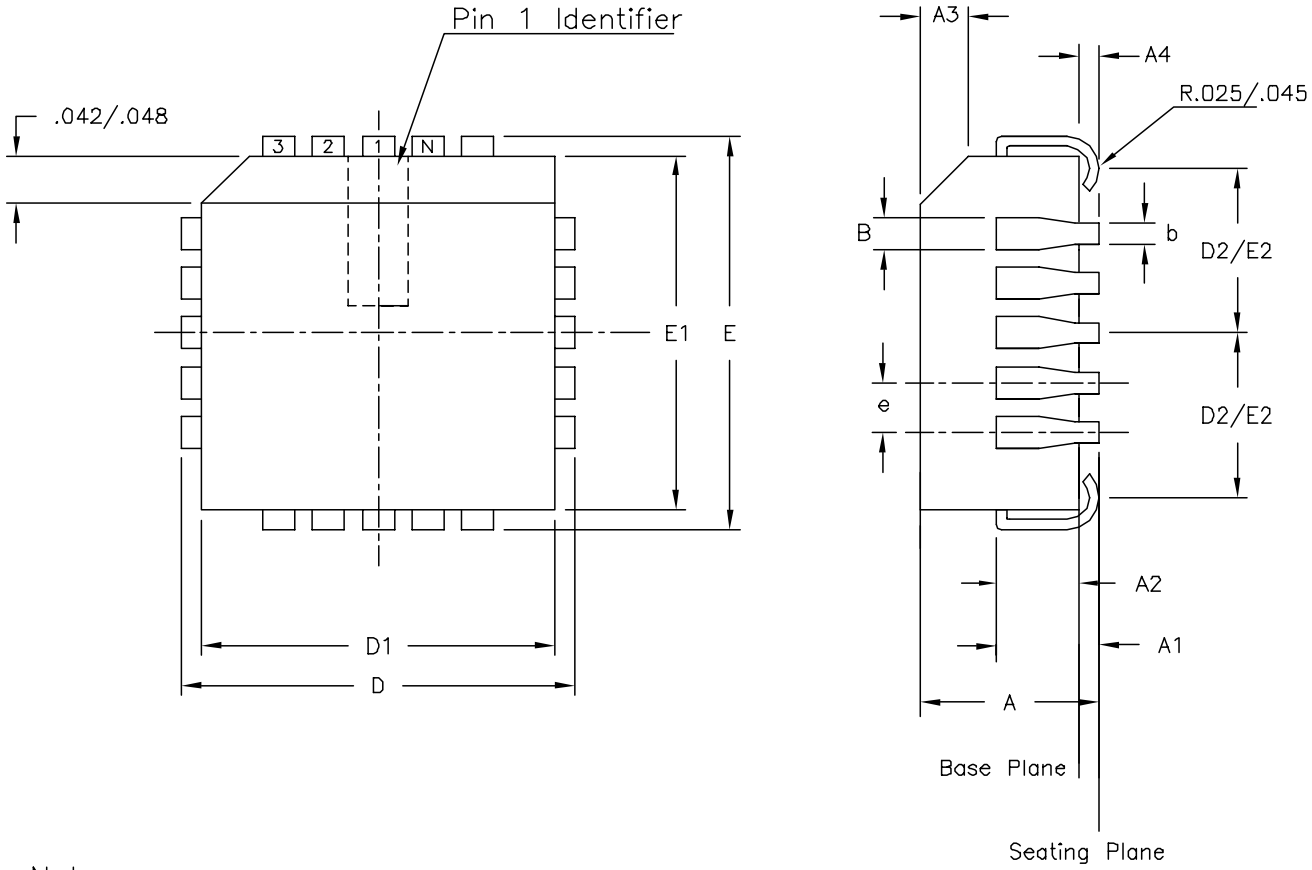


Fig.3 Three state delay measurement load



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.059	0.080	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	1.185	1.195	30.10	30.35
D1	1.150	1.158	29.21	29.41
D2	0.541	0.569	13.74	14.45
E	1.185	1.195	30.10	30.35
E1	1.150	1.158	29.21	29.41
E2	0.541	0.569	13.74	14.45
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	21			
NE	21			
N	84			
Note	Square			
Conforms to JEDEC MS-018AF Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2			
ACN	5958	207471			
DATE	15AUG94	10SEP99			
APPD.					

MITEL SEMICONDUCTOR

Title: Package Outline for 84 Lead PLCC

Drawing Number

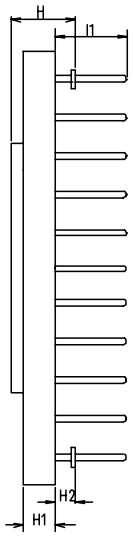
GPD00006

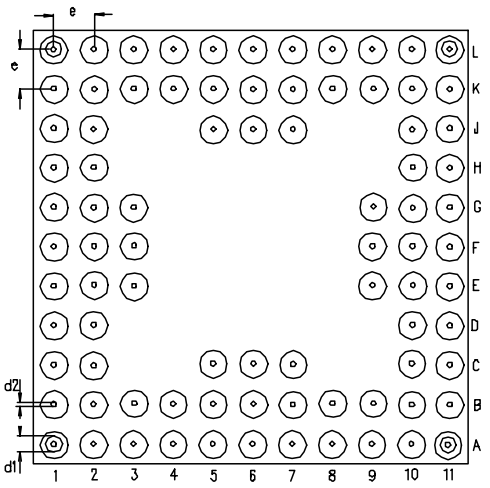
ORIGINATING SITE: Swindon

BOND PAD NUMBER	Goes to Pin No. on Matrix	
1	B	2
2	C	2
3	B	1
4	C	1
5	D	2
6	D	1
7	E	3
8	E	2
9	E	1
10	F	2
11	F	3
12	G	3
13	G	1
14	G	2
15	F	1
16	H	1
17	H	2
18	J	1
19	K	1
20	J	2
21	L	1
22	K	2
23	K	3
24	L	2
25	L	3
26	K	4
27	L	4
28	J	5
29	K	5
30	L	5

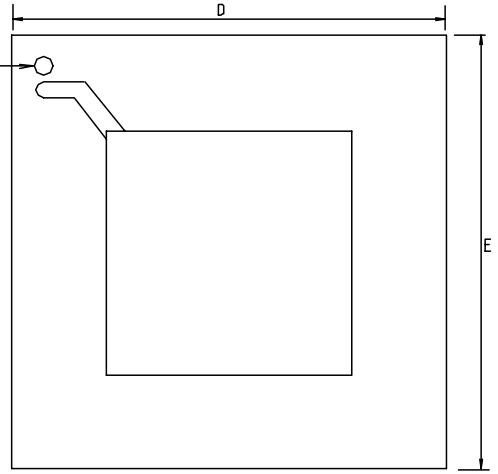
BOND PAD NUMBER	Goes to Pin No. on Matrix	
31	K	6
32	J	6
33	J	7
34	L	7
35	K	7
36	L	6
37	L	8
38	K	8
39	L	9
40	L	10
41	K	9
42	L	11
43	K	10
44	J	10
45	K	11
46	J	11
47	H	10
48	H	11
49	F	10
50	G	10
51	G	11
52	G	9
53	F	9
54	F	11
55	E	11
56	E	10
57	E	9
58	D	11
59	D	10
60	C	11

BOND PAD NUMBER	Goes to Pin No. on Matrix	
61	B	11
62	C	10
63	A	11
64	B	10
65	B	9
66	A	10
67	A	9
68	B	8
69	A	8
70	B	6
71	B	7
72	A	7
73	C	7
74	C	6
75	A	6
76	A	5
77	B	5
78	C	5
79	A	4
80	B	4
81	A	3
82	A	2
83	B	3
84	A	1





Symbol	Altern. Dimensions in millimetres			Control Dimensions in inches	
	MIN	MAX		MIN	MAX
H	3.35	4.14		0.132	0.163
H1	1.93	2.39		0.076	0.094
H2	1.14	1.40		0.045	0.055
D	27.64	28.24		1.088	1.112
D1	1.14	1.40		0.045	0.055
D2	0.41	0.51		0.016	0.020
E	27.64	28.24		1.088	1.112
e	2.54			0.100	
I1	4.45	4.70		0.175	0.185
	Pin features				
N	84				
ND	---				
NE	---				
NOTE	---				



NOTES:

1 GOLD PLATING 60U INCHES MIN THICKNESS OVER 100U INCHES NOMINAL THICKNESS OF NICKEL UNLESS OTHERWISE SPECIFIED IN PURCHASE ORDER

2 LEAD RESISTANCE:
PIN NO. 11,32,53,74--0.250 MAX.
ALL OTHERS-------0.50 MAX.

3 SEAL RING & DIE ATTACH METALLIZED AREAS TO BE FLOATING

4 INDEX MARK INDICATES A1 REF CORNER & CAN BE ANY SHAPE

5 PLATING BARS CAN APPEAR IN VARIOUS POSITIONS & SHOULD NOT BE USED FOR ORIENTATION PURPOSES

6 This drawing supersedes 418/ED/39506/002 issue 3

ORIGINATING SITE: Swindon

ISSUE	1				
ACN	207473				
DATE	13SEP99				
APPRD.					

MITEL SEMICONDUCTOR

Title: Outline Drawing for 84 PGA (AC)

Drawing Number
GPD00603

http://www.mitelsemi.com

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Preliminary and Advance Data/Information: Some datasheets carry the designation “Preliminary” or “Advance”. Preliminary Information represents the design objective for a device type in development and may be revised without notice before the device reaches production. Advance Information is intended for design guidance purposes and refers to a device type in early production where device characterization is ongoing and information is still subject to change without notice. Current information on the status of Preliminary or Advance programs may be obtained from Mitel Sales Offices, Representatives or Distributors.