

41MF2

Quad Differential Line Receiver

Features

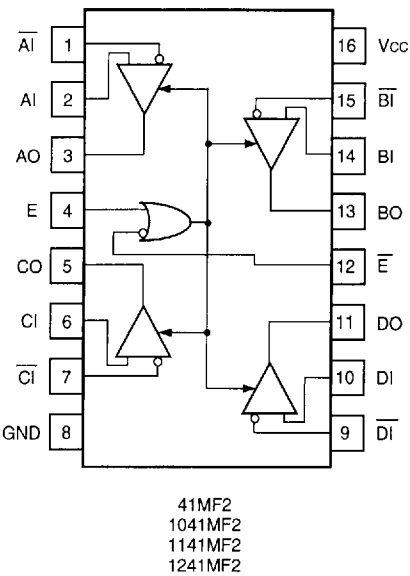
- 1000 V CDM and 1000 V HBM input ESD rating
- Pin-equivalent to the general-trade 26LS32 device, with improved speed, reduced power consumption, and significantly lower levels of EMI
- High input impedance $\approx 8\text{ k}\Omega$
- Four line receivers per package
- Meets ESDI standards
- 5 ns maximum propagation delay
- Single 5.0 V supply
- Operating temperature range: 0 °C to 85 °C
- 200 Mbits/s or 320 Mbits/s maximum data rate when used with the 41Lx or 41Mx drivers respectively
- 220 mW maximum power dissipation
- 0.20 V input sensitivity (typical)
- -1.0 V to +7.2 V common-mode range
- Output defaults to logic 1 when inputs are left open

Description

The 41MF2 Quad Differential Line Receiver integrated circuits receive digital data over balanced transmission lines. These receivers translate differential input logic levels to TTL output logic levels. The 41MF2 offers improved ESD performance over the 41MF device. These devices are pin equivalent to the general-trade 26LS32 device, but offer improved speed and reduced power consumption and significantly lower levels of electromagnetic interference (EMI). These devices have four receivers with a common enable control, and are compatible with the AT&T 41 Series line drivers and transceivers.

The packaging options that are available for the quad differential line receivers include a 16-pin DIP (41MF2), a 16-pin J-lead SOJ (1041MF2), a 16-pin gull-wing SOIC (1141MF2), and a 16-pin narrow-body gull-wing SOIC (1241MF2).

Pin Information



12-2248C

Note The device is disabled when E = 0 and E = 1

Figure 4-6. 41MF2 Logic Diagram

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	Vcc	—	7.0	V
Ambient Operating Temperature	T _A	0	85	°C
Storage Temperature	T _{stg}	−40	125	°C

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. 41 Series 4-14

receiver differential inputs are not equipped with ESD protection. The standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is used. The HBM ESD threshold voltages presented here were obtained using this circuit.

HBM ESD Threshold Voltage	
Device	Rating
41 Series Receiver Inputs and Outputs	>1000 V

Electrical Characteristics

Table 4-10. 41MF2 Power Supply Current Characteristics
 $T_A = 0\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current: 41MF2:					
All Outputs Disabled	I_{CC}	—	35	50	mA
All Outputs Enabled	I_{CC}	—	30	45	mA

Table 4-11. 41MF2 Voltage and Current Characteristics
 $T_A = 0\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages, $V_{CC} = 4.5\text{ V}$:					
Low, $I_{OL} = 8.0\text{ mA}$	V_{OL}	—	—	0.5	V
High, $I_{OH} = -400\text{ }\mu\text{A}$	V_{OH}	2.5	—	—	V
Enable Input Voltages:					
Low, $V_{CC} = 5.5\text{ V}$	V_{IL}^*	—	—	0.8	V
High, $V_{CC} = 4.5\text{ V}$	V_{IH}^*	2.0	—	—	V
Minimum Input Differential Voltage, $V_{IH} - V_{IL}$: [†] $-0.40\text{ V} < V_{IH} < 7.2\text{ V}$, $-0.80\text{ V} < V_{IL} < 6.8\text{ V}$	V_{TH}^*	—	0.1	0.20	V
Input Offset Voltage	V_{OFF}	—	0.15	—	V
Output Currents, $V_{CC} = 5.5\text{ V}$:					
Off-state (high Z), $V_O = 0.4\text{ V}$	I_{OZL}	—	—	-20	μA
Off-state (high Z), $V_O = 2.4\text{ V}$	I_{OZH}	—	—	20	μA
Short Circuit	I_{OS}^{\ddagger}	-25.0	—	-100	mA
Enable Input Currents, $V_{CC} = 5.5\text{ V}$					
Low, $V_{IN} = -1.2\text{ V}$	I_{iL}	—	—	-400	μA
High, $V_{IN} = 2.7\text{ V}$	I_{iH}	—	—	20	μA
Reverse, $V_{IN} = 5.5\text{ V}$	I_{iH}	—	—	100	μA
Differential Input Currents					
Low, $V_{IN} = -1.2\text{ V}$	I_{iL}	—	—	-1.0	mA
High, $V_{IN} = 7.2\text{ V}$	I_{iH}	—	—	1.0	mA

* The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment

† Outputs of unused receivers assume a logic 1 level when the inputs are left open

‡ Test must be performed one lead at a time to prevent damage to the device

Timing Characteristics

Table 4-12. 41MF2 Timing Characteristics (See Figures 6-3 and 6-4.)

Output propagation delay test circuit is connected to output (see Figure 6-8).

T_A = 25 °C, V_{CC} = 5 V.

Symbol	Parameter	Typ	Max	Unit
t _{PLH} t _{PHL}	Propagation Delay: Input to Output High Input to Output Low	3.0 3.0	5.0 5.0	ns ns
t _{PHZ} t _{PLZ}	Disable Time, C _L = 5 pF: High to High Impedance Low to High Impedance	8 8	12 12	ns ns
t _{PZH} t _{PZL}	Enable Time, C _L = 5 pF: High Impedance to High High Impedance to Low	8 8	12 12	ns ns
t _{LH}	Rise Time (20%—80%)	—	3.0	ns
t _{HL}	Fall Time (80%—20%)	—	3.0	ns