GENERAL INSTRUMENT	RO9128B/CS/C/DS/D FlexSelect™

131,072 BIT STATIC READ ONLY MEMORY

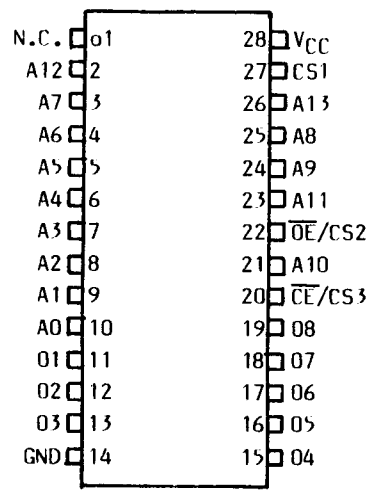
FEATURES

- 16,384 x 8 organization
- Single +5V ±10% volt supply
- 450ns max access time: RO9128B
- 350ns max access time: RO9128CS
- 300ns max access time: RO9128C
- 250ns max access time: RO9128DS
- 200ns max access time: RO9128D
- Totally static operation
- Three state outputs
- All TTL compatible inputs/outputs
- 28 pin JEDEC approved pinout
- Programmable "FlexSelect"™ chip enable/disable/power down capabilities controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs
- ESD Protection: Inputs are designed to meet 2.3KV per test method 3015.1, MIL-STD883B

PIN CONFIGURATION

28 LEAD DUAL-IN-LINE

Top View



DESCRIPTION

The General Instrument RO9128 is a 131,072 Bit Static Read Only Memory organized as 16,384 eight-bit words and is ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RO9128 provides the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation.

The RO9128 offers a programmable "Flexselect"™ chip enable/disable/power down feature controlled by the chip enable ($\overline{CE}$), output enable ($\overline{OE}$) and chip select (CS) inputs. These inputs can be programmed to implement various logic functions which provides the designer with a flexible and easy means of "chip selecting" and/or "powering down" the device. The chip select options are as shown on the following pages.

34 Res Only
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I) *Standard Chip Select requirements - Non-Power Down

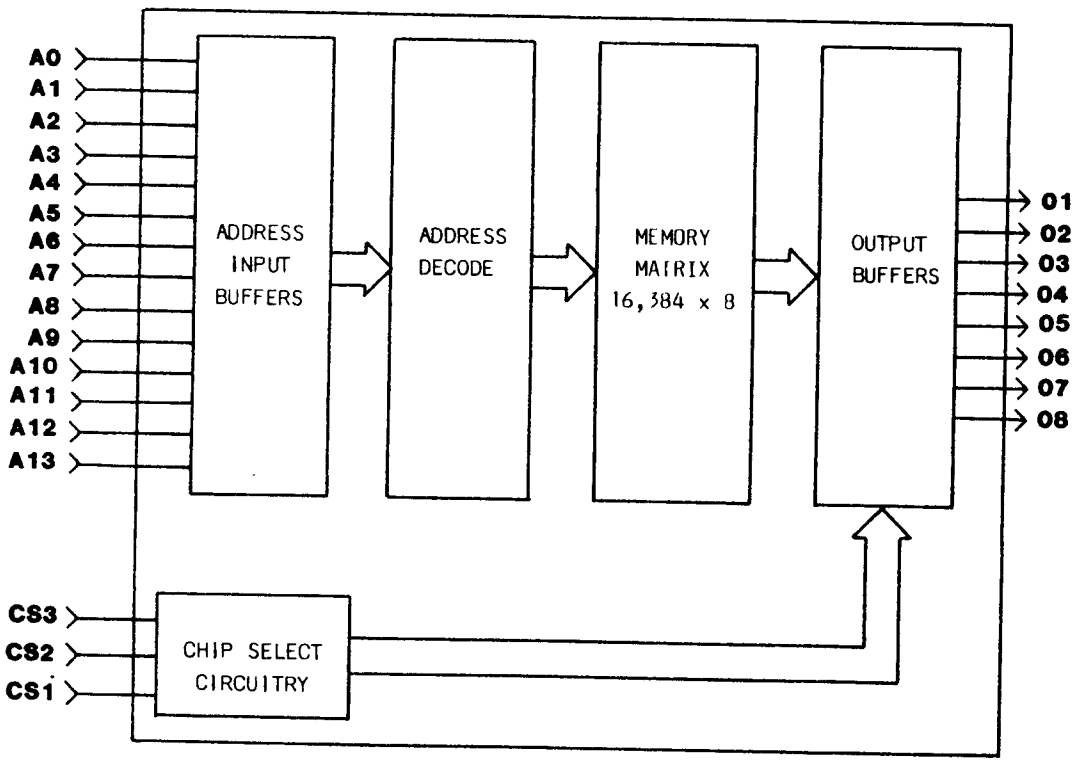
CS1 = 0,1 or don't care (Pin 27)
CS2 = 0,1 or don't care (Pin 22)
CS3 = 0,1 or don't care (Pin 20)

Logic Function $^{1}(CS1)\cdot{}^{1}(CS2)\cdot{}^{1}(CS3)$ = Chip Selected

^{1} Programmed in active state
"." = Logical "AND"

*Not available on "D" speed devices

BLOCK DIAGRAM



Chip selects (CS1, CS2, CS3) are programmable active low, active high or don't care.

II) Standard Chip Select requirements - Power Down

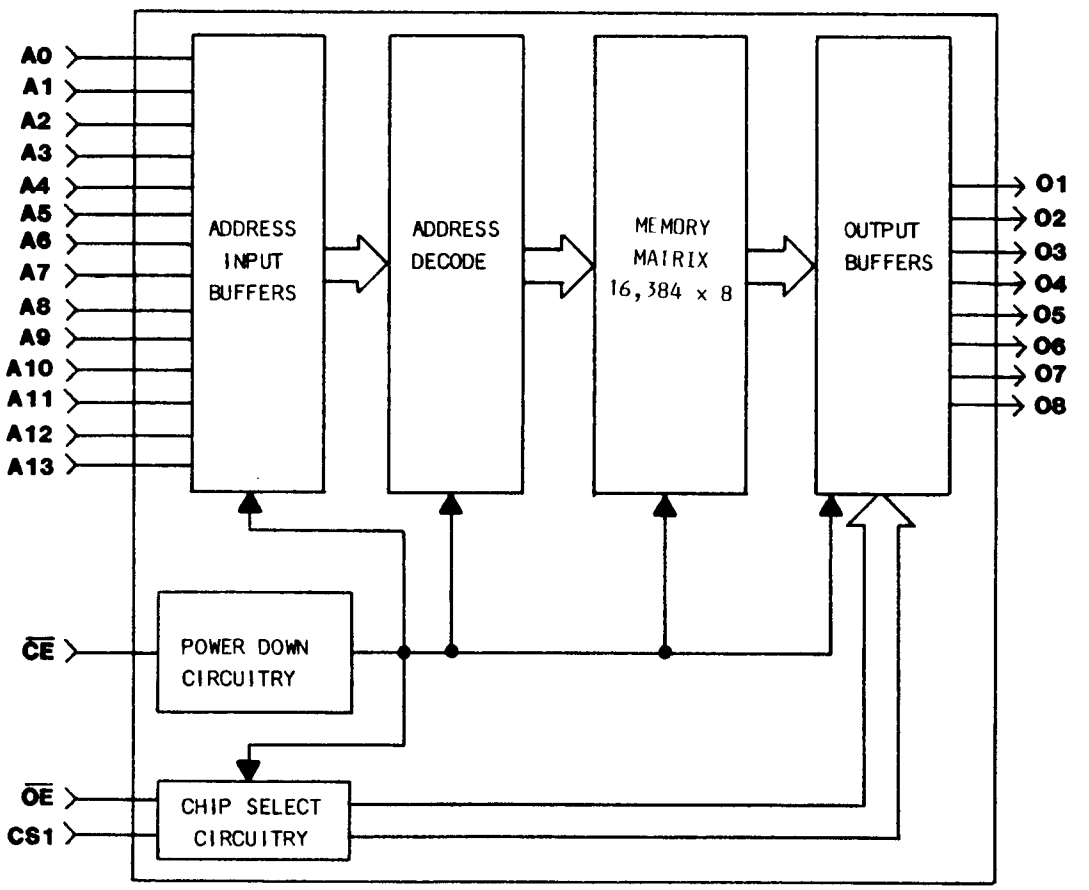
CS1 = 0,1 or don't care (Pin 27)

$\overline{OE}$ (Pin 22) When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power
$\overline{CE}$ (Pin 20) standby mode as long as $\overline{CE}$ remains high. $\overline{OE}$ and CS functions eliminate bus contention in multiple memory device systems.

Logic Function: $^{1}(CS1)\cdot(\overline{CE})\cdot(\overline{OE})$ = Chip Selected

^{1}Programmed in active state
"." = LOGICAL "AND"

BLOCK DIAGRAM



Chip select (CS1) is programmable active low, active high, or don't care.

III) **"ORED" chip select requirement (chip selects at pins 20 (CE) and 22 (OE) function as a logical "OR").

* This is ideally suited for applications that have limited chip select decoding capabilities.

CS1 = 0,1 or don't care (Pin 27)

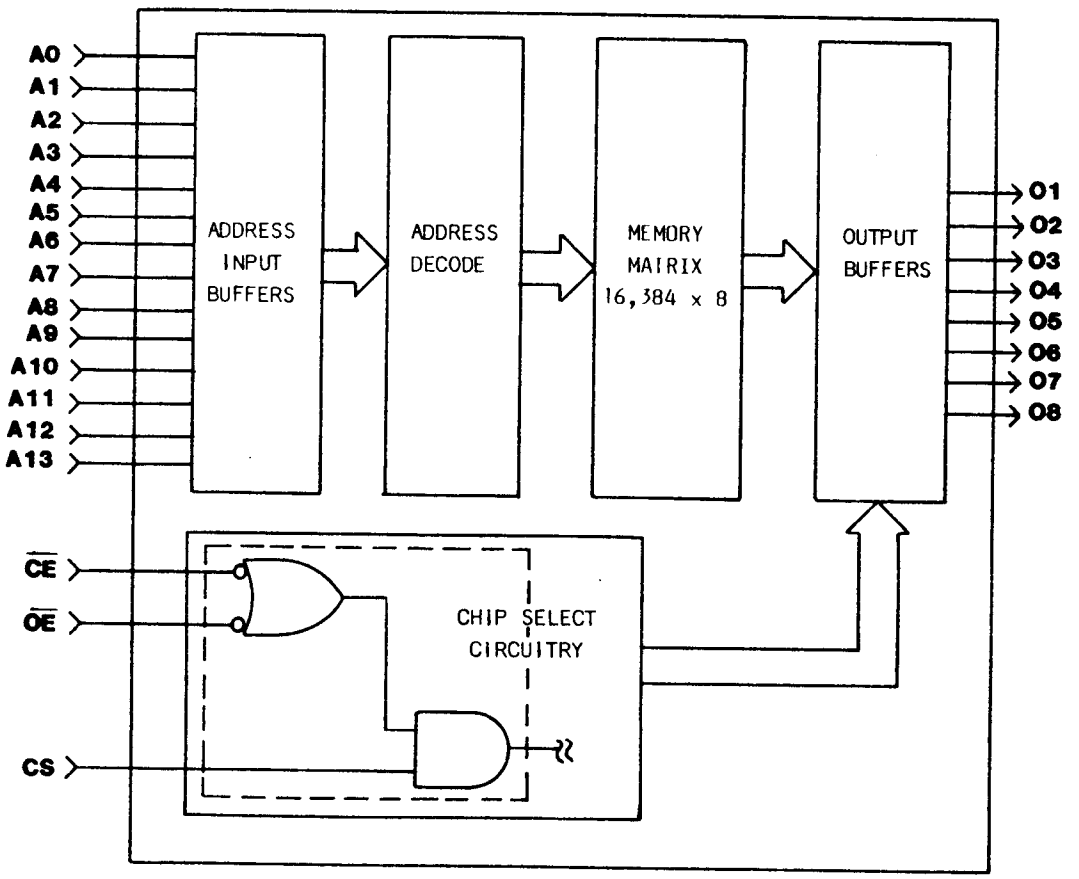
Logic Function: [1](CS).(CE + OE) = Chip Selected

[1]Programmed in active state

"." = LOGICAL "AND"
"+" = LOGICAL "OR"

**Not available on "D" speed devices

BLOCK DIAGRAM



Chip Select (CS1) is programmable active low, active high, or don't care.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND)..... -0.5V to +7.0V

Storage Temperature..... -65°C to + 150°C

Standard Conditions (unless otherwise noted):

V_{CC} = 5V ±10%

Operating Temperature T_A = 0°C to + 70°C

Output Loading: Two TTL Loads, C_L TOTAL = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied -- operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, CE/CS3, OE/CS2, CS1 Inputs						
Logic "1"	V_{IH}	2.0	-	V_{CC}	V	
Logic "0"	V_{IL}	0	-	0.8	V	
Leakage	I_{LI}	-10	-	+10	µA	V_{IN}=0.4V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	-	V_{CC}	V	I_{OH}=-200µA
Logic "0"	V_{OL}	-	-	0.4	V	I_{OL}=3.2mA
Leakage	I_{LO}	-10	-	+10	µA	V_{OUT}=0.4V to V_{CC}
Power Supply Current						
I_{CC} (Active)	-	-	-	100	mA	Note 1
I_{CC} (Standby)	-	-	-	15	mA	Note 2,6
I_{CC} (Standby)	-	-	-	50	mA	Note 7

AC CHARACTERISTICS

		R09128B		R09128CS		R09128C		R09128DS		R09128D			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	-	450	-	350	-	300	-	250	-	200	ns	
Address Hold After Address Change	t_{OH}	10	-	10	-	5	-	5	-	5	-	ns	Note 3
Chip Enable Time	t_{ACE}	-	450	-	350	-	300	-	250	-	200	ns	
Chip Select, Output Enable Access Time	t_{ACS}	-	150	-	125	-	100	-	85	-	70	ns	Note 4
Output Disable Time	t_{OFF}	-	150	-	125	-	100	-	85	-	70	ns	
Output Low Z Delay	t_{LZ}	10	-	10	-	5	-	5	-	5	70	ns	Note 3
Output High Z Delay	t_{HZ}	-	150	-	125	-	100	-	85	-	70		
Capacitance***													
Input Capacitance	C_I	-	7	-	7	-	7	-	7	-	7	pf	F=1MHz, T_A=+25°C
Output Capacitance	C_O	-	10	-	10	-	10	-	10	-	10	pf	F=1MHz, T_A=+25°C

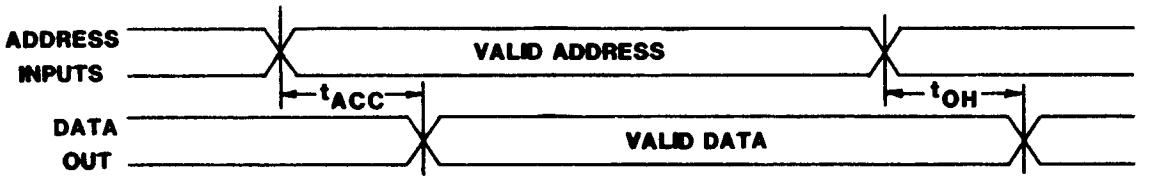
***Capacitance is periodically sampled and is not 100% tested.

NOTES:

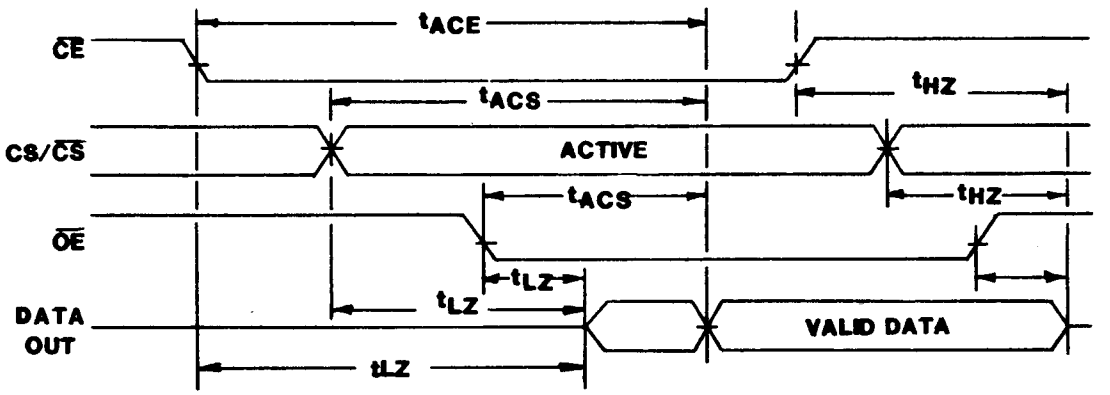
1. Measured with device selected and outputs unloaded.
2. Device disabled with $\overline{CE} \geq 2.0V$ ("Power Down" programmed parts only).
3. These parameters are periodically sampled and are not 100% tested.
4. Access time to valid data measured from CS1 going active and/or $\overline{OE}$ going low which ever occurs last/first.
5. Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ and/or $\overline{OE}$ going high or CS1 going active, which ever occurs last/first.
6. Applies to B, CS, and C speeds only.
7. Applies to DS, D speeds only.

TIMING DIAGRAMS

Propagation Delay from Address $\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5/10ns
Timing Measurement Levels: Input/Output	0.8V AND 2.0V
Output Load	See Figure 1

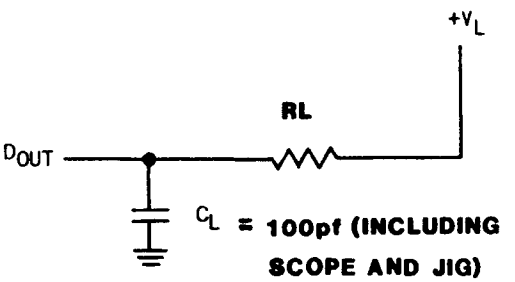


Fig. 1