

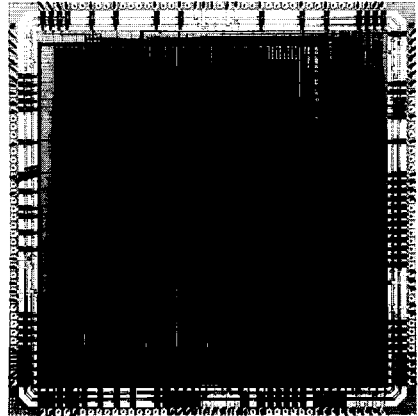
L64210/L64211 Variable-Length Video Shift Registers

Description

The L64210 and L64211 are two high-speed Variable-Length Video Shift Registers. These devices can be used individually or as video line delays for the L64200 series filter processors.

The L64210 provides four individual 8-bit shift registers, each with a length of up to 1032, and is packaged in a 68-pin Plastic Leaded Chip Carrier or Ceramic Pin Grid Array.

The L64211 provides eight individual 8-bit shift registers, each with a length adjustable to 516 and is packaged in a 120-pin Ceramic Pin Grid Array.



L64210 Chip

Features

- Variable-length video shift register
- Acts as a variable-length line delay, reformatting serial (raster-scanned video) data into a 2-D video signal for image processing
- Can work individually or with any of the LSI Logic L64200 series filter processors
- L64210 contains four separate 8-bit shift registers whose length can be varied from 24 to 1032
- L64211 contains eight separate 8-bit shift registers whose length can be varied from 12 to 516
- High data rates
- Control available to blank (force to zero) data outputs during horizontal video blanking intervals
- Control available to blank (force to zero) data inputs, which could be used to ignore invalid data during vertical video blanking intervals
- Input data can be sent to all eight internal shift registers simultaneously
- L64210 is available in a 68-pin PLDCC (Plastic Leaded Chip Carrier) or CPGA (Ceramic Pin Grid Array) package
- L64211 is available in a 120-pin CPGA (Ceramic Pin Grid Array) package

Commercial
20 MHz
15 MHz

Military
16 MHz
12 MHz

Architecture

The L64211 contains eight individual 8-bit variable-length shift registers which can be used as video line delays. The L64210 has every other shift register output connected to external package pins and effectively has four individual 8-bit shift registers. The length of the shift registers is controlled by the value residing in the level-triggered LENGTH latch register controlled by an active LOW \overline{WE} input. The length of each of the eight shift registers of the L64211 can be varied from 12 to 516 bits by loading the LENGTH register according to:

$$\text{Number of Shifts} = (4 \cdot \text{LENGTH}) + 8.$$

where 0 is an illegal input. Since the L64210 internally cascades two shift registers together, each of the resulting four registers can be varied from 24 to 1032 bits long, and its length is determined by the equation:

$$\text{Number of Shifts} = (8 \cdot \text{LENGTH}) + 16.$$

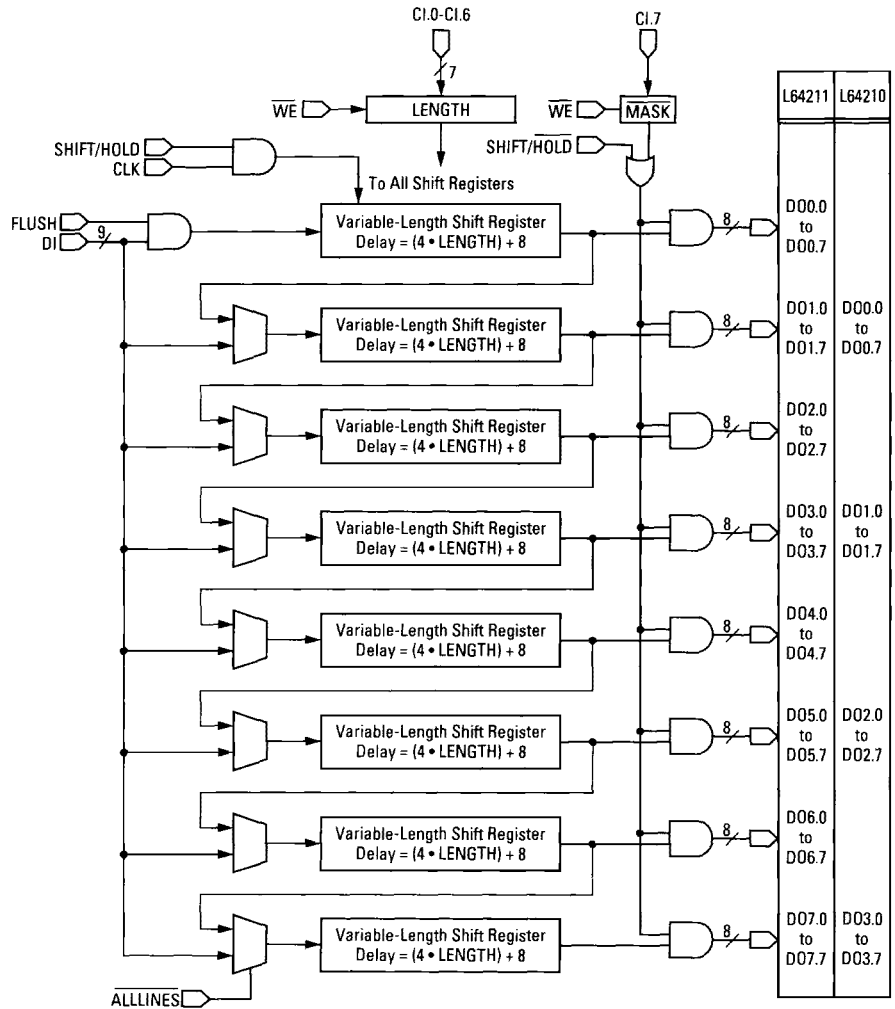
L64210/L64211 Variable-Length Video Shift Registers

Architecture (Continued)

In a video or image-processing system, the length of each shift register is normally set to the number of pixels per video line. When used in this fashion (as a video line delay or as a front end to any of the LSI Logic real-time image-processing chips), the line delay outputs the pixels vertically adjacent to (in the same column as) the input pixel. In the case of the L64211, the outputs of the eight line delays will

be eight pixels in a vertical line. To accommodate the horizontal and vertical blanking periods of a video signal, provision is made to disable the shift register. The **SHIFT/HOLD** input causes the system clock to be disabled - ie data is not shifted. The **MASK** and **FLUSH** controls allow the outputs and inputs respectively of the device to be forced to zero.

Block Diagram



L64210/L64211 Variable-Length Video Shift Registers

Pin Listing and Description

DI
Eight-bit input data bus. Data inputs are loaded into the first stage of the shift register at the rising edge of CLK while SHIFT/HOLD is HIGH.

CLK
System clock. Active at the rising edge.

FLUSH
When FLUSH is LOW, zeros are forced into the shift register. This action overrides the data on DI bus. If FLUSH is connected to the vertical blanking signal in a video system, the input will be blank during the blanking period.

CI.0 to CI.7
Control input bus. This bus is common to all L64200 series devices. On the L64210/11, the bus feeds into two control registers, LENGTH and MASK.

WE
Active-LOW Write Enable for the CI (LENGTH and MASK control) inputs. When WE is LOW, new data is written into the LENGTH and MASK registers. LENGTH becomes active at the next rising edge of CLK.

SHIFT/HOLD

Disables the action of the CLK input and forces the shift register outputs LOW when MASK is LOW. When SHIFT/HOLD is connected to the horizontal blanking signal in a video system, data will not be loaded during the horizontal blanking period.

DOX.Y

Data output buses where X and Y represent the output bus number and bit numbers, respectively. The L64210 has 4 8-bit output buses, while the L64211 has 8 8-bit output buses.

ALLINES

When ALLINES is LOW, data from DI bus (overridden by FLUSH) is fed into all eight shift registers simultaneously. ALLINES is intended as a test function; in normal operation it should be held HIGH.

TEST

Internal LSI Logic test input. Should be held HIGH or left unconnected by user.

Loading of Control Words

The L64210 and L64211 are configured by writing an 8-bit control word to the LENGTH and MASK registers. The LENGTH register, accessed through CI.0 - CI.6 is a number between 0 and 127 which controls the length of the individual shift registers.

For the L64210 each of the four shift registers will be of length $(8 \cdot \text{LENGTH}) + 16$. For the L64211 the length of each of the eight shift registers will be $(4 \cdot \text{LENGTH}) + 8$.

The value written into LENGTH becomes active on the next rising edge of the clock after it has

been written. The value in this register must be greater than zero for correct operation.

The MASK register, which is accessed through CI.7, controls the masking of the outputs. If a zero is written into MASK then the effect of the SHIFT/HOLD input will be to force all data outputs to zero. If a one is written into MASK then the effect of the SHIFT/HOLD input will be to freeze the current value on the outputs.

Both the MASK and LENGTH registers are loaded when WE is LOW.

Blanking Periods

Typically the horizontal blanking signal of a video system will be tied to the SHIFT/HOLD input. This disables the clock and hence disables data input to the device, during the blanking period. If MASK has been set LOW then this will also have the effect of setting to zero – ie blanking – the data outputs.

If MASK is LOW and SHIFT/HOLD is taken LOW then the delay from SHIFT/HOLD going LOW to the data outputs being valid (ie zero) is 20 ns.

When SHIFT/HOLD is taken HIGH again, the delay to data outputs being valid is 15 ns. The vertical blanking signal might be connected to the FLUSH input, causing zeros to be input into the device during this period. This means that any spurious data during vertical blanking will be ignored, leaving only zero data values between frames.

For operation as a standard shift register, both FLUSH and MASK should be held high.

L64210/L64211 Variable-Length Video Registers

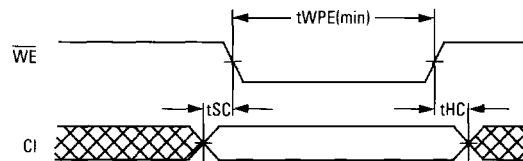
Data Retention

The shift registers in the L64210 and L64211 are constructed from DRAM cells. These DRAM cells are refreshed only when a new data value is written into that location. In the worst case, ie with the shift registers set to their maximum length, there will be 512 cycles, plus any time when SHIFT/HOLD is held LOW, between successive writes to a location. The DRAM used will retain data for 200 usecs. Care must be taken to ensure that the cumulative

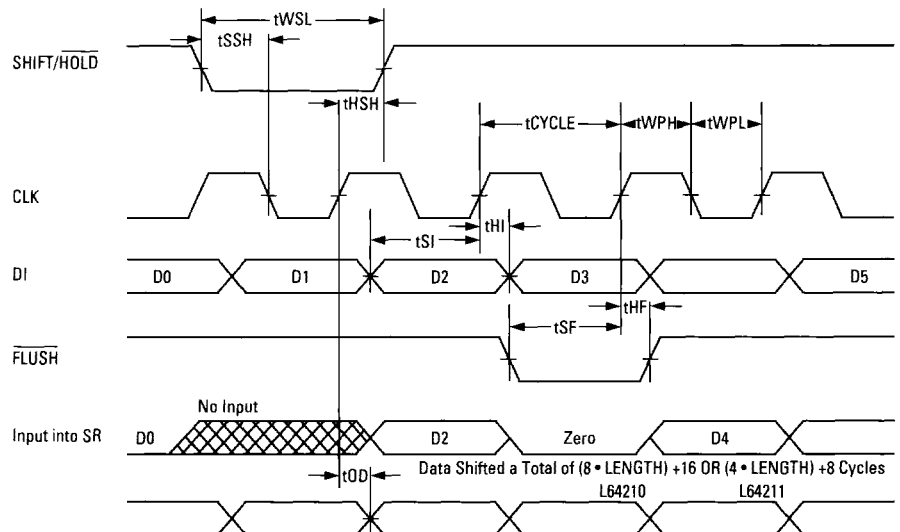
time between accesses does not exceed this limit. The maximum values given in the AC Switching Characteristics for tCYCLE and tWSL are an example of meeting this requirement: the total time elapsed between successive writes to the same memory location is given by $(512 \cdot 200) + 100,000 = 200,400$ ns. In practice, the designer may trade off the parameters of LENGTH, tCYCLE and tWSL as long as this 200 usec limit is observed.

AC Timing

Coefficient/Control Section



Input Timing



L64210/L64211
Variable-Length
Video Shift Registers



AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64210-20 L64211-20		L64210-15 L64211-15	
tCYCLE	Clock cycle time	50	400*	65	400*
tPWH(min)	Min clock pulse width HIGH	10		15	
tPWL(min)	Min clock pulse width LOW	10		15	
tSI	Input data set-up time	10		15	
tHI	Input data hold time	5		6	
tWPE	WE pulse width	20		30	
tSC	CI input set-up time	7		8	
tHC	CI input hold time	5		6	
tSF	FLUSH input set-up time	7		8	
tHF	FLUSH input hold time	5		6	
tOD	Output delay time		33		40
tSSH	SHIFT/HOLD set-up time	2		3	
tHSH	SHIFT/HOLD hold time	0		0	
tWSL	SHIFT/HOLD width LOW		200,000*		200,000

AC Switching Characteristics: Military (TA = 55°C to 125°C, VDD = 4.5 V to 5.5 V)

Symbol	Parameter	L64210-16 L64211-16		L64210-12 L64211-12	
tCYCLE	Clock cycle time	60	400*	75	400*
tPWH(min)	Min clock pulse width HIGH	25		35	
tPWL(min)	Min clock pulse width LOW	25		35	
tSI	Input data set-up time	20		25	
tHI	Input data hold time	10		15	
tWPE	WE pulse width	30		35	
tSC	CI input set-up time	15		20	
tHC	CI input hold time	15		20	
tSF	FLUSH input set-up time	20		25	
tHF	FLUSH input hold time	10		15	
tOD	Output delay time		35		55
tSSH	SHIFT/HOLD set-up time	3		4	
tHSH	SHIFT/HOLD hold time	0		0	
tWSL	SHIFT/HOLD width LOW		200,000*		200,000

All units are in ns, output loading = 50 pF.

* Assuming SHIFT/HOLD always HIGH, LENGTH = 127.

** Assuming LENGTH = 1 (see text for further information).

L64210/L64211

Variable-Length Video Shift Registers

Ordering Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	± 10	mA
Storage temperature range	TSTG	-65 to + 150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range	TA	- 55 to + 125	°C
Military			
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges¹

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIL	Low level input voltage				0.8	V
VIH ²	High level input voltage		2.0			V
	Commercial temperature range		2.25			V
	Military temperature range					V
IIN	Input current	VIN = VDD	-150		200	µA
VOH	High level output voltage	Comm Mil				
		IOH = -4 mA -3.2 mA	2.4	4.5		V
VOL	Low level output voltage	Comm Mil				
		IOL = 4 mA 3.2 mA		0.2	0.4	V
IOS	Output short circuit current ³	VDD = Max, VO = VDD	15		130	mA
		VDD = Max, VO = 0V	-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS			10	mA
IDD	Operating supply current	tCYCLE = 50 ns		100		mA
CIN	Input capacitance	Any Input		5		pF
COUT	Output capacitance	Any Output		10		pF

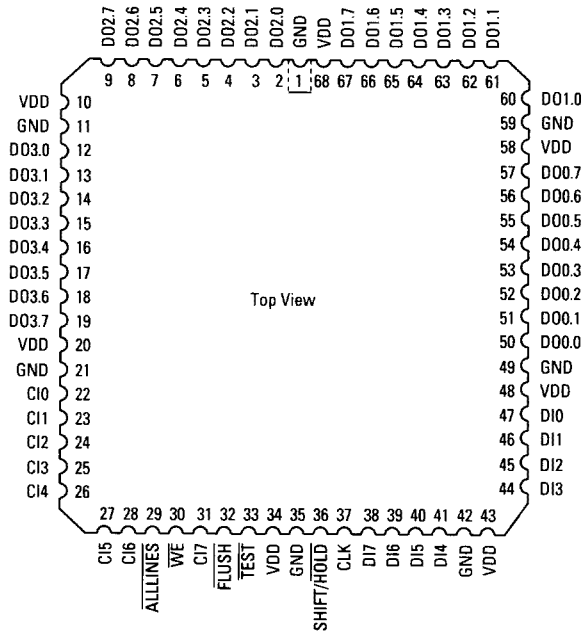
Notes:

1. Military temperature range is -55°C to + 125°C, ± 10% power supply; commercial temperature range is 0°C to 70°C, ± 5% power supply.
2. L64211, VIH for CLK, WE, and TEST = 2.6 V commercial, 3.0 V military.
3. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

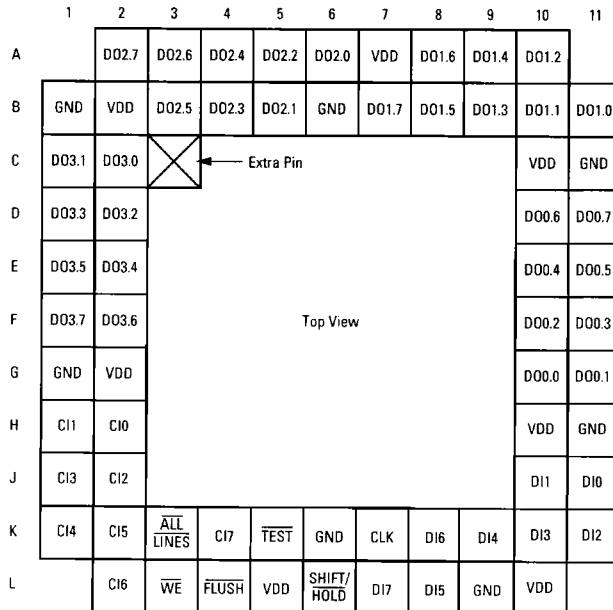
L64210/L64211 Variable-Length Video Shift Registers

L64210 Pinout Diagram

68-Pin Plastic Leaded Chip Carrier (PLCC)



68-Pin Grid Array (PGA)





L64210/L64211
Variable-Length
Video Shift Registers

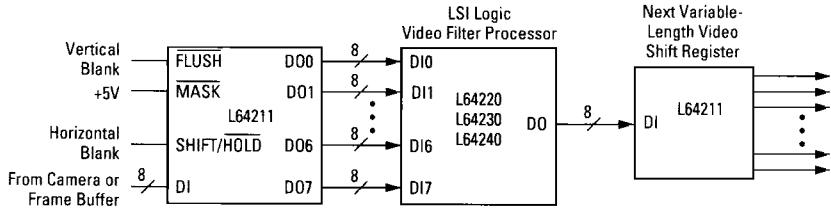
L64211 Pinout Diagram 120-Pin Ceramic Pin Grid Array (CPGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	D05.6	D05.5	D05.3	NC	D05.0	NC	VDD	NC	D03.6	D03.4	D03.1	D03.0
B	VDD	NC	D05.7	D05.4	D05.2	NC	NC	NC	NC	D03.5	D03.3	NC	VDD
C	D07.1	D07.0	NC	NC	NC	D05.1	GND	D03.7	NC	D03.2	NC	NC	D01.7
D	D07.4	D07.2	GND	X	Extra Pin						GND	D01.6	D01.4
E	D07.6	D07.5	D07.3	Top View						D01.5	D01.3	D01.2	
F	NC	NC	D07.7							D01.1	D01.0	D00.0	
G	D06.6	NC	D06.7							D00.2	D00.3	D00.1	
H	D06.5	D06.4	VDD							D00.6	D00.5	D00.4	
J	GND	D06.3	D06.1							D02.0	GND	D00.7	
K	D06.2	D06.0	C12							D10	D02.1	VDD	
L	C10	C13	C15							D04.6	D04.3	\overline{WE}	VDD
M	C11	C16	\overline{ALL} LINES	D04.4	D04.1	C17	\overline{TEST}	CLK	D02.5	D17	GND	D12	D11
N	C14	D04.7	D04.5	D04.2	D04.0	\overline{FLUSH}	GND	$\overline{SHIFT/HOLD}$	D02.6	D02.4	D16	D15	VDD

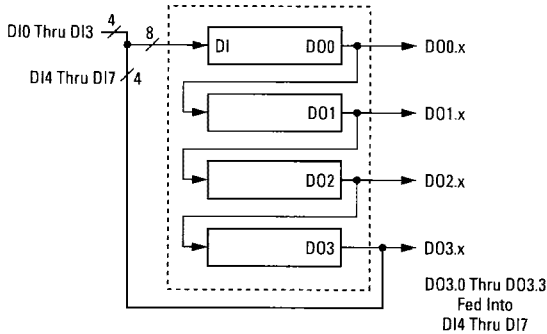
**L64210/L64211
Variable-Length
Video Shift Registers**

Application Examples

Recommended Application in a Video System



**Example No. 1: L64210 Configured for 4-Bit Operation
Eight Individual 1 K x 4 Shift Registers**

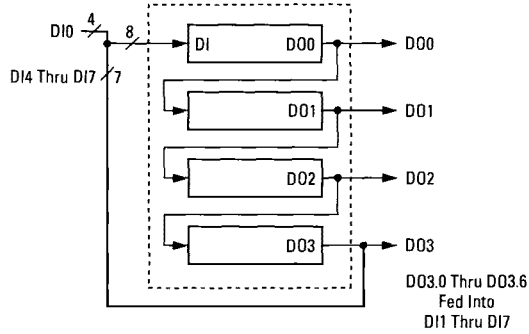


Output of Shift Register	Data Output Pins
0	D00.0...D00.3
1	D01.0...D01.3
2	D02.0...D02.3
3	D03.0...D03.3
4	D00.4...D00.7
5	D01.4...D01.7
6	D02.4...D02.7
7	D03.4...D03.7

**L64210/L64211
Variable-Length
Video Shift Registers**

**Application Examples
(Continued)**

**Example No. 2: L64210 Set-Up for Binary Operation
32 Individual 1 K x 1 Shift Registers**

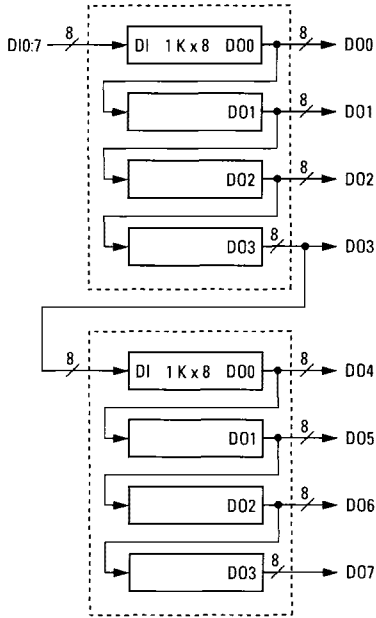


Output of Shift Register	Data Output Pins
0	D00.0
1	D01.0
2	D02.0
3	D03.0
4	D00.1
*	*
*	*
*	*
29	D01.7
30	D02.7
31	D03.7

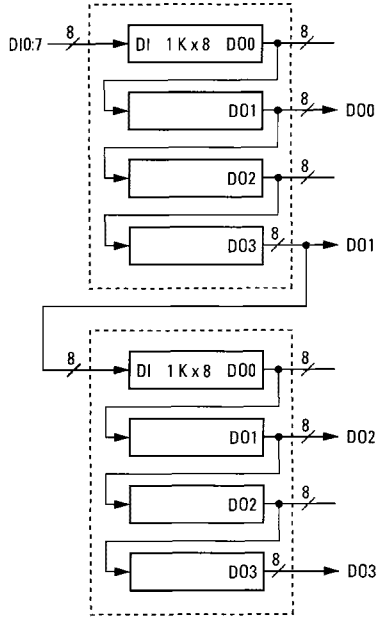
**L64210/L64211
Variable-Length
Video Shift Registers**

**Application Examples
(Continued)**

Example No. 3: Expansion to Larger Shift Registers. Eight 1 K x 8 Shift Registers Using Two L64210s



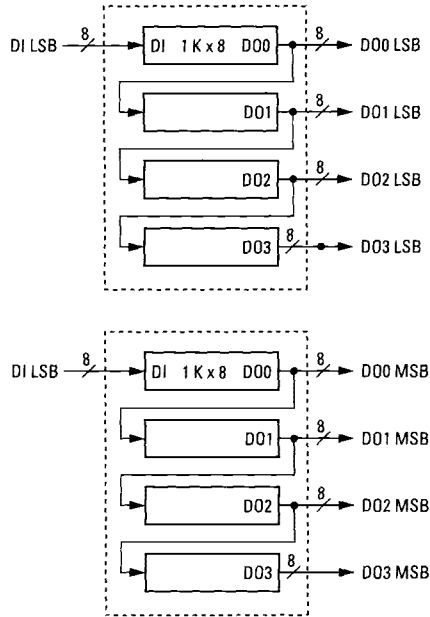
Example No. 4: Expansion to Larger Shift Registers. Four 2 K x 8 Shift Registers Using Two L64210s



**L64210/L64211
Variable-Length
Video Shift Registers**

**Application Examples
(Continued)**

**Example No. 5: Expansion to Larger Shift Registers.
Four 1 K x 16 Shift Registers Using Two L64210s**





**L64210/L64211
Variable-Length
Video Shift Registers**

Packaging

68-pin Plastic Leaded Chip Carrier: See MC Package in Package Selector Guide
68-pin Ceramic Pin Grid Array: See FB Package in Package Selector Guide
120-pin Ceramic Pin Grid Array: See FD Package in Package Selector Guide

Ordering Information

