

# SN54LS348, SN74LS348 (TIM9908) 8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

SDLS161 - OCTOBER 1976 - REVISED MARCH 1988

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:  
N-Bit Encoding  
Code Converters and Generators
- Typical Data Delay . . . 15 ns
- Typical Power Dissipation . . . 60 mW

## description

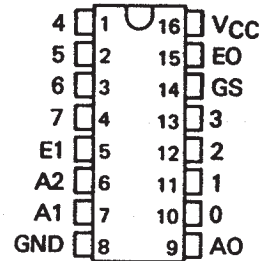
These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'LS348 circuits encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output EO) has been provided to allow octal expansion. Outputs A0, A1, and A2 are implemented in three-state logic for easy expansion up to 64 lines without the need for external circuitry. See Typical Application Data.

FUNCTION TABLE

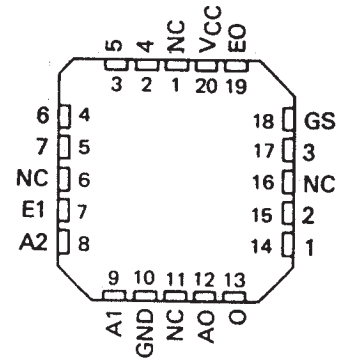
E1	INPUTS								OUTPUTS				
	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	L	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	L	L	H
L	L	H	H	H	H	H	H	H	H	H	L	L	H

H = high logic level, L = low logic level, X = irrelevant  
Z = high-impedance state

SN54LS348 . . . J OR W PACKAGE  
SN74LS348 . . . D OR N PACKAGE  
(TOP VIEW)

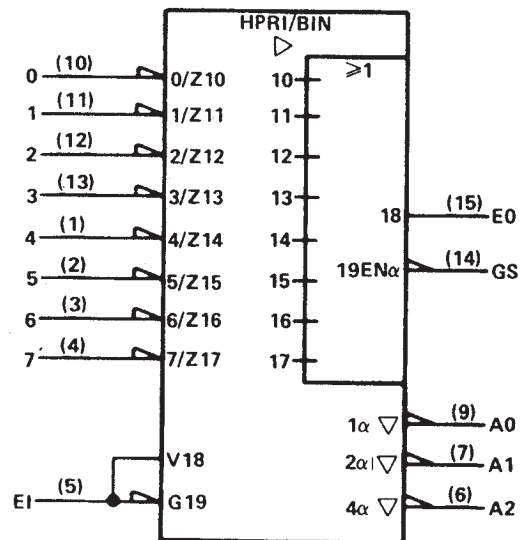


SN54LS348 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol†



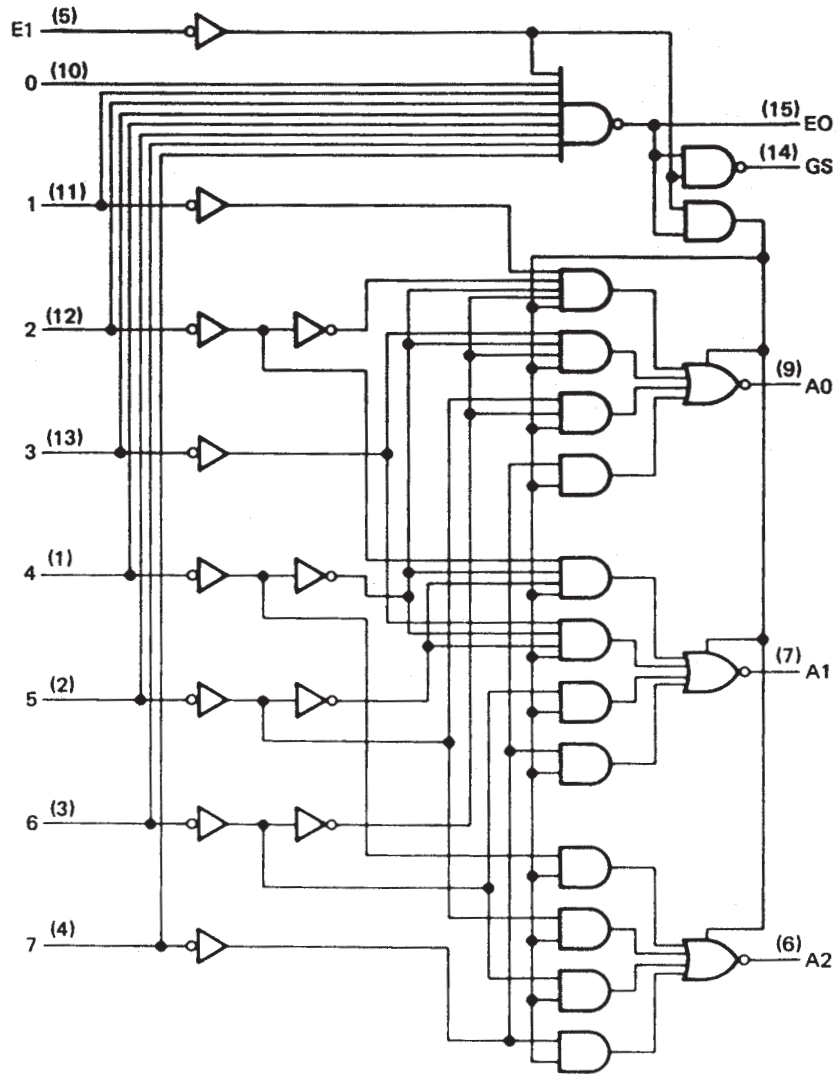
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

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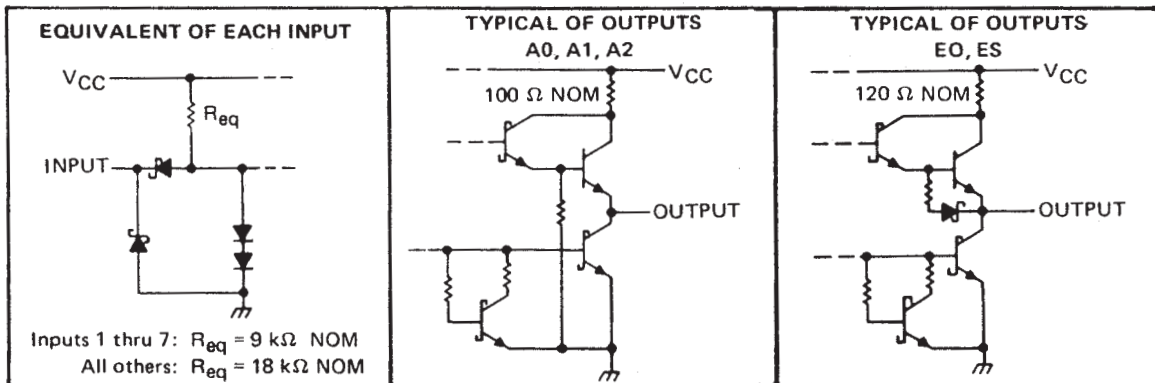
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## logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

## schematic of inputs and outputs



# SN54LS348, SN74LS348 (TIM9908)

## 8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS348	-55°C to 125°C
SN74LS348	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

	SN54LS348			SN74LS348			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	A0, A1, A2			-1			mA
	EO, GS			-400			$\mu$ A
Low-level output current, $I_{OL}$	A0, A1, A2			12			mA
	EO, GS			4			mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS348		SN74LS348		UNIT	
			MIN	TYP‡	MAX	MIN		TYP‡
$V_{IH}$	High-level input voltage		2		2		V	
$V_{IL}$	Low-level input voltage		0.7		0.8		V	
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5		-1.5		V	
$V_{OH}$	High-level output voltage	A0, A1, A2	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$		2.4 3.1		V	
		EO, GS	$V_{IL} = V_{IL\text{max}}, I_{OH} = -2.6 \text{ mA}$		2.4 3.1			
$V_{OL}$	Low-level output voltage	A0, A1, A2	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}$		0.25 0.4		V	
			$I_{OL} = 24 \text{ mA}$		0.35 0.5			
		$V_{IL} = V_{IL\text{max}}, I_{OL} = 4 \text{ mA}$		0.25 0.4		0.25 0.4		
				$I_{OL} = 8 \text{ mA}$		0.35 0.5		
$I_{OZ}$	Off-State (high-impedance state) output current	A0, A1, A2	$V_{CC} = \text{MAX}, V_{OH} = 2.7 \text{ V}, V_{OL} = 0.4 \text{ V}$		20		$\mu$ A	
					-20			
$I_I$	Input current at maximum input voltage	Inputs 1 thru 7	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.2		mA	
		All other inputs			0.1			
$I_{IH}$	High-level input current	Inputs 1 thru 7	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		40		$\mu$ A	
		All other inputs			20			
$I_{IL}$	Low-level input current	Inputs 1 thru 7	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.8		mA	
		All other inputs			-0.4			
$I_{OS}$	Short-circuit output current§	Outputs A0, A1, A2	$V_{CC} = \text{MAX}$		-30 -130		mA	
		Outputs EO, GS			-20 -100			
$I_{CC}$	Supply current		$V_{CC} = \text{MAX}$	Condition 1		13 25		mA
			See Note 2			Condition 2		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  (condition 1) is measured with inputs 7 and E1 grounded, other inputs and outputs open.  $I_{CC}$  (condition 2) is measured with all inputs and outputs open.



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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	1 thru 7	A0, A1, or A2	In-phase output	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω, See Note 3		11	17	ns
t <sub>PHL</sub>						20	30	
t <sub>PLH</sub>	1 thru 7	A0, A1, or A2	Out-of-phase output			23	35	ns
t <sub>PHL</sub>						23	35	
t <sub>PZH</sub>	EI	A0, A1, or A2				25	39	ns
t <sub>PZL</sub>						24	41	
t <sub>PLH</sub>	0 thru 7	EO	Out-of-phase output	C <sub>L</sub> = 15 pF R <sub>L</sub> = 2 kΩ, See Note 3		11	18	ns
t <sub>PHL</sub>						26	40	
t <sub>PLH</sub>	0 thru 7	GS	In-phase output			38	55	ns
t <sub>PHL</sub>						9	21	
t <sub>PLH</sub>	EI	GS	In-phase output			11	17	ns
t <sub>PHL</sub>						14	36	
t <sub>PLH</sub>	EI	EO	In-phase output			17	26	ns
t <sub>PHL</sub>						25	40	
t <sub>PHZ</sub>	EI	A0, A1, or A2			C <sub>L</sub> = 5 pF R <sub>L</sub> = 667 Ω		18	27
t <sub>PLZ</sub>						23	35	

† t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

t<sub>PZH</sub> = output enable time to high level

t<sub>PZL</sub> = output enable time to low level

t<sub>PHZ</sub> = output disable time from high level

t<sub>PLZ</sub> = output disable time from low level

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## TYPICAL APPLICATION DATA

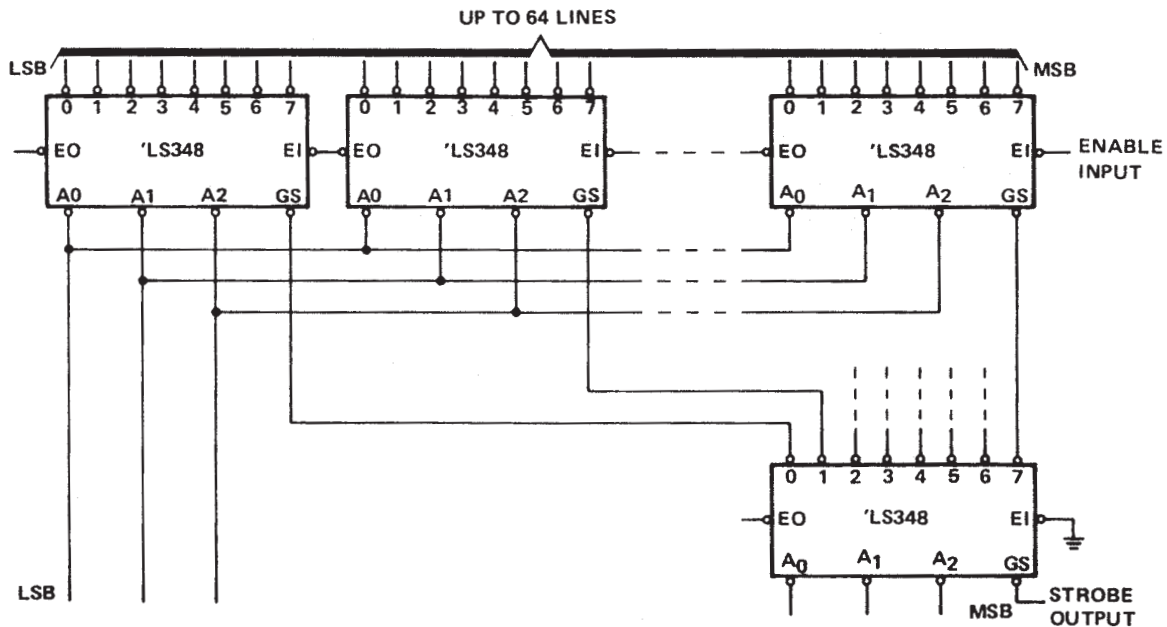


FIGURE 1—PRIORITY ENCODER WITH UP TO 64 INPUTS.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
JM38510/36002B2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
JM38510/36002BEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SN54LS348J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SN74LS348D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS348	<a href="#">Samples</a>
SN74LS348DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS348	<a href="#">Samples</a>
SN74LS348DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS348	<a href="#">Samples</a>
SN74LS348N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS348N	<a href="#">Samples</a>
SN74LS348N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS348NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS348N	<a href="#">Samples</a>
SNJ54LS348FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS348J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS348W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54LS348, SN74LS348 :**

- Catalog: [SN74LS348](#)
- Military: [SN54LS348](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

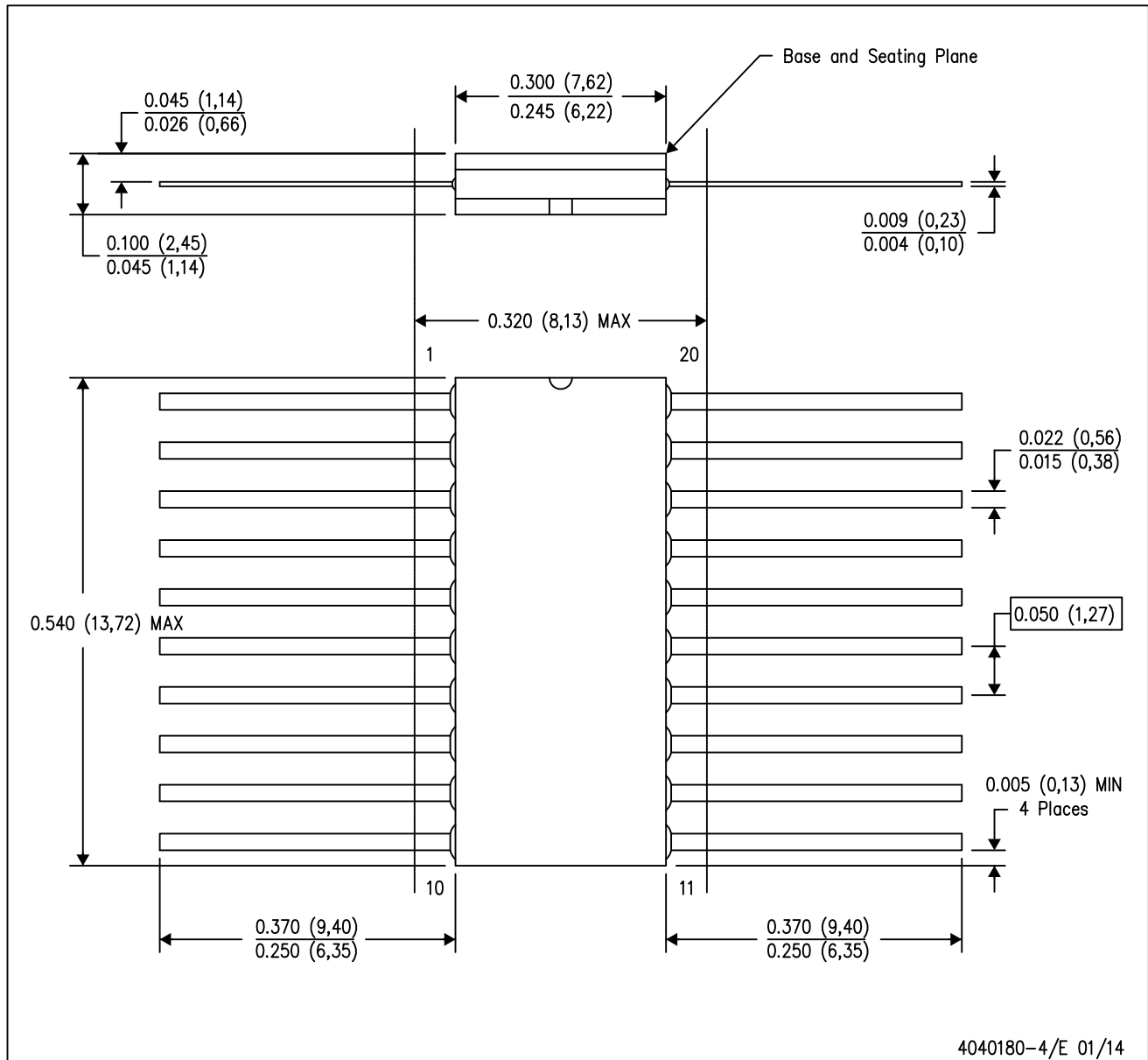


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within Mil-Std 1835 GDFP2-F20



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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