

BGS8L3UK

SiGe:C low-noise amplifier MMIC with bypass switch for LTE

Rev. 1 — 17 November 2016

Product data sheet

1. General description

The BGS8L3UK is a Low-Noise Amplifier (LNA) with bypass switch for LTE receiver applications, available in a Wafer-Level Chip-Scale Package (WLCSP). This product is only used in an overmolded module.

The BGS8L3UK delivers system-optimized gain for both primary and diversity applications where sensitivity improvement is required. The high linearity of this low noise device ensures the required receive sensitivity independent of cellular transmit power level in Frequency Division Duplex (FDD) systems. When receive signal strength is sufficient, the BGS8L3UK can be switched off to operate in bypass mode at a 1 μ A current to lower power consumption.

The BGS8L3UK is optimized for 720 MHz to 960 MHz.

2. Features and benefits

- Operating frequency from 720 MHz to 960 MHz
- Noise figure = 0.9 dB
- Gain 15 dB
- High input 1 dB compression point of -3.5 dBm
- Bypass switch insertion loss of -1.8 dB
- IP_{3i} of 0.5 dBm
- Supply voltage 1.5 V to 3.1 V
- Integrated supply decoupling capacitor
- Optimized performance at a supply current of 5.7 mA
- Bypass mode current consumption < 1 μ A
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Input and output AC coupled
- ESD protection on all pins (HBM > 2 kV)
- Integrated matching for the output
- Available in a WLCSP 0.69 mm \times 0.44 mm \times 0.29 mm: SOT1445-1
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity level 1



3. Applications

- LNA for LTE reception in smart phones
- tablet PCs
- feature phones
- RF front-end modules

4. Quick reference data

Table 1. Quick reference data

$f = 882 \text{ MHz}$; $V_{CC} = 2.8 \text{ V}$; $V_{I(CTRL)} \geq 0.8 \text{ V}$; $T_{amb} = 25^\circ\text{C}$. Input matched to 50Ω using a 8.2 nH Murata LQW15 type inductor connected in series; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
I_{CC}	supply current	in gain mode	-	5.7	-	mA
		in bypass mode; $0.1 \text{ V} \leq V_{I(CTRL)} \leq 0.3 \text{ V}$	-	-	1	μA
G_p	power gain	in gain mode [1]	-	15	-	dB
		in bypass mode [1]	-	-1.8	-	dB
NF	noise figure	[1][2]	-	0.9	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	[1]	-	-3.5	-	dBm
$IP3_i$	input third-order intercept point	[1]	-	0.5	-	dBm

[1] E-UTRA operating band 5 (869 MHz to 894 MHz).

[2] PCB losses are subtracted.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BGS8L3UK	WLCSP6	wafer level chip-scale package; 6 bumps; $0.69 \times 0.44 \times 0.29 \text{ mm}$	SOT1445-1

6. Marking

Table 3. Marking codes

Type number	Marking code
BGS8L3UK	single character, indicating assembly month [1]

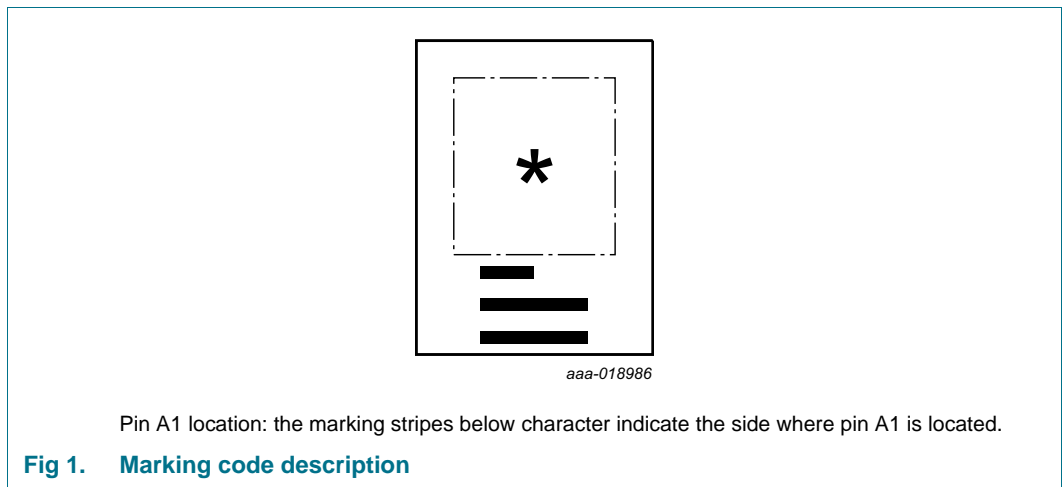
[1] Month codes see [Table 4](#).

Table 4. Calendar marking month code

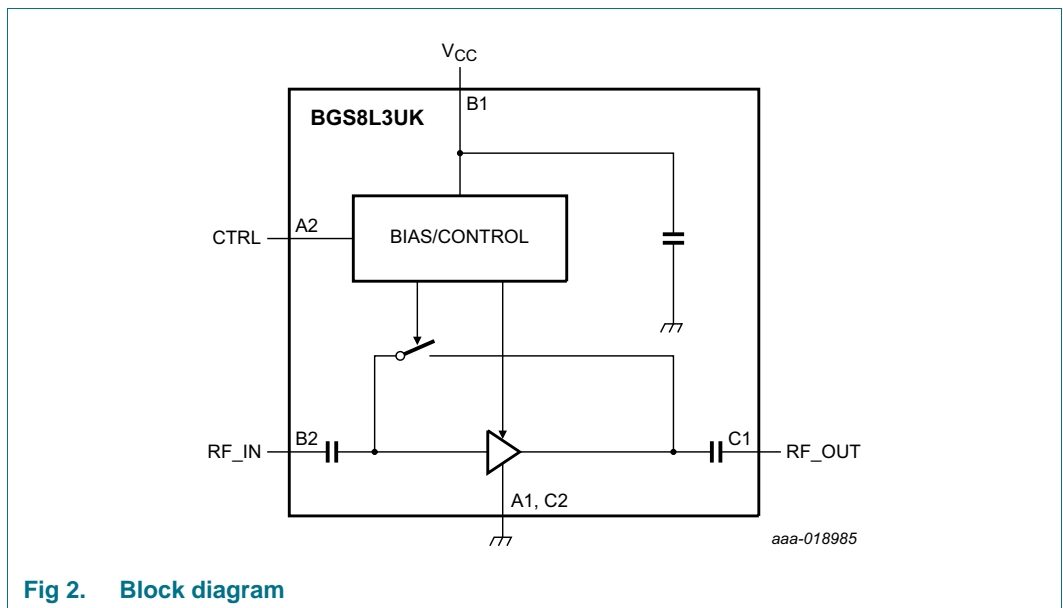
The character from the table replaces the asterisk (*), see [Figure 1](#).

Year ^[1]	Month											
	J	F	M	A	M	J	J	A	S	O	N	D
2015	A	B	C	D	E	F	G	H	I	J	K	L
2016	M	N	O	P	Q	R	S	T	U	V	W	X
2017	Y	Z	b	d	f	h	3	4	5	6	7	8

[1] Rotates every 3 years.

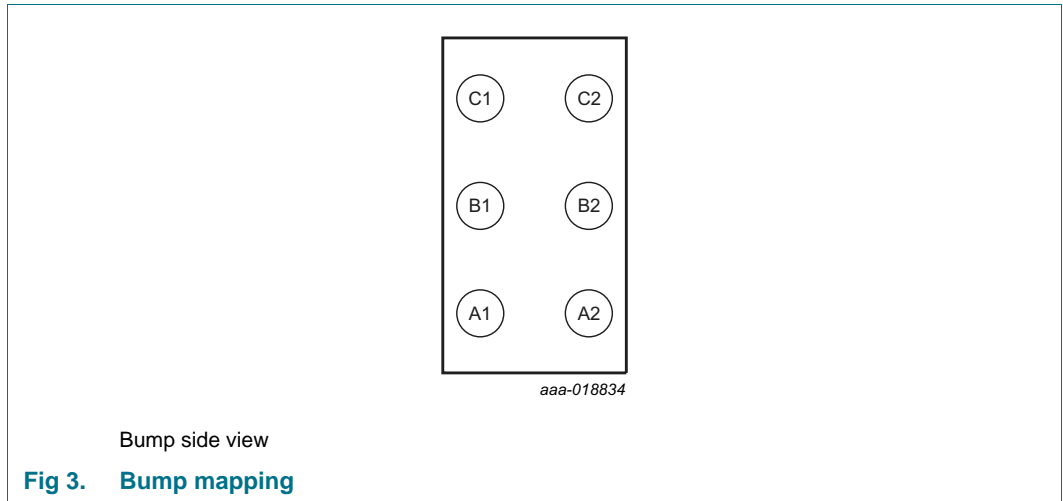


7. Block diagram



8. Pinning information

8.1 Pinning



8.2 Pin description

Table 5. Bump description

Symbol	Pad	Description
GND	A1	ground
V _{CC}	B1	supply voltage
RF_OUT	C1	RF out
CTRL	A2	gain control, switch between gain and bypass mode
RF_IN	B2	RF in
GND_RF	C2	ground RF

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Absolute Maximum Ratings are given as Limiting Values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{CC}	supply voltage	RF input AC coupled	[1]	-0.5	+5.0	V
V _{I(CTRL)}	input voltage on pin CTRL	V _{I(CTRL)} < V _{CC} + 0.6 V	[1][2]	-0.5	+5.0	V
V _{I(RF_IN)}	input voltage on pin RF_IN	DC; V _{I(RF_IN)} < V _{CC} + 0.6 V	[1][2][3]	-0.5	+5.0	V
V _{I(RF_OUT)}	input voltage on pin RF_OUT	DC; V _{I(RF_OUT)} < V _{CC} + 0.6 V	[1][2][3]	-0.5	+5.0	V
P _i	input power		[1]	-	10	dBm
P _{tot}	total power dissipation	T _{sp} ≤ 130 °C		-	55	mW
T _{stg}	storage temperature			-65	+150	°C

Table 6. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Absolute Maximum Ratings are given as Limiting Values of stress conditions during operation, that must not be exceeded under the worst probable conditions.

Symbol	Parameter	Conditions	Min	Max	Unit
T_j	junction temperature		-	150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001	-	±2	kV
		Charged Device Model (CDM) according to JEDEC standard JESD22-C101C	-	±1	kV

[1] Stressed with pulses of 200 ms in duration.

[2] Warning: Due to internal ESD diode protection, to avoid excess current, the applied DC voltage must not exceed $V_{CC} + 0.6\text{ V}$ or 5.0 V.

[3] The RF input and output are AC coupled through internal DC blocking capacitors.

10. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		-40	+25	+85	°C
$V_{I(CTRL)}$	input voltage on pin CTRL	OFF state	-	-	0.25	V
		ON state	0.8	-	-	V

11. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		225	K/W

12. Characteristics

Table 9. Characteristics

720 MHz ≤ f ≤ 960 MHz; $V_{CC} = 1.8\text{ V}$; $V_{I(CTRL)} \geq 0.8\text{ V}$; $T_{amb} = 25^\circ\text{C}$. Input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see [Figure 4](#). Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Gain mode							
I_{CC}	supply current	$V_{I(CTRL)} \geq 0.8\text{ V}$	-	5.5	-	mA	
G_p	power gain	f = 740 MHz	[1]	-	15	-	dB
		f = 882 MHz	[2]	-	15	-	dB
		f = 943 MHz	[3]	-	15	-	dB
RL_{in}	input return loss	f = 740 MHz	[1]	-	9	-	dB
		f = 882 MHz	[2]	-	13.5	-	dB
		f = 943 MHz	[3]	-	15	-	dB

Table 9. Characteristics ...continued

720 MHz \leq f \leq 960 MHz; $V_{CC} = 1.8$ V; $V_{I(CTRL)} \geq 0.8$ V; $T_{amb} = 25^\circ\text{C}$. Input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see [Figure 4](#). Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RL _{out}	output return loss	f = 740 MHz [1]	-	15	-	dB
		f = 882 MHz [2]	-	15	-	dB
		f = 943 MHz [3]	-	14	-	dB
ISL	isolation	f = 740 MHz [1]	-	23	-	dB
		f = 882 MHz [2]	-	23	-	dB
		f = 943 MHz [3]	-	23	-	dB
NF	noise figure	f = 740 MHz [1][4]	-	0.9	-	dB
		f = 882 MHz [2][4]	-	0.9	-	dB
		f = 943 MHz [3][4]	-	0.95	-	dB
P _{i(1dB)}	input power at 1 dB gain compression	f = 740 MHz [1]	-	-9	-	dBm
		f = 882 MHz [2]	-	-8	-	dBm
		f = 943 MHz [3]	-	-8	-	dBm
IP _{3i}	input third-order intercept point	f = 740 MHz [1]	-	-1	-	dBm
		f = 882 MHz [2]	-	-1	-	dBm
		f = 943 MHz [3]	-	-1	-	dBm
t _{on}	turn-on time	time from V _{I(CTRL)} ON to 90 % of the gain	-	-	4	μs
t _{off}	turn-off time	time from V _{I(CTRL)} OFF to 10 % of the gain	-	-	1	μs
K	Rollett stability factor		1	-	-	-
Bypass mode						
I _{CC}	supply current	V _{I(CTRL)} < 0.3 V	-	-	1	μA
G _p	power gain	f = 740 MHz [1]	-	-1.7	-	dB
		f = 882 MHz [2]	-	-1.9	-	dB
		f = 943 MHz [3]	-	-2.1	-	dB
RL _{in}	input return loss	f = 740 MHz [1]	-	15.3	-	dB
		f = 882 MHz [2]	-	11.8	-	dB
		f = 943 MHz [3]	-	10.8	-	dB
RL _{out}	output return loss	f = 740 MHz [1]	-	13.5	-	dB
		f = 882 MHz [2]	-	12	-	dB
		f = 943 MHz [3]	-	11.5	-	dB

[1] E-UTRA operating band 17 (734 MHz to 746 MHz).

[2] E-UTRA operating band 5 (869 MHz to 894 MHz).

[3] E-UTRA operating band 8 (925 MHz to 960 MHz).

[4] PCB losses are subtracted.

Table 10. Characteristics

720 MHz ≤ f ≤ 960 MHz; V_{CC} = 2.8 V; V_{I(CTRL)} ≥ 0.8 V; T_{amb} = 25°C. Input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see [Figure 4](#). Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I _{CC}	supply current	V _{I(CTRL)} ≥ 0.8 V	-	5.7	-	mA
G _p	power gain	f = 740 MHz [1]	-	15	-	dB
		f = 882 MHz [2]	-	15	-	dB
		f = 943 MHz [3]	-	15	-	dB
RL _{in}	input return loss	f = 740 MHz [1]	-	9	-	dB
		f = 882 MHz [2]	-	13.5	-	dB
		f = 943 MHz [3]	-	15	-	dB
RL _{out}	output return loss	f = 740 MHz [1]	-	15	-	dB
		f = 882 MHz [2]	-	15	-	dB
		f = 943 MHz [3]	-	15	-	dB
ISL	isolation	f = 740 MHz [1]	-	23	-	dB
		f = 882 MHz [2]	-	23	-	dB
		f = 943 MHz [3]	-	23	-	dB
NF	noise figure	f = 740 MHz [1] [4]	-	0.90	-	dB
		f = 882 MHz [2] [4]	-	0.90	-	dB
		f = 943 MHz [3] [4]	-	0.95	-	dB
P _{i(1dB)}	input power at 1 dB gain compression	f = 740 MHz [1]	-	-3.5	-	dBm
		f = 882 MHz [2]	-	-3.5	-	dBm
		f = 943 MHz [3]	-	-3.5	-	dBm
IP3 _i	input third-order intercept point	f = 740 MHz [1]	-	0.5	-	dBm
		f = 882 MHz [2]	-	0.5	-	dBm
		f = 943 MHz [3]	-	0.5	-	dBm
t _{on}	turn-on time	time from V _{I(CTRL)} ON to 90 % of the gain	-	-	4	μs
t _{off}	turn-off time	time from V _{I(CTRL)} OFF to 10 % of the gain	-	-	1	μs
K	Rollett stability factor		1	-	-	-
Bypass mode						
I _{CC}	supply current	V _{I(CTRL)} < 0.3 V	-	-	1	μA
G _p	power gain	f = 740 MHz [1]	-	-1.6	-	dB
		f = 882 MHz [2]	-	-1.8	-	dB
		f = 943 MHz [3]	-	-2.0	-	dB
RL _{in}	input return loss	f = 740 MHz [1]	-	15.0	-	dB
		f = 882 MHz [2]	-	11.5	-	dB
		f = 943 MHz [3]	-	10.5	-	dB

Table 10. Characteristics ...continued

720 MHz ≤ f ≤ 960 MHz; V_{CC} = 2.8 V; V_{I(CTRL)} ≥ 0.8 V; T_{amb} = 25°C. Input matched to 50 Ω using a 8.2 nH Murata LQW15 type inductor connected in series; see [Figure 4](#). Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RL _{out}	output return loss	f = 740 MHz	[1]	-	14	- dB
		f = 882 MHz	[2]	-	12	- dB
		f = 943 MHz	[3]	-	11.5	- dB

- [1] E-UTRA operating band 17 (734 MHz to 746 MHz).
- [2] E-UTRA operating band 5 (869 MHz to 894 MHz).
- [3] E-UTRA operating band 8 (925 MHz to 960 MHz).
- [4] PCB losses are subtracted.

13. Application information

13.1 LTE LNA

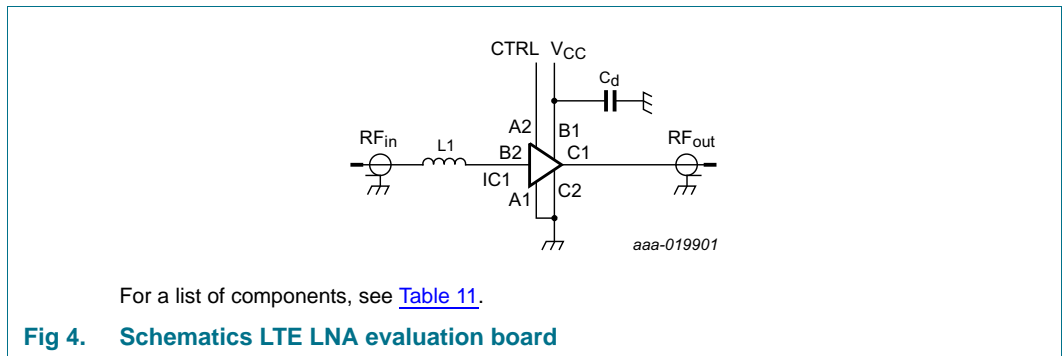


Table 11. List of components

For schematics, see [Figure 4](#).

Component	Description	Value	Remarks
C _d	decoupling capacitor	1 μF	Required to suppress power supply noise
IC1	BGS8L3UK	-	NXP Semiconductors N.V.
L1	high-quality matching inductor	8.2 nH	Murata LQW15A

14. Package outline

WLCSP6: wafer level chip-scale package; 6 bumps; 0.69 x 0.44 x 0.29 mm

SOT1445-1

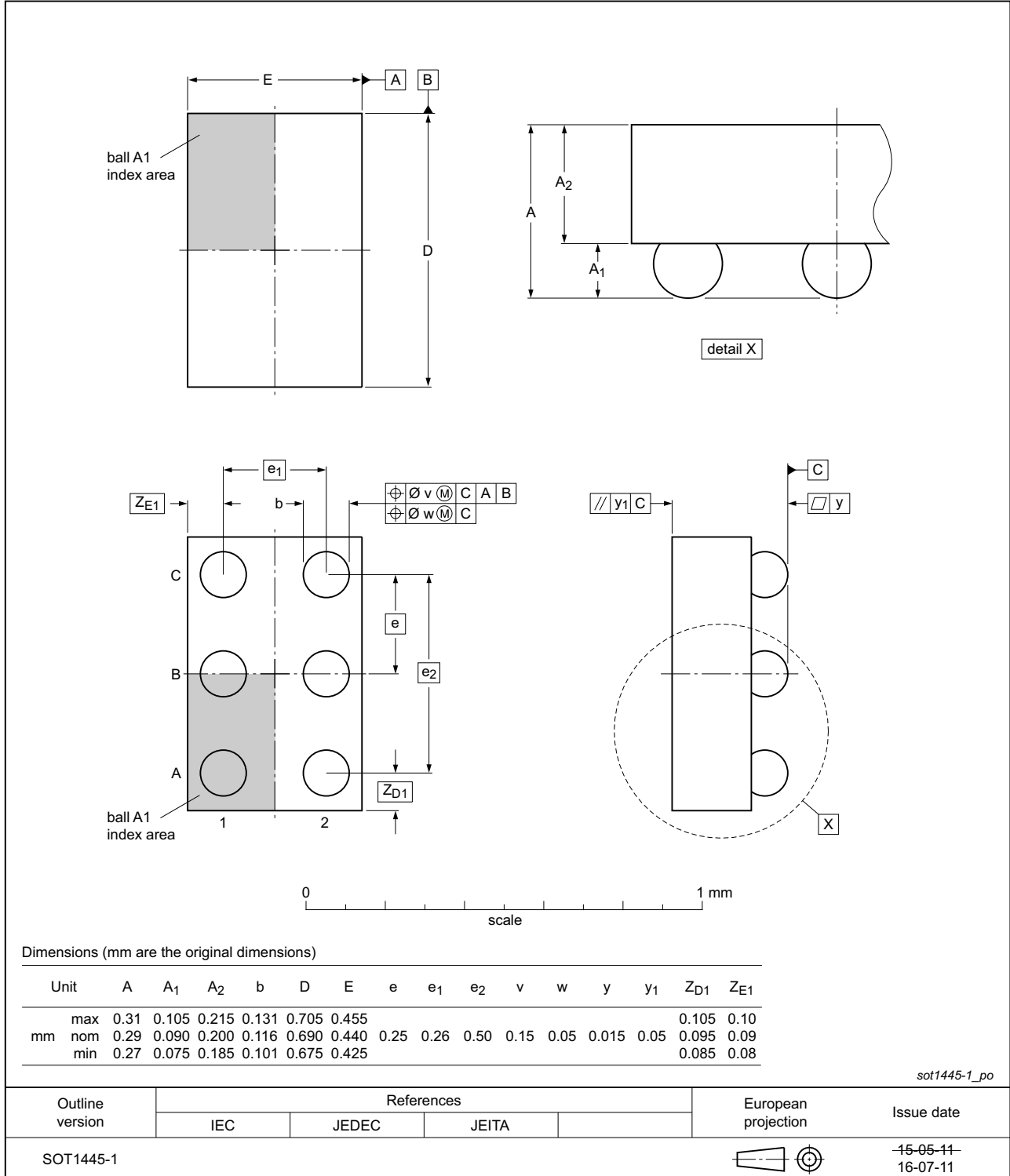


Fig 5. Package outline SOT1445-1 (WLCSP6)

15. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

16. Mounting

This WLCSP is only to be used in an over-molded module (using MUF)

17. Abbreviations

Table 12. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MUF	Molded Underfill
PCB	Printed-Circuit Board
SiGe:C	Silicon Germanium Carbon

18. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGS8L3UK v.1	20161115	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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