NT1GT72U89D0BV / NT2GT72U4PD0BV / NT4GT72U4ND0BV
NT2GT72U8PD0BV
1GB: 128M x 72 / 2GB: 256M x 72 / 4GB: 512M x 72
PC2-5300 / PC3-6400
Registered DDR2 SDRAM DIMM

Based on DDR2-667/800 128Mx8 (1GB/2GB) and 256MX4 (2GB/4GB) SDRAM D-Die

Features

- 1GB/2GB: 128Mx72/256Mx72 Registered DDR2 DIMM based on 128Mx8 DDR2 SDRAM. (NT5TU128M8DE)
- 2GB/4GB: 256Mx72/512MX72 Registered DDR2 DIMM based on 256Mx4 DDR2 SDRAM. (NT5TU256M4DE)
- 240-Pin Registered Dual In-Line Memory Module (RDIMM)
- Error Check Correction (ECC) Support
- Phase-lock loop (PLL) clock driver to reduce loading
- Performance:

Speed Sort	PC2-5300	PC2-6400	Unit
	-3C	-AD	
DIMM $\overline{CAS}$ Latency	5	6	
fck – Clock Freqency	333	400	MHz
tck – Clock Cycle	3	2.5	ns
fDQ – DQ Burst Freqency	667	800	Mbps

- Intended for 333MHz & 400MHz applications
- Inputs and outputs are SSTL-18 compatible
- V_{DD} = 1.8Volt ± 0.1Volt, V_{DDQ} = 1.8Volt ± 0.1Volt
- SDRAMs have 8 internal banks for concurrent operation
- One clock cycle added for registered DIMMs to account for input register
- Differential clock inputs
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Programmable Operation:
  - Device $\overline{CAS}$ Latency: 3,4,5,6
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/11/2 (row/column/rank) Addressing for 4GB
  14/11/1 (row/column/rank) Addressing for 2GB
  14/10/1 (row/column/rank) Addressing for 1GB/2GB
- Serial Presence Detect
- Gold contacts
- SDRAMs in 60-ball BGA Package
- RoHS Complianc

Description

NT1GT72U89D0BV, NT2GT72U4PD0BV, NT2GT72U8PD0BV and NT4GT72U4ND0BV are Registered 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as a one rank 128Mx72, 256Mx72 high-speed memory array and two ranks 512MX72 high-speed memory array. The module uses nine 128Mx8 (NT1GT72U89D0BV), eighteen 128Mx8 (NT2GT72U8PD0BV), eighteen 256Mx4 (NT2GT72U4PD0BV) and thirty-six 256Mx4 (NT4GT72U4ND0BV) DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25” long space-saving footprint.

The DIMM is intended for use in applications operating up to 333 MHz (or 400 MHz) clock speeds and achieves high-speed data transfer rates of up to 667Mbps (or 800Mbps). Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1, and BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power
NT1GT72U89D0BV-3C	333MHz (3ns @ CL = 5)	DDR2-667	PC2-5300	128Mx72	Gold	1.8V
NT2GT72U4PD0BV-3C				256Mx72		
NT2GT72U8PD0BV-3C				256Mx72		
NT4GT72U4ND0BV-3C				512Mx72		
NT1GT72U89D0BV-AD	400MHz (2.5ns @ CL = 6)	DDR2-800	PC2-6400	128Mx72		
NT2GT72U4PD0BV-AD				256Mx72		
NT2GT72U8PD0BV-AD				256Mx72		
NT4GT72U4ND0BV-AD				512Mx72		

Pin Description

Pin Name	Description	Pin Name	Description
CK0	Clock Input, positive line	ODT[1:0]	On Die Termination Inputs
$\overline{CK0}$	Clock input, negative line	DQ[63:0]	Data input/output
CKE[1:0]	Clock Enables	CB[7:0]	Data Check Bit Input/Output
$\overline{RAS}$	Row Address Strobe	DQS[8:0]	Data strobes
$\overline{CAS}$	Column Address Strobe	$\overline{DQS}$[8:0]	Data strobes / negative line
$\overline{WE}$	Write Enable	DM[8:0] / DQS[17:9]	Data Masks / Data strobes
$\overline{S}$[1:0]	Chip Selects	$\overline{DQS}$[17:9]	Data strobes / negative line
A[9:0], A[13:11]	Address Inputs	RFU	Reserved for Future use
A10/AP	Address Input/Autoprecharge	NC	No Connect
BA[2:0]	SDRAM Bank Addresses	TEST	Memory bus test tool
SCL	Serial Presence Detect (SPD) Clock Input	V_{DDSPD}	Serial EEPROM positive power supply
SDA	SPD Data Input/Output	V_{SS}	Ground
SA[2:0]	SPD Address Inputs	V_{DD}	Core Power
Par_In	Parity bit for the Address and Control bus	V_{DDQ}	I/O Power
$\overline{Err\_Out}$	Parity error found on the Address and Control bus	VREF	Input/Output Reference
$\overline{RESET}$	Register and PLL control pin		

DDR2 SDRAM Pin Assignment

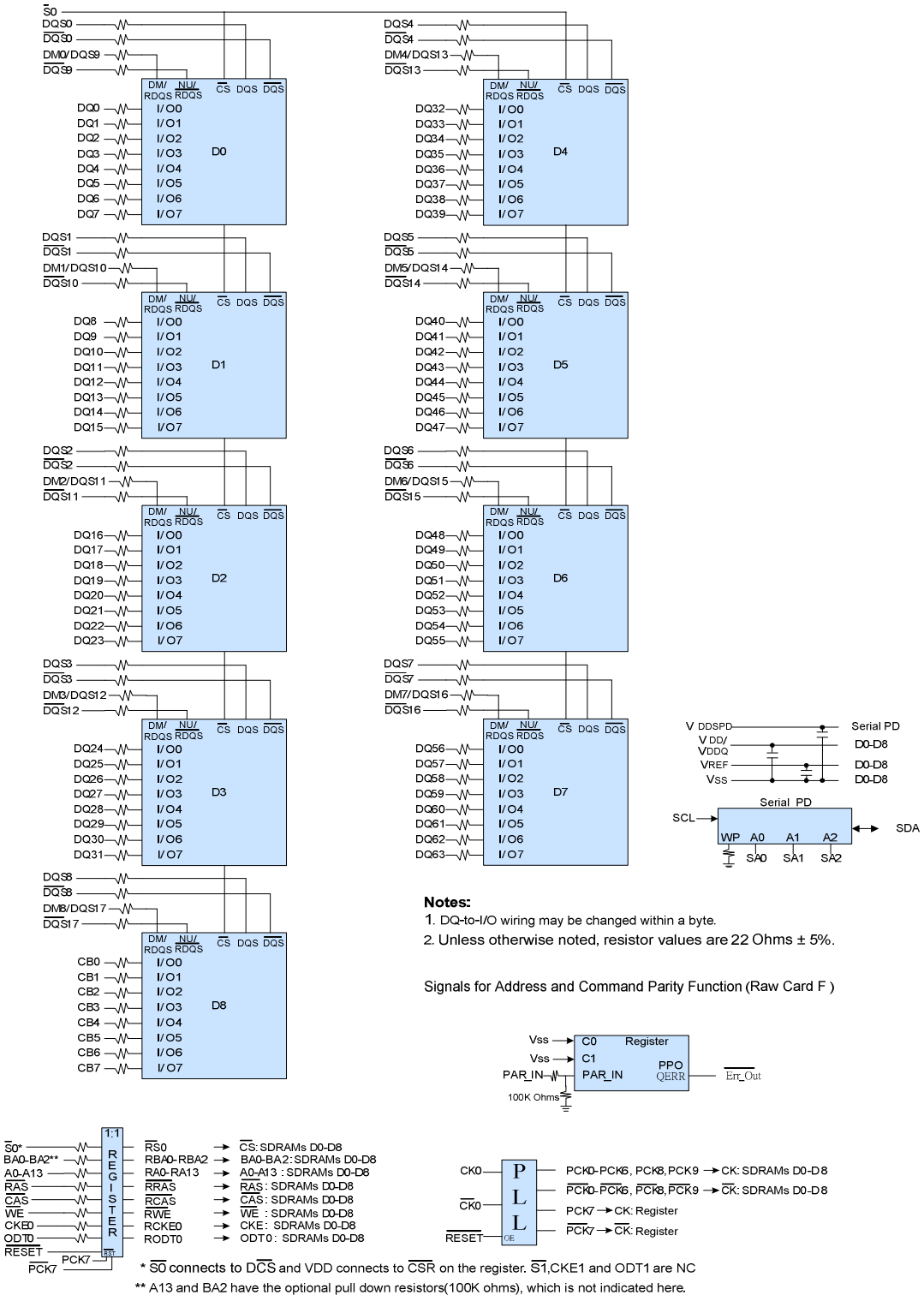
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	42	CB0	82	VSS	121	VSS	162	CB5	202	DM4/DQS13
2	VSS	43	CB1	83	$\overline{DQS4}$	122	DQ4	163	VSS	203	NC, $\overline{DQS13}$
3	DQ0	44	VSS	84	DQS4	123	DQ5	164	DM8/DQS17	204	VSS
4	DQ1	45	$\overline{DQS8}$	85	VSS	124	VSS	165	NC, $\overline{DQS17}$	205	DQ38
5	VSS	46	DQS8	86	DQ34	125	DM0 / DQS9	166	VSS	206	DQ39
6	$\overline{DQS0}$	47	VSS	87	DQ35	126	NC, $\overline{DQS9}$	167	CB6	207	VSS
7	DQS0	48	CB2	88	VSS	127	VSS	168	CB7	208	DQ44
8	VSS	49	CB3	89	DQ40	128	DQ6	169	VSS	209	DQ45
9	DQ2	50	VSS	90	DQ41	129	DQ7	170	VDDQ	210	VSS
10	DQ3	51	VDDQ	91	VSS	130	VSS	171	NC,CKE1	211	DM5/DQS14
11	VSS	52	CKE0	92	$\overline{DQS5}$	131	DQ12	172	VDD	212	NC, $\overline{DQS14}$
12	DQ8	53	VDD	93	DQS5	132	DQ13	173	NC	213	VSS
13	DQ9	54	BA2	94	VSS	133	VSS	174	NC	214	DQ46
14	VSS	55	$\overline{Err\_Out}$	95	DQ42	134	DM1/DQS10	175	VDDQ	215	DQ47
15	$\overline{DQS1}$	56	VDDQ	96	DQ43	135	NC, $\overline{DQS10}$	176	A12	216	VSS
16	DQS1	57	A11	97	VSS	136	VSS	177	A9	217	DQ52
17	VSS	58	A7	98	DQ48	137	RFU	178	VDD	218	DQ53
18	$\overline{RESET}$	59	VDD	99	DQ49	138	RFU	179	A8	219	VSS
19	NC	60	A5	100	VSS	139	VSS	180	A6	220	RFU
20	VSS	61	A4	101	SA2	140	DQ14	181	VDDQ	221	RFU
21	DQ10	62	VDDQ	102	NC	141	DQ15	182	A3	222	VSS
22	DQ11	63	A2	103	VSS	142	VSS	183	A1	223	DM6/DQS15
23	VSS	64	VDD	104	$\overline{DQS6}$	143	DQ20	184	VDD	224	NC, $\overline{DQS15}$
24	DQ16	KEY		105	DQS6	144	DQ21	KEY		225	VSS
25	DQ17	65	VSS	106	VSS	145	VSS	185	CK0	226	DQ54
26	VSS	66	VSS	107	DQ50	146	DM2/DQS11	186	$\overline{CK0}$	227	DQ55
27	$\overline{DQS2}$	67	VDD	108	DQ51	147	NC, $\overline{DQS11}$	187	VDD	228	VSS
28	DQS2	68	Par_In	109	VSS	148	VSS	188	A0	229	DQ60
29	VSS	69	VDD	110	DQ56	149	DQ22	189	VDD	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	VSS
31	DQ19	71	BA0	112	VSS	151	VSS	191	VDDQ	232	DM7/DQS16
32	VSS	72	VDDQ	113	$\overline{DQS7}$	152	DQ28	192	$\overline{RAS}$	233	NC, $\overline{DQS16}$
33	DQ24	73	$\overline{WE}$	114	DQS7	153	DQ29	193	$\overline{S0}$	234	VSS
34	DQ25	74	$\overline{CAS}$	115	VSS	154	VSS	194	VDDQ	235	DQ62
35	Vss	75	VDDQ	116	DQ58	155	DM3/DQS12	195	ODT0	236	DQ63
36	$\overline{DQS3}$	76	NC, $\overline{S1}$	117	DQ59	156	NC, $\overline{DQS12}$	196	A13	237	VSS
37	DQS3	77	NC, ODT1	118	VSS	157	VSS	197	VDD	238	VDDSPD
38	Vss	78	VDDQ	119	SDA	158	DQ30	198	VSS	239	SA0
39	DQ26	79	Vss	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	VSS	200	DQ37		
41	Vss	81	DQ33			161	CB4	201	VSS		

Note: NC = No Connect; RFU = Reserved Future Use
ODT1, CKE1, $\overline{S1}$ = for4GB module uses only
DQS9~DQS17 & $\overline{DQS9}$~$\overline{DQS17}$ = for 2GB/4GB modules use only

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
$\overline{S}$[1:0]	IN	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both [0:1] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state. For modules supporting 4 ranks, [2:3] operate similarly to [0:1] for a second set of register outputs.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR2 SDRAM output buffers to provide improved noise immunity
ODT[1:0]	IN	Active High	On-Die Termination control signals
BA[2:0]	IN	-	Selects which SDRAM bank is to be active.
A[13:11,10/AP,9:0]	IN	-	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1,BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1 or BA2. If AP is low, BA0 and BA1 and BA2 are used to define which bank to precharge.
DQ[63:0] CB[7:0]	I/O	-	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR2 SDRAM input buffers and core logic
DQS[17:0]	I/O	Positive Edge	Data strobe for input and output data
$\overline{DQS}$[17:0]	I/O	Negative Edge	Data strobe for input and output data
DM[8:0]	I/O	Active High	Masks write data when high, issued concurrently with input data.
$\overline{RESET}$	IN	Active Low	The $\overline{RESET}$ pin is connected to the $\overline{RST}$ pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be nset to low level (the PLL will remain synchronized with the input clock)
SA[2:0]	IN	-	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull-up.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 Volt to 3.6 Volt (nominal 1.8 Volt, 2.5 Volt and 3.3 Volt) operation.
Par_In	IN	-	Parity bit for the Address and Control bus. (1 for Odd, 0 for Even)
$\overline{Err\_Out}$	OUT	-	Parity error found in the Address and Control bus.

Functional Block Diagram: Raw Card Version F [1GB, 1Rank, 128Mx8 DDR2 SDRAMs]



Notes:

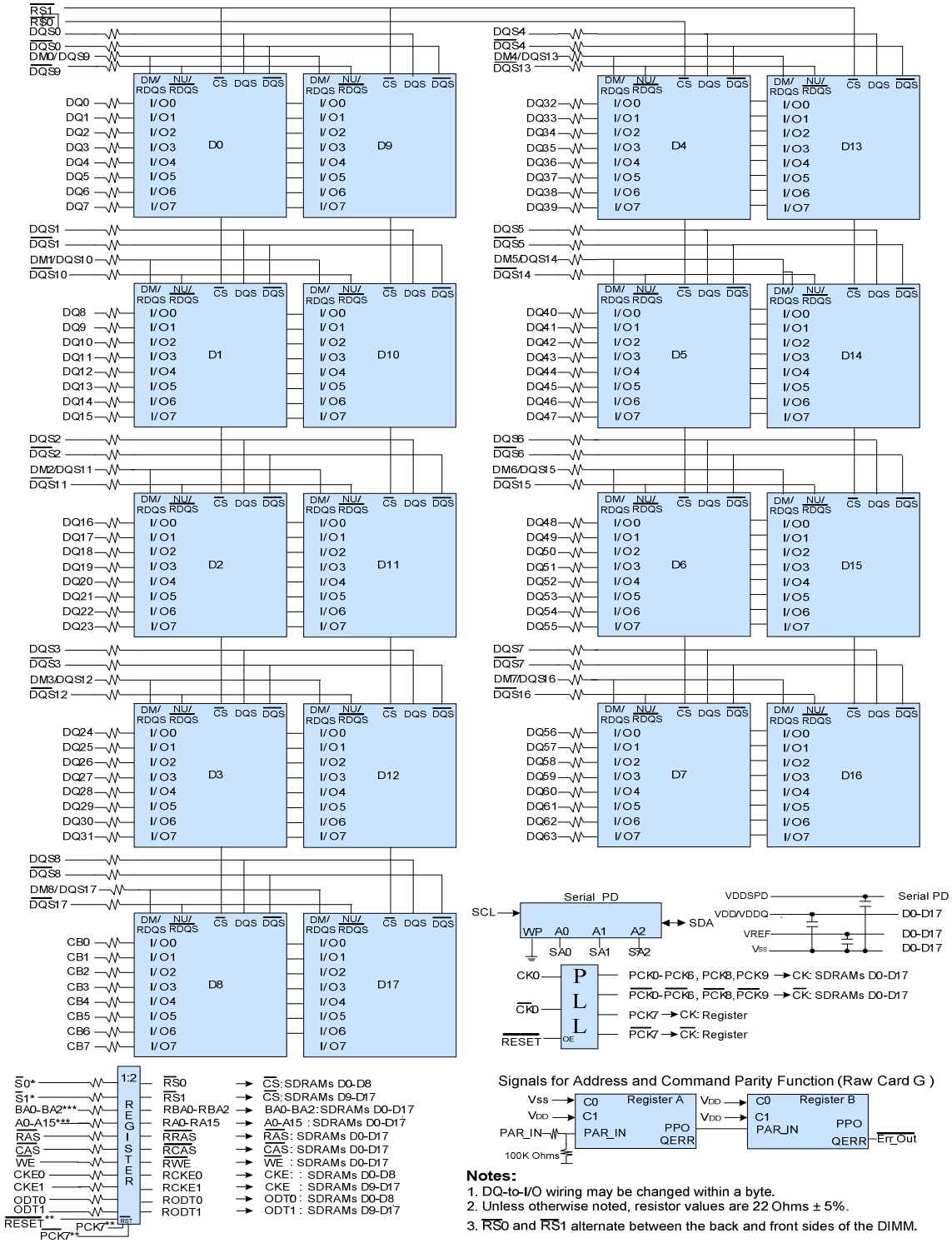
1. DQ-to-I/O wiring may be changed within a byte.
2. Unless otherwise noted, resistor values are 22 Ohms ± 5%.

Signals for Address and Command Parity Function (Raw Card F)

* S0 connects to DCS and VDD connects to CSR on the register. S1,CKE1 and ODT1 are NC

** A13 and BA2 have the optional pull down resistors(100K ohms), which is not indicated here.

Functional Block Diagram: Raw Card Version G [2GB, 2Rank, 128Mx8 DDR2 SDRAMs]

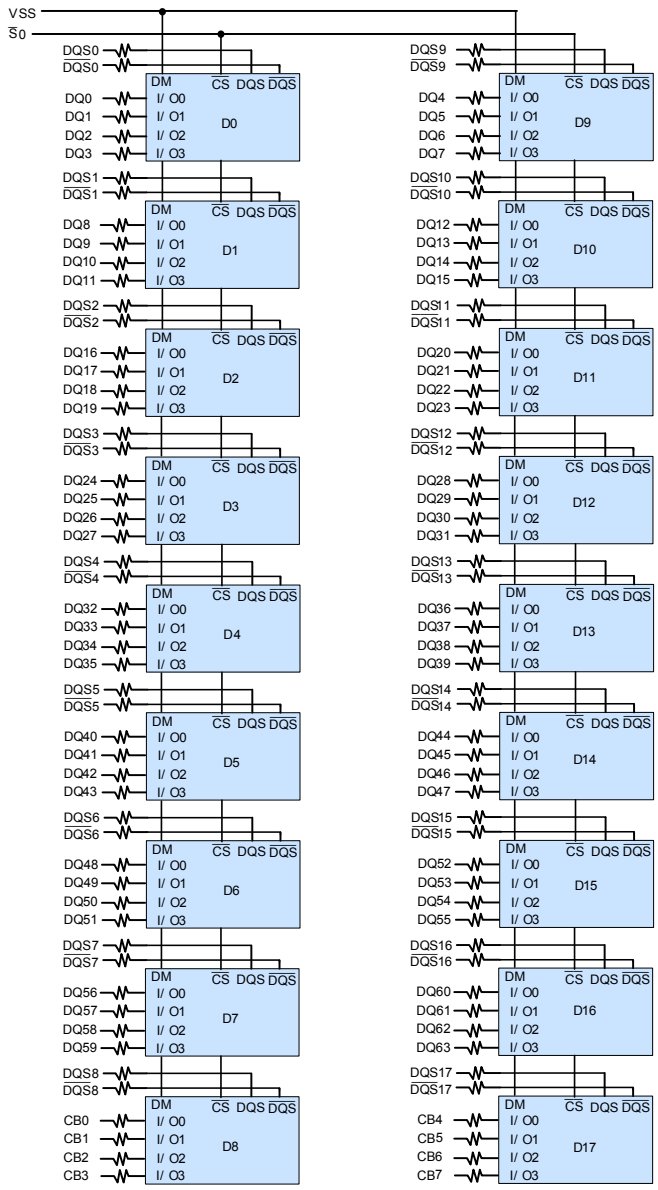


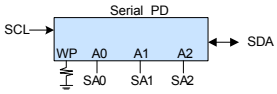
Notes:

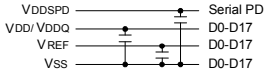
1. DQ-to-I/O wiring may be changed within a byte.
2. Unless otherwise noted, resistor values are 22 Ohms ± 5%.
3. $\overline{RS0}$ and $\overline{RS1}$ alternate between the back and front sides of the DIMM.

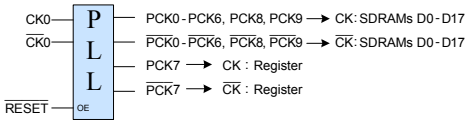
* $\overline{S0}$ connects to $\overline{DCS}$ and $\overline{S1}$ connects to $\overline{CSR}$ on a Register. $\overline{S1}$ connects to $\overline{DCS}$ and $\overline{S0}$ connects to $\overline{CSR}$ on another Register.
** $\overline{RESET}$, PCK7 and $\overline{PCK7}$ connect to both Registers. Other signals connect to one of two Registers.
*** A13-15 and BA2 have the optional pull down resistors(100K ohms), which is not indicated here.

Functional Block Diagram: Raw Card Version H [2GB, 1Rank, 256Mx4 DDR2 SDRAMs]







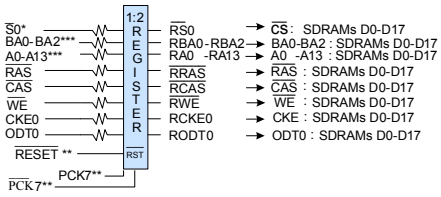


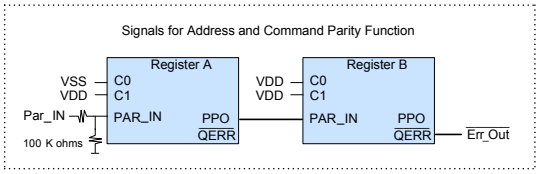
Notes:
1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 22 Ohms ± 5%

* S0 connects to DCS of Register A and CSR of Register B.
CSR of Register A and DCS of Register B connects to VDD.

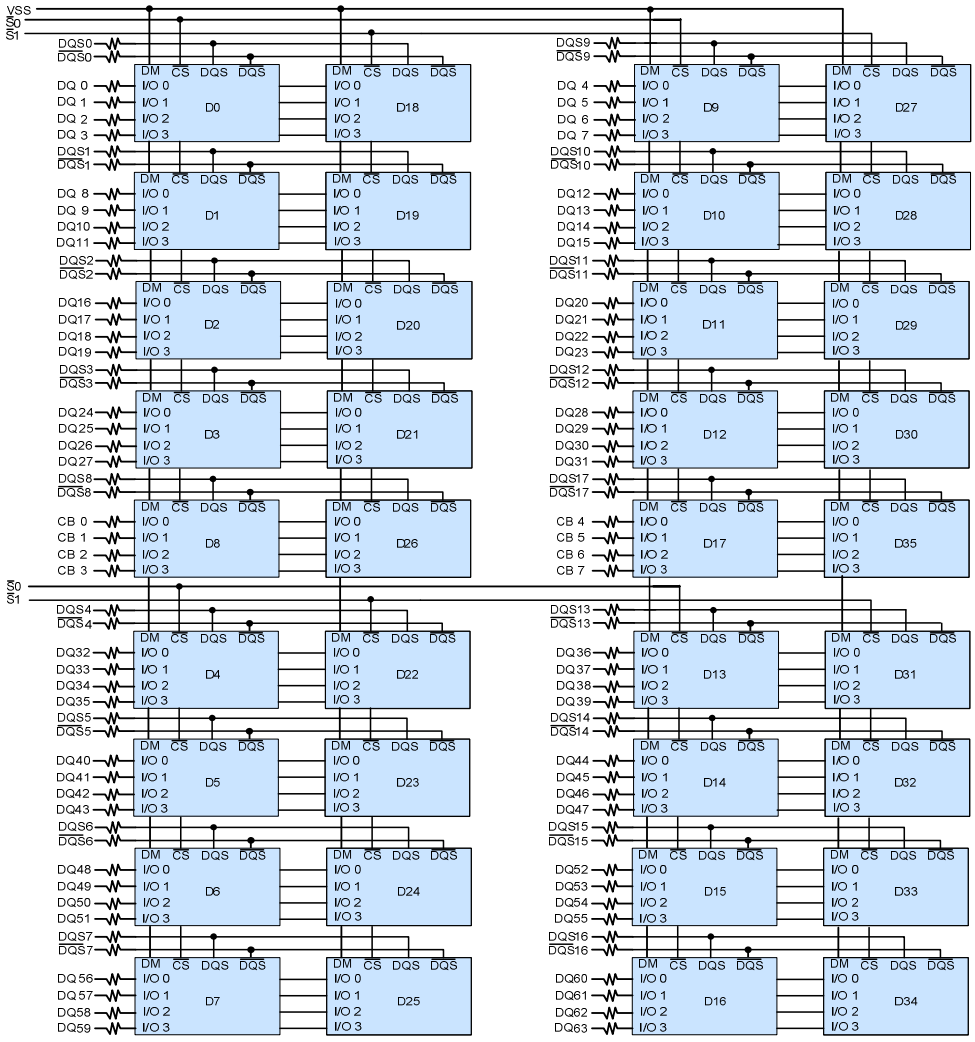
** RESET, PCK7 and PCK7 connect to both Registers.
Other signals connect to one of two Registers.

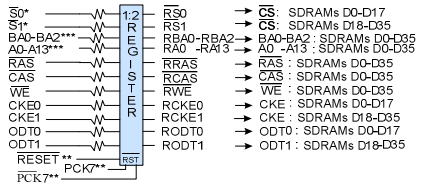
*** A13 and BA2 have the optional pull down resistors (100K ohms), which is not indicated here.

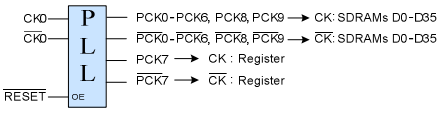


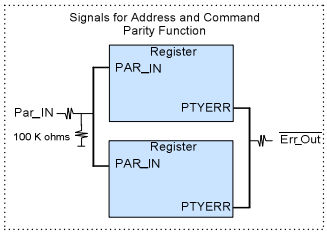


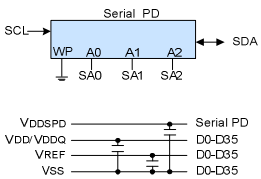
Functional Block Diagram: Raw Card Version AF [4GB, 2Ranks, 256Mx4 DDR2 SDRAMs]











* $\overline{S0}$ connects to $\overline{DCS}$ and $\overline{S1}$ connects to $\overline{CSR}$ on a pair of Registers. $\overline{S1}$ connects to $\overline{DCS}$ and $\overline{S0}$ connects to $\overline{CSR}$ on another pair of Registers.
** $\overline{RESET}$, PCK7 and $\overline{PCK7}$ connect to all Registers. Other signals connect to one pair of four Registers.
*** A13 and BA2 have the optional pull down resistors (100K ohms), which is not indicated here.

Notes:
1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 22 Ohms ± 5%
3. $\overline{RS0}$ and $\overline{RS1}$ alternate between the bottom and surface sides of the DIMM.

Serial Presence Detect (Part 1 of 2) **[NT1GT72U89D0BV, 1GB – 1 Rank, 128Mx8 DDR2 SDRAMs]**

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-3C	-AD	-3C	-AD
0	Number of Serial PD Bytes Written during Production	128	128	80	80
1	Total Number of Bytes in Serial PD device	256	256	08	08
2	Fundamental Memory Type	DDR2 SDRAM	DDR2 SDRAM	08	08
3	Number of Row Addresses on Assembly	14	14	0E	0E
4	Number of Column Addresses on Assembly	10	10	0A	0A
5	Number of DIMM Ranks	Module Height = 30.0mm, 1 rank	Module Height = 30.0mm, 1 rank	60	60
6	Data Width of Assembly	X72	X72	48	48
7	Reserved	Undefined	Undefined	00	00
8	Voltage Interface Level of this Assembly	SSTL 1.8V	SSTL 1.8V	05	05
9	DDR2 SDRAM Device Cycle Time at CL=X	3ns	2.5ns	30	25
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45ns	0.4ns	45	40
11	DIMM Configuration Type	Address/Command Parity, Data ECC, Non Data Parity,	Address/Command Parity, Data ECC, Non Data Parity,	06	06
12	Refresh Rate/Type	7.8 µs	7.8 µs	82	82
13	Primary DDR2 SDRAM Width	X8	X8	08	08
14	Error Checking DDR2 SDRAM Device Width	X8	X8	08	08
15	Reserved	Undefined	Undefined	00	00
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8	4,8	0C	0C
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8	8	08	08
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5	4,5,6	38	70
19	DIMM Mechanical Characteristics	x ≤ 4.10 (mm)	x ≤ 4.10 (mm)	01	01
20	DDR2 SDRAM DIMM Type Information	RDIMM (133.35mm)	RDIMM (133.35mm)	01	01
21	DDR2 SDRAM Module Attributes:	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 1, Number of Active Registers : 1,	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 1, Number of Active Registers : 1,	04	04
22	DDR2 SDRAM Device Attributes: General	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,	07	07
23	Minimum Clock Cycle at CL=X-1	3.75ns	3ns	3D	30
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns	0.45ns	50	45
25	Minimum Clock Cycle Time at CL=X-2	5ns	3.75ns	50	3D
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns	0.5ns	60	50
27	Minimum Row Precharge Time (t_{RP})	15ns	15ns	3C	3C
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns	7.5ns	1E	1E
29	Minimum RAS to CAS delay (t_{RCD})	15ns	15ns	3C	3C
30	Minimum RAS Pulse Width (t_{RAS})	45ns	45ns	2D	2D
31	Module Bank Density	1GB	1GB	01	01
32	Address and Command Setup Time Before Clock (t_{IS})	0.2ns	0.17ns	20	17
33	Address and Command Hold Time After Clock (t_{IH})	0.27ns	0.25ns	27	25
34	Data Input Setup Time Before Clock (t_{DS})	0.1ns	0.05ns	10	05
35	Data Input Hold Time After Clock (t_{DH})	0.17ns	0.12ns	17	12
36	Write Recovery Time (t_{WR})	15ns	15ns	3C	3C
37	Internal Write to Read Command delay (t_{WTR})	7.5ns	7.5ns	1E	1E
38	Internal Read to Precharge delay (t_{RTP})	7.5ns	7.5ns	1E	1E
39	Reserved	Undefined	Undefined	00	00
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	06	06
41	Minimum Core Cycle Time (t_{RC})	60ns	60ns	3C	3C
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	127.5ns	127.5ns	7F	7F
43	Maximum Clock Cycle Time (t_{CK})	8ns	8ns	80	80
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.24ns	0.2ns	18	14
45	Read Data Hold Skew Factor (t_{QHS})	0.34ns	0.3ns	22	1E
46	PLL Relock Time	15µs	15µs	0F	0F
47	Tcasemax, DT4R4W Delta	Undefined	Undefined	00	00
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	Undefined	Undefined	00	00
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Undefined	Undefined	00	00
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Undefined	Undefined	00	00
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	Undefined	Undefined	00	00
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Undefined	Undefined	00	00
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	Undefined	Undefined	00	00

Serial Presence Detect (Part 1 of 2) **[NT1GT72U89D0BV, 1GB – 1 Rank, 128Mx8 DDR2 SDRAMs]**

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-3C	-AD	-3C	-AD
0	Number of Serial PD Bytes Written during Production	128	128	80	80
1	Total Number of Bytes in Serial PD device	256	256	08	08
2	Fundamental Memory Type	DDR2 SDRAM	DDR2 SDRAM	08	08
3	Number of Row Addresses on Assembly	14	14	0E	0E
4	Number of Column Addresses on Assembly	10	10	0A	0A
5	Number of DIMM Ranks	Module Height = 30.0mm, 1 rank	Module Height = 30.0mm, 1 rank	60	60
6	Data Width of Assembly	X72	X72	48	48
7	Reserved	Undefined	Undefined	00	00
8	Voltage Interface Level of this Assembly	SSTL 1.8V	SSTL 1.8V	05	05
9	DDR2 SDRAM Device Cycle Time at CL=X	3ns	2.5ns	30	25
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45ns	0.4ns	45	40
11	DIMM Configuration Type	Address/Command Parity, Data ECC, Non Data Parity,	Address/Command Parity, Data ECC, Non Data Parity,	06	06
12	Refresh Rate/Type	7.8 µs	7.8 µs	82	82
13	Primary DDR2 SDRAM Width	X8	X8	08	08
14	Error Checking DDR2 SDRAM Device Width	X8	X8	08	08

Serial Presence Detect (Part 1 of 2) [NT2GT72U4PD0BV, 2GB – 1 Rank, 256Mx4 DDR2 SDRAMs]

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-3C	-AD	-3C	-AD
0	Number of Serial PD Bytes Written during Production	128	128	80	80
1	Total Number of Bytes in Serial PD device	256	256	08	08
2	Fundamental Memory Type	DDR2 SDRAM	DDR2 SDRAM	08	08
3	Number of Row Addresses on Assembly	14	14	0E	0E
4	Number of Column Addresses on Assembly	11	11	0B	0B
5	Number of DIMM Ranks	Module Height = 30.0mm, 1 rank	Module Height = 30.0mm, 1 rank	60	60
6	Data Width of Assembly	X72	X72	48	48
7	Reserved	Undefined	Undefined	00	00
8	Voltage Interface Level of this Assembly	SSTL 1.8V	SSTL 1.8V	05	05
9	DDR2 SDRAM Device Cycle Time at CL=X	3ns	2.5ns	30	25
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45ns	0.4ns	45	40
11	DIMM Configuration Type	Address/Command Parity, Data ECC, Non Data Parity,	Address/Command Parity, Data ECC, Non Data Parity,	06	06
12	Refresh Rate/Type	7.8 µs	7.8 µs	82	82
13	Primary DDR2 SDRAM Width	X4	X4	04	04
14	Error Checking DDR2 SDRAM Device Width	X4	X4	04	04
15	Reserved	Undefined	Undefined	00	00
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8	4,8	0C	0C
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8	8	08	08
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5	4,5,6	38	70
19	DIMM Mechanical Characteristics	x ≤ 4.10 (mm)	x ≤ 4.10 (mm)	01	01
20	DDR2 SDRAM DIMM Type Information	RDIMM (133.35mm)	RDIMM (133.35mm)	01	01
21	DDR2 SDRAM Module Attributes:	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 1, Number of Active Registers : 2,	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 1, Number of Active Registers : 2,	05	05
22	DDR2 SDRAM Device Attributes: General	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,	07	07
23	Minimum Clock Cycle at CL=X-1	3.75ns	3ns	3D	30
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns	0.45ns	50	45
25	Minimum Clock Cycle Time at CL=X-2	5ns	3.75ns	50	3D
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns	0.5ns	60	50
27	Minimum Row Precharge Time (t_{RP})	15ns	15ns	3C	3C
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns	7.5ns	1E	1E
29	Minimum RAS to CAS delay (t_{RCD})	15ns	15ns	3C	3C
30	Minimum RAS Pulse Width (t_{RAS})	45ns	45ns	2D	2D
31	Module Bank Density	2GB	2GB	02	02
32	Address and Command Setup Time Before Clock (t_{IS})	0.2ns	0.17ns	20	17
33	Address and Command Hold Time After Clock (t_{IH})	0.27ns	0.25ns	27	25
34	Data Input Setup Time Before Clock (t_{DS})	0.1ns	0.05ns	10	05
35	Data Input Hold Time After Clock (t_{DH})	0.17ns	0.12ns	17	12
36	Write Recovery Time (t_{WR})	15ns	15ns	3C	3C
37	Internal Write to Read Command delay (t_{WTR})	7.5ns	7.5ns	1E	1E
38	Internal Read to Precharge delay (t_{RTP})	7.5ns	7.5ns	1E	1E
39	Reserved	Undefined	Undefined	00	00
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	06	06
41	Minimum Core Cycle Time (t_{RC})	60ns	60ns	3C	3C
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	127.5ns	127.5ns	7F	7F
43	Maximum Clock Cycle Time (t_{CK})	8ns	8ns	80	80
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.24ns	0.2ns	18	14
45	Read Data Hold Skew Factor (t_{QHS})	0.34ns	0.3ns	22	1E
46	PLL Relock Time	15µs	15µs	0F	0F
47	Tcasemax, DT4R4W Delta	Undefined	Undefined	00	00
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	Undefined	Undefined	00	00
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Undefined	Undefined	00	00
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Undefined	Undefined	00	00
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	Undefined	Undefined	00	00
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Undefined	Undefined	00	00
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	Undefined	Undefined	00	00

Serial Presence Detect (Part 1 of 2) **[NT2GT72U4PD0BV, 2GB – 1 Rank, 256Mx4 DDR2 SDRAMs]**

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-3C	-AD	-3C	-AD
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	Undefined	Undefined	00	00
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	Undefined	Undefined	00	00
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	Undefined	Undefined	00	00
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	Undefined	Undefined	00	00
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	Undefined	Undefined	00	00
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	Undefined	Undefined	00	00
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	Undefined	Undefined	00	00
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	Undefined	Undefined	00	00
62	SPD Revision	1.3	1.3	13	13
63	Checksum for Byte 0-62	Checksum Data	Checksum Data	3A	04
64-71	Manufacturer's JEDEC ID Code	Nanya	Nanya	7F7F7F0B00000000	
72	Module Manufacturing Location	Manufacturing code	Manufacturing code	--	--
73-91	Module Part Number	Module Part Number in ASCII	Module Part Number in ASCII	--	--
92-255	Reserved	Undefined	Undefined	--	--

Note1:
NT2GT72U4PD0BV-3C -> 4E5432475437325534504430425 62D33432020
NT2GT72U4PD0BV-AD -> 4E5432475437325534504430425 62D41442020

Serial Presence Detect (Part 1 of 2) [NT2GT72U8PD0BV, 2GB – 2 Ranks, 128Mx8 DDR2 SDRAMs]

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-3C	-AD	-3C	-AD
0	Number of Serial PD Bytes Written during Production	128	128	80	80
1	Total Number of Bytes in Serial PD device	256	256	08	08
2	Fundamental Memory Type	DDR2 SDRAM	DDR2 SDRAM	08	08
3	Number of Row Addresses on Assembly	14	14	0E	0E
4	Number of Column Addresses on Assembly	10	10	0A	0A
5	Number of DIMM Ranks	Module Height = 30.0mm, 2 ranks	Module Height = 30.0mm, 2 ranks	61	61
6	Data Width of Assembly	X72	X72	48	48
7	Reserved	Undefined	Undefined	00	00
8	Voltage Interface Level of this Assembly	SSTL 1.8V	SSTL 1.8V	05	05
9	DDR2 SDRAM Device Cycle Time at CL=X	3ns	2.5ns	30	25
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45ns	0.4ns	45	40
11	DIMM Configuration Type	Address/Command Parity, Data ECC, Non Data Parity,	Address/Command Parity, Data ECC, Non Data Parity,	06	06
12	Refresh Rate/Type	7.8 µs	7.8 µs	82	82
13	Primary DDR2 SDRAM Width	X8	X8	08	08
14	Error Checking DDR2 SDRAM Device Width	X8	X8	08	08
15	Reserved	Undefined	Undefined	00	00
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8	4,8	0C	0C
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8	8	08	08
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5	4,5,6	38	70
19	DIMM Mechanical Characteristics	x ≤ 4.10 (mm)	x ≤ 4.10 (mm)	01	01
20	DDR2 SDRAM DIMM Type Information	RDIMM (133.35mm)	RDIMM (133.35mm)	01	01
21	DDR2 SDRAM Module Attributes:	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 1, Number of Active Registers : 2,	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 1, Number of Active Registers : 2,	05	05
22	DDR2 SDRAM Device Attributes: General	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,	07	07
23	Minimum Clock Cycle at CL=X-1	3.75ns	3ns	3D	30
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns	0.45ns	50	45
25	Minimum Clock Cycle Time at CL=X-2	5ns	3.75ns	50	3D
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns	0.5ns	60	50
27	Minimum Row Precharge Time (t_{RP})	15ns	15ns	3C	3C
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns	7.5ns	1E	1E
29	Minimum RAS to CAS delay (t_{RCD})	15ns	15ns	3C	3C
30	Minimum RAS Pulse Width (t_{RAS})	45ns	45ns	2D	2D
31	Module Bank Density	1GB	1GB	01	01
32	Address and Command Setup Time Before Clock (t_{IS})	0.2ns	0.17ns	20	17
33	Address and Command Hold Time After Clock (t_{IH})	0.27ns	0.25ns	27	25
34	Data Input Setup Time Before Clock (t_{DS})	0.1ns	0.05ns	10	05
35	Data Input Hold Time After Clock (t_{DH})	0.17ns	0.12ns	17	12
36	Write Recovery Time (t_{WR})	15ns	15ns	3C	3C
37	Internal Write to Read Command delay (t_{WTR})	7.5ns	7.5ns	1E	1E
38	Internal Read to Precharge delay (t_{RTP})	7.5ns	7.5ns	1E	1E
39	Reserved	Undefined	Undefined	00	00
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	06	06
41	Minimum Core Cycle Time (t_{RC})	60ns	60ns	3C	3C
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	127.5ns	127.5ns	7F	7F
43	Maximum Clock Cycle Time (t_{CK})	8ns	8ns	80	80
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.24ns	0.2ns	18	14
45	Read Data Hold Skew Factor (t_{QHS})	0.34ns	0.3ns	22	1E
46	PLL Relock Time	15µs	15µs	0F	0F
47	Tcasemax, DT4R4W Delta	Undefined	Undefined	00	00
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	Undefined	Undefined	00	00
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Undefined	Undefined	00	00
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Undefined	Undefined	00	00
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	Undefined	Undefined	00	00
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Undefined	Undefined	00	00
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	Undefined	Undefined	00	00

Serial Presence Detect (Part 1 of 2) **[NT2GT72U8PD0BV, 2GB – 2 Ranks, 128Mx8 DDR2 SDRAMs]**

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-3C	-AD	-3C	-AD
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	Undefined	Undefined	00	00
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	Undefined	Undefined	00	00
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	Undefined	Undefined	00	00
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	Undefined	Undefined	00	00
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	Undefined	Undefined	00	00
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	Undefined	Undefined	00	00
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	Undefined	Undefined	00	00
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	Undefined	Undefined	00	00
62	SPD Revision	1.3	1.3	13	13
63	Checksum for Byte 0-62	Checksum Data	Checksum Data	41	0B
64-71	Manufacturer's JEDEC ID Code	Nanya	Nanya	7F7F7F0B00000000	
72	Module Manufacturing Location	Manufacturing code	Manufacturing code	--	--
73-91	Module Part Number	Module Part Number in ASCII	Module Part Number in ASCII	--	--
92-255	Reserved	Undefined	Undefined	--	--

Note1:
NT2GT72U8PD0BV-3C -> 4E5432475437325538504430425 62D33432020
NT2GT72U8PD0BV-AD -> 4E5432475437325538504430425 62D41442020

Serial Presence Detect (Part 1 of 2) [NT4GT72U4ND0BV, 4GB – 2 Ranks, 256Mx4 DDR2 SDRAMs]

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-3C	-AD	-3C	-AD
0	Number of Serial PD Bytes Written during Production	128	128	80	80
1	Total Number of Bytes in Serial PD device	256	256	08	08
2	Fundamental Memory Type	DDR2 SDRAM	DDR2 SDRAM	08	08
3	Number of Row Addresses on Assembly	14	14	0E	0E
4	Number of Column Addresses on Assembly	11	11	0B	0B
5	Number of DIMM Ranks	Module Height = 30.0mm, 2 ranks	Module Height = 30.0mm, 2 ranks	61	61
6	Data Width of Assembly	X72	X72	48	48
7	Reserved	Undefined	Undefined	00	00
8	Voltage Interface Level of this Assembly	SSTL 1.8V	SSTL 1.8V	05	05
9	DDR2 SDRAM Device Cycle Time at CL=X	3ns	2.5ns	30	25
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45ns	0.4ns	45	40
11	DIMM Configuration Type	Address/Command Parity, Data ECC, Non Data Parity,	Address/Command Parity, Data ECC, Non Data Parity,	06	06
12	Refresh Rate/Type	7.8 µs	7.8 µs	82	82
13	Primary DDR2 SDRAM Width	X4	X4	04	04
14	Error Checking DDR2 SDRAM Device Width	X4	X4	04	04
15	Reserved	Undefined	Undefined	00	00
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8	4,8	0C	0C
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8	8	08	08
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5	4,5,6	38	70
19	DIMM Mechanical Characteristics	x ≤ 4.10 (mm)	x ≤ 4.10 (mm)	01	01
20	DDR2 SDRAM DIMM Type Information	RDIMM (133.35mm)	RDIMM (133.35mm)	01	01
21	DDR2 SDRAM Module Attributes:	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 1, Number of Active Registers : 4,	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 1, Number of Active Registers : 4,	07	07
22	DDR2 SDRAM Device Attributes: General	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,	07	07
23	Minimum Clock Cycle at CL=X-1	3.75ns	3ns	3D	30
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns	0.45ns	50	45
25	Minimum Clock Cycle Time at CL=X-2	5ns	3.75ns	50	3D
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns	0.5ns	60	50
27	Minimum Row Precharge Time (t_{RP})	15ns	15ns	3C	3C
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns	7.5ns	1E	1E
29	Minimum RAS to CAS delay (t_{RCD})	15ns	15ns	3C	3C
30	Minimum RAS Pulse Width (t_{RAS})	45ns	45ns	2D	2D
31	Module Bank Density	2GB	2GB	02	02
32	Address and Command Setup Time Before Clock (t_{IS})	0.2ns	0.17ns	20	17
33	Address and Command Hold Time After Clock (t_{IH})	0.27ns	0.25ns	27	25
34	Data Input Setup Time Before Clock (t_{DS})	0.1ns	0.05ns	10	05
35	Data Input Hold Time After Clock (t_{DH})	0.17ns	0.12ns	17	12
36	Write Recovery Time (t_{WR})	15ns	15ns	3C	3C
37	Internal Write to Read Command delay (t_{WTR})	7.5ns	7.5ns	1E	1E
38	Internal Read to Precharge delay (t_{RTP})	7.5ns	7.5ns	1E	1E
39	Reserved	Undefined	Undefined	00	00
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	06	06
41	Minimum Core Cycle Time (t_{RC})	60ns	60ns	3C	3C
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	127.5ns	127.5ns	7F	7F
43	Maximum Clock Cycle Time (t_{CK})	8ns	8ns	80	80
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.24ns	0.2ns	18	14
45	Read Data Hold Skew Factor (t_{QHS})	0.34ns	0.3ns	22	1E
46	PLL Relock Time	15µs	15µs	0F	0F
47	Tcasemax, DT4R4W Delta	Undefined	Undefined	00	00
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	Undefined	Undefined	00	00
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Undefined	Undefined	00	00
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Undefined	Undefined	00	00
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	Undefined	Undefined	00	00
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Undefined	Undefined	00	00
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	Undefined	Undefined	00	00

Serial Presence Detect (Part 1 of 2) **[NT4GT72U4ND0BV, 4GB – 2 Ranks, 256Mx4 DDR2 SDRAMs]**

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-3C	-AD	-3C	-AD
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	Undefined	Undefined	00	00
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	Undefined	Undefined	00	00
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	Undefined	Undefined	00	00
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	Undefined	Undefined	00	00
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	Undefined	Undefined	00	00
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	Undefined	Undefined	00	00
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	Undefined	Undefined	00	00
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	Undefined	Undefined	00	00
62	SPD Revision	1.3	1.3	13	13
63	Checksum for Byte 0-62	Checksum Data	Checksum Data	3D	07
64-71	Manufacturer's JEDEC ID Code	Nanya	Nanya	7F7F7F0B00000000	
72	Module Manufacturing Location	Manufacturing code	Manufacturing code	--	--
73-91	Module Part Number	Module Part Number in ASCII	Module Part Number in ASCII	--	--
92-255	Reserved	Undefined	Undefined	--	--

Note1:
NT4GT72U4ND0BV-3C -> 4E54344754373255344E443042562D33432020
NT4GT72U4ND0BV-AD -> 4E54344754373255344E443042562D41442020

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	-0.5 to 2.3	V
V_{DD}	Voltage on VDD supply relative to V_{SS}	-1.0 to 2.3	V
V_{DDQ}	Voltage on VDDQ supply relative to V_{SS}	-0.5 to 2.3	V
V_{DDL}	Voltage on VDDL supply relative to V_{SS}	-0.5 to 2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Environmental Parameters

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Operating temperature (ambient)	See Note		3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{OPR}	Storage temperature	-50 to 100	℃	1
H_{OPR}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Short Circuit Output Current	105 to 69	K Pascal	1,2

Note:
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	5
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	1, 5
V_{REF}	Input Reference Voltage	0.49V_{DDQ}	0.5 V_{DDQ}	0.51V_{DDQ}	V	2, 3
V_{TT}	Termination Voltage	V_{REF} – 0.04	V_{REF}	V_{DDQ} + 0.04	V	4

Note:
1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must be less than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
4. VTT of transmitting device must track VREF of receiving device.
5. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

Operating, Standby, and Refresh Currents

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V) [1GB, 1Rank, 128Mx8 DDR2 SDRAMs]

Symbol	Parameter/Condition	PC2-5300 (-3C)	PC2-6400 (-AD)	Unit
I_{DD0}	Operating Current: One bank Active – Precharge; $t_{CK} = t_{CK\ (MIN)}$, $t_{RC} = t_{RC\ (MIN)}$, $t_{RAS} = t_{RAS\ (MIN)}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Data bus inputs are switching.	1243	1392	mA
I_{DD1}	Operating Current: One bank; active/read/precharge; BL = 4; $t_{RC} = t_{RC\ (MIN)}$; CL=2.5; $t_{CK} = t_{CK\ (MIN)}$; I_{OUT} = 0mA; $t_{RAS} = t_{RAS\ (MIN)}$. CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	1144	1293	mA
I_{DD2P}	Precharge Power-Down Current: Other control and address inputs are stable, Data bus inputs are floating.	332	332	mA
I_{DD2N}	Precharge Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH. $t_{CK} = t_{CK\ (MIN)}$. Other control and address inputs are switching, data bus inputs are switching.	897	997	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	748	798	mA
I_{DD3PF}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	530	550	mA
I_{DD3PS}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	362	362	mA
I_{DD3N}	Active Standby Current: All banks open; Continuous burst reads; BL=4; AL=0; CL=CLMIN; tRAS = tRAS (MAX); tRP = tRP (MIN); tCK = tCK (MIN); CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching; I_{OUT} = 0mA	847	946	mA
I_{DD4R}	Operating Current: Burst read: All banks open; Continuous burst reads; BL = 4; AL = 0; CL = CL_{MIN}; $t_{CK} = t_{CK\ (MIN)}$; $t_{RAS} = t_{RAS\ (MAX)}$; **$t_{RP} = t_{RP\ (MIN)}$;** CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching.	1441	1590	mA
I_{DD4W}	Operating Current: Burst write: All banks open; Continuous burst writes; BL = 4; AL = 0; CL = CL_{MIN}; $t_{CK} = t_{CK\ (MIN)}$; $t_{RAS} = t_{RAS\ (MAX)}$; **$t_{RP} = t_{RP\ (MAX)}$;** CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching.	1293	1441	mA
I_{DD5}	Auto-Refresh Current: $t_{RC} = t_{RFC\ (MIN)}$, Refresh command every $t_{RFC} = t_{RFC\ (MIN)}$ interval, CKE is HIGH, CS is HIGH between valid commands, other control and address inputs are switching, Data bus inputs are switching.	1837	1986	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are floating, Data bus inputs are floating. RESET is LOW. I_{DD6} current values are guaranteed up to TCASE of 85 ºC max	342	342	mA
I_{DD7}	All Bank Interleave Read Current: All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are stable during deselects. I_{OUT} = 0mA	2085	2283	mA

Note: Module IDD was calculated from component IDD. It may different from the actual measurement.

Operating, Standby, and Refresh Currents

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V) [2GB, 1Rank, 256Mx4 DDR2 SDRAMs]

Symbol	Parameter/Condition	PC2-5300 (-3C)	PC2-6400 (-AD)	Unit
I_{DD0}	Operating Current: One bank Active – Precharge; $t_{CK} = t_{CK\ (MIN)}$, $t_{RC} = t_{RC\ (MIN)}$, $t_{RAS} = t_{RAS\ (MIN)}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Data bus inputs are switching.	2321	2618	mA
I_{DD1}	Operating Current: One bank; active/read/precharge; BL = 4; $t_{RC} = t_{RC\ (MIN)}$; CL=2.5; $t_{CK} = t_{CK\ (MIN)}$; I_{OUT} = 0mA; $t_{RAS} = t_{RAS\ (MIN)}$. CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	2123	2420	mA
I_{DD2P}	Precharge Power-Down Current: Other control and address inputs are stable, Data bus inputs are floating.	499	499	mA
I_{DD2N}	Precharge Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH. $t_{CK} = t_{CK\ (MIN)}$. Other control and address inputs are switching, data bus inputs are switching.	1628	1829	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	1331	1430	mA
I_{DD3PF}	Active Power-Down Current: All banks open; $t_{CK} = t_{CK\ (MIN)}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	895	935	mA
I_{DD3PS}	Active Power-Down Current: All banks open; $t_{CK} = t_{CK\ (MIN)}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	559	559	mA
I_{DD3N}	Active Standby Current: All banks open; Continuous burst reads; BL=4; AL=0; CL=CL$_{MIN}$; $t_{RAS} = t_{RAS\ (MAX)}$; $t_{RP} = t_{RP\ (MIN)}$; $t_{CK} = t_{CK\ (MIN)}$; CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching; I_{OUT} = 0mA	1529	1727	mA
I_{DD4R}	Operating Current: Burst read: All banks open; Continuous burst reads; BL = 4; AL = 0; CL = CL $_{MIN}$; $t_{CK} = t_{CK\ (MIN)}$; $t_{RAS} = t_{RAS\ (MAX)}$; **$t_{RP} = t_{RP\ (MIN)}$;** CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching.	2717	3014	mA
I_{DD4W}	Operating Current: Burst write: All banks open; Continuous burst writes; BL = 4; AL = 0; CL = CL $_{MIN}$; $t_{CK} = t_{CK\ (MIN)}$; $t_{RAS} = t_{RAS\ (MAX)}$; **$t_{RP} = t_{RP\ (MAX)}$;** CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching.	2420	2717	mA
I_{DD5}	Auto-Refresh Current: $t_{RC} = t_{RFC\ (MIN)}$, Refresh command every $t_{RFC} = t_{RFC\ (MIN)}$ interval, CKE is HIGH, CS is HIGH between valid commands, other control and address inputs are switching, Data bus inputs are switching.	3509	3806	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are floating, Data bus inputs are floating. RESET is LOW. I_{DD6} current values are guaranteed up to TCASE of 85 ºC max	519	519	mA
I_{DD7}	All Bank Interleave Read Current: All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are stable during deselects. I_{OUT} = 0mA	4004	4400	mA

Note: Module IDD was calculated from component IDD. It may different from the actual measurement.

Operating, Standby, and Refresh Currents

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V) [2GB, 2Rank, 128Mx8 DDR2 SDRAMs]

Symbol	Parameter/Condition	PC2-5300 (-3C)	PC2-6400 (-AD)	Unit
I_{DD0}	Operating Current: One bank Active – Precharge; $t_{CK} = t_{CK\ (MIN)}$, $t_{RC} = t_{RC\ (MIN)}$, $t_{RAS} = t_{RAS\ (MIN)}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Data bus inputs are switching.	1925	2173	mA
I_{DD1}	Operating Current: One bank; active/read/precharge; BL = 4; $t_{RC} = t_{RC\ (MIN)}$; CL=2.5; $t_{CK} = t_{CK\ (MIN)}$; I_{OUT} = 0mA; $t_{RAS} = t_{RAS\ (MIN)}$. CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	1826	2074	mA
I_{DD2P}	Precharge Power-Down Current: Other control and address inputs are stable, Data bus inputs are floating.	499	499	mA
I_{DD2N}	Precharge Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH. $t_{CK} = t_{CK\ (MIN)}$. Other control and address inputs are switching, data bus inputs are switching.	1628	1829	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	1331	1430	mA
I_{DD3PF}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	895	935	mA
I_{DD3PS}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	559	559	mA
I_{DD3N}	Active Standby Current: All banks open; Continuous burst reads; BL=4; AL=0; CL=CLMIN; tRAS = tRAS (MAX); tRP = tRP (MIN); tCK = tCK (MIN); CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching; I_{OUT} = 0mA	1529	1727	mA
I_{DD4R}	Operating Current: Burst read: All banks open; Continuous burst reads; BL = 4; AL = 0; CL = CL_{MIN}; $t_{CK} = t_{CK\ (MIN)}$; $t_{RAS} = t_{RAS\ (MAX)}$; **$t_{RP} = t_{RP\ (MIN)}$;** CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching.	2123	2371	mA
I_{DD4W}	Operating Current: Burst write: All banks open; Continuous burst writes; BL = 4; AL = 0; CL = CL_{MIN}; $t_{CK} = t_{CK\ (MIN)}$; $t_{RAS} = t_{RAS\ (MAX)}$; **$t_{RP} = t_{RP\ (MAX)}$;** CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching.	1975	2222	mA
I_{DD5}	Auto-Refresh Current: $t_{RC} = t_{RFC\ (MIN)}$, Refresh command every $t_{RFC} = t_{RFC\ (MIN)}$ interval, CKE is HIGH, CS is HIGH between valid commands, other control and address inputs are switching, Data bus inputs are switching.	2519	2767	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are floating, Data bus inputs are floating. RESET is LOW. I_{DD6} current values are guaranteed up to TCASE of 85 ºC max	519	519	mA
I_{DD7}	All Bank Interleave Read Current: All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are stable during deselects. I_{OUT} = 0mA	2767	3064	mA

Note: Module IDD was calculated from component IDD. It may different from the actual measurement.

Operating, Standby, and Refresh Currents

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) [4GB, 2Ranks, 256Mx4 DDR2 SDRAMs]

Symbol	Parameter/Condition	PC2-5300 (-3C)	PC2-6400 (-AD)	Unit
I_{DD0}	Operating Current: One bank Active – Precharge; $t_{CK} = t_{CK\ (MIN)}$, $t_{RC} = t_{RC\ (MIN)}$, $t_{RAS} = t_{RAS\ (MIN)}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Data bus inputs are switching.	3509	4004	mA
I_{DD1}	Operating Current: One bank; active/read/precharge; BL = 4; $t_{RC} = t_{RC\ (MIN)}$; CL=2.5; $t_{CK} = t_{CK\ (MIN)}$; I_{OUT} = 0mA; $t_{RAS} = t_{RAS\ (MIN)}$. CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	3311	3806	mA
I_{DD2P}	Precharge Power-Down Current: Other control and address inputs are stable, Data bus inputs are floating.	658	658	mA
I_{DD2N}	Precharge Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH. $t_{CK} = t_{CK\ (MIN)}$. Other control and address inputs are switching, data bus inputs are switching.	2915	3317	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	2321	2519	mA
I_{DD3PF}	Active Power-Down Current: All banks open; $t_{CK} = t_{CK\ (MIN)}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	1450	1529	mA
I_{DD3PS}	Active Power-Down Current: All banks open; $t_{CK} = t_{CK\ (MIN)}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	777	777	mA
I_{DD3N}	Active Standby Current: All banks open; Continuous burst reads; BL=4; AL=0; CL=CL$_{MIN}$; $t_{RAS} = t_{RAS\ (MAX)}$; $t_{RP} = t_{RP\ (MIN)}$; $t_{CK} = t_{CK\ (MIN)}$; CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching; I_{OUT} = 0mA	2717	3113	mA
I_{DD4R}	Operating Current: Burst read: All banks open; Continuous burst reads; BL = 4; AL = 0; CL = CL $_{MIN}$; $t_{CK} = t_{CK\ (MIN)}$; $t_{RAS} = t_{RAS\ (MAX)}$; **$t_{RP} = t_{RP\ (MIN)}$;** CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching.	3905	4400	mA
I_{DD4W}	Operating Current: Burst write: All banks open; Continuous burst writes; BL = 4; AL = 0; CL = CL $_{MIN}$; $t_{CK} = t_{CK\ (MIN)}$; $t_{RAS} = t_{RAS\ (MAX)}$; **$t_{RP} = t_{RP\ (MAX)}$;** CKE is HIGH, CS is HIGH between valid commands. Address inputs are switching; Data bus inputs are switching.	3608	4103	mA
I_{DD5}	Auto-Refresh Current: $t_{RC} = t_{RFC\ (MIN)}$, Refresh command every $t_{RFC} = t_{RFC\ (MIN)}$ interval, CKE is HIGH, CS is HIGH between valid commands, other control and address inputs are switching, Data bus inputs are switching.	4697	5192	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are floating, Data bus inputs are floating. RESET is LOW. I_{DD6} current values are guaranteed up to TCASE of 85 ºC max	697	697	mA
I_{DD7}	All Bank Interleave Read Current: All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are stable during deselects. I_{OUT} = 0mA	5192	5786	mA

Note: Module IDD was calculated from component IDD. It may different from the actual measurement.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	PC2-5300 -3C		PC2-6400 -AD		Unit
		Min.	Max.	Min.	Max.	
tCK	Average clock period	3000	8000	2500	8000	ps
tCH	Average clock high-level width	0.48	0.52	0.48	0.52	tCK
tCL	Average clock low-level width	0.48	0.52	0.48	0.52	tCK
WL	Write command to DQS associated clock edge	RL-1		RL-1		nCK
tDQSS	DQS latching rising transitions to associated clock edges	-0.25	0.25	-0.25	+0.25	tCK
tDSS	DQS falling edge to CK setup time	0.2	-	0.2	-	tCK
tDSH	DQS falling edge hold time from CK	0.2	-	0.2	-	tCK
tDQSL,(H)	DQS input low (high) pulse width	0.35	-	0.35	-	tCK
tWPRE	Write preamble	0.35	-	0.35	-	tCK
tWPST	Write postamble	0.4	0.6	0.40	0.60	tCK
tIS	Address and control input setup time	200	-	175	-	ps
tIH	Address and control input hold time	275	-	250	-	ps
tIPW	Control & Address Input pulse width for each input	0.6	-	0.6	-	tCK
tDS	DQ and DM input setup time	100	-	50	-	ps
tDH	DQ and DM input hold time	175	-	125	-	ps
tDIPW	DQ and DM input pulse width for each input	0.35	-	0.35	-	tCK
tAC	DQ output access time from CK/$\overline{CK}$	-450	450	-400	400	ps
tDQSCK	DQS output access time from CK/$\overline{CK}$	-400	400	-350	350	ps
tHZ	Data-out high-impedance time from CK/$\overline{CK}$	-	t_{AC} max	-	tACmax	ps
tLZ(DQS)	DQS low-impedance time from CK/$\overline{CK}$	t_{AC} min	t_{AC} max	tACmin	tACmax	ps
tLZ(DQ)	DQ low-impedance time from CK/$\overline{CK}$	$2t_{AC}$ min	t_{AC} max	$2t_{AC}$ min	t_{AC} max	ps
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	240	-	200	ps
tHP	CK half pulse width	Min(tCH(abs), tCL(abs))	-	Min(tCH(abs), tCL(abs))	-	ps
tQHS	Data hold Skew Factor	-	340	-	300	ps
tQH	DQ/DQS output hold time from DQS	t_{HP} - t_{QHS}	-	tHP - tQHS	-	ps
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	0.40	0.60	tCK
tRRD	Active to Active command period	7.5	-	7.5	-	ns
tFAW	Four Activate Window	37.5	-	35	-	ns
tCCD	$\overline{CAS}$ to $\overline{CAS}$ command delay	2		2		nCK
tWR	Write recovery time	15	-	15	-	ns
tDAL	Auto precharge write recovery + precharge time	WR+tRP	-	WR+tRP	-	nCK
tWTR	Internal write to read command delay	7.5	-	7.5	-	ns
tRTP	Internal read to precharge command delay	7.5		7.5		ns
tCKE	CKE minimum pulse width	3		3		nCK
tXSNR	Exit self refresh to a Non-read command	tRFC+10	-	tRFC+10		ns
tXSRD	Exit self refresh to a Read command	200	-	200		nCK
tXP	Exit precharge power down to any command	2	-	2	-	nCK

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

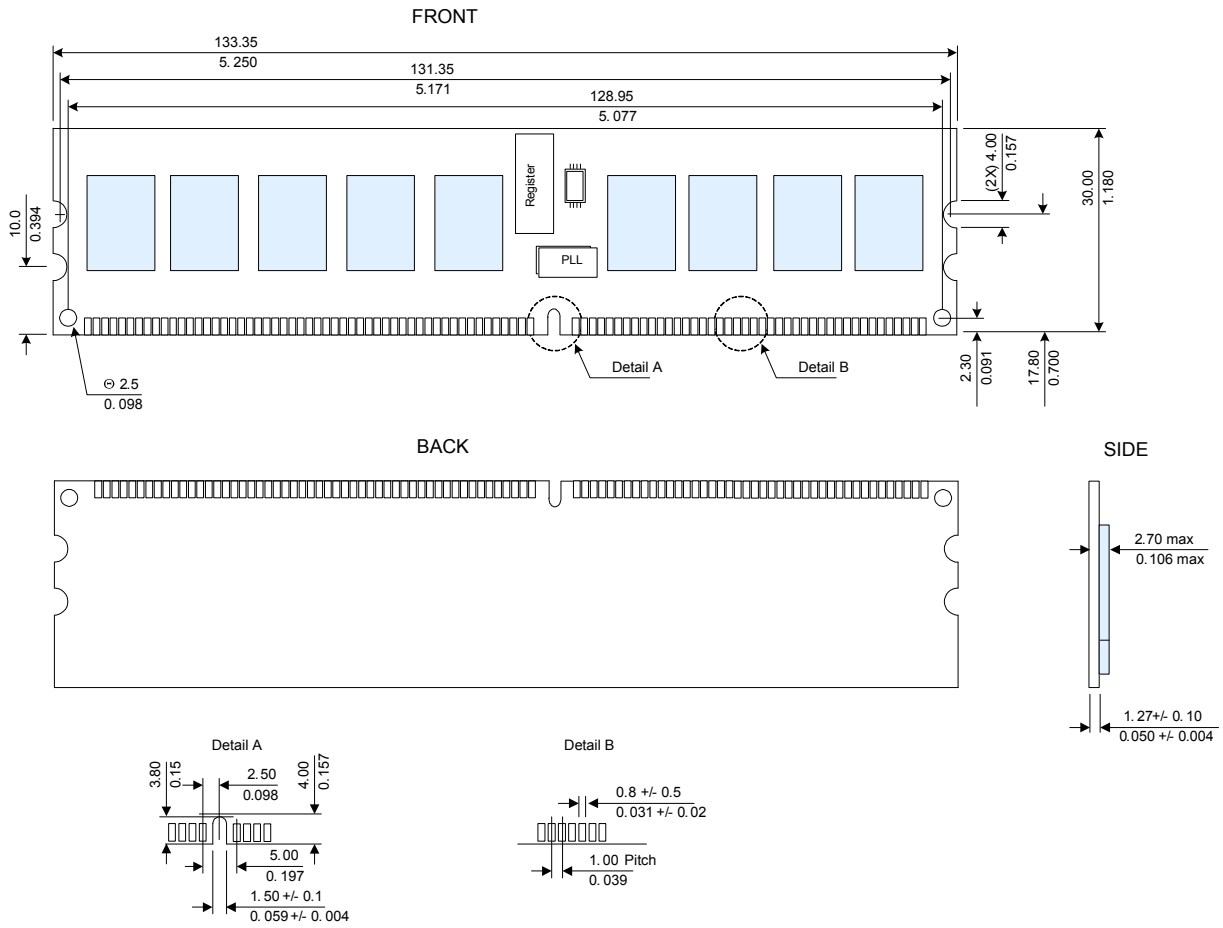
Symbol	Parameter	PC2-5300 -3C		PC2-6400 -AD		Unit
		Min.	Max.	Min.	Max.	
tXARD	Exit active power down to read command	2	-	2	-	nCK
tXARDS	Exit active power down to read command (slow exit, lower power)	7-AL		8-AL		nCK
tAOND	ODT turn-on delay	2	2	2	2	nCK
tAON	ODT turn-on	tAC (min)	tAC (max) +0.7	tAC (min)	tAC (max) +0.7	ns
tAONPD	ODT turn-on (Power down mode)	tAC (min) +2	2tCK + tAC(max) +1	tAC (min) +2	2tCK + tAC(max) +1	ns
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	nCK
tAOF	ODT turn-off	tAC(min)	tAC(max) +0.6	tAC(min)	tAC(max) +0.6	ns
tAOFPD	ODT turn-off (Power down mode)	tAC (min)+2	2.5tCK + tAC(max) +1	tAC (min)+2	2.5tCK + tAC(max) +1	ns
tANPD	ODT to power down entry latency	3	-	3	-	nCK
tAXPD	ODT power down exit latency	8		8		nCK
tMRD	Mode register set command cycle time	2	-	2	-	nCK
tMOD	MRS command to ODT update delay	0	12	0	12	ns
tOIT	OCD drive mode output delay	0	12	0	12	ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	tIS + tCK + tIH	-	tIS + tCK + tIH	-	ns
tREFI	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	3.9		3.9		µs
	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	7.8		7.8		µs

Speed Grade Definition

Symbol	Parameter	PC2-5300 -3C		PC2-6400 -AD		Unit
		Min	Max	Min	Max	
tRAS	Row Active Time	45	70,000	45	70,000	ns
tRC	Row Cycle Time	60	-	60	-	ns
tRCD	RAS to CAS delay	15	-	15	-	ns
tRP	Row Precharge Time	15	-	15	-	ns

Package Dimensions

(1GB, 1Rank, 128MX8 DDR2 SDRAMs)



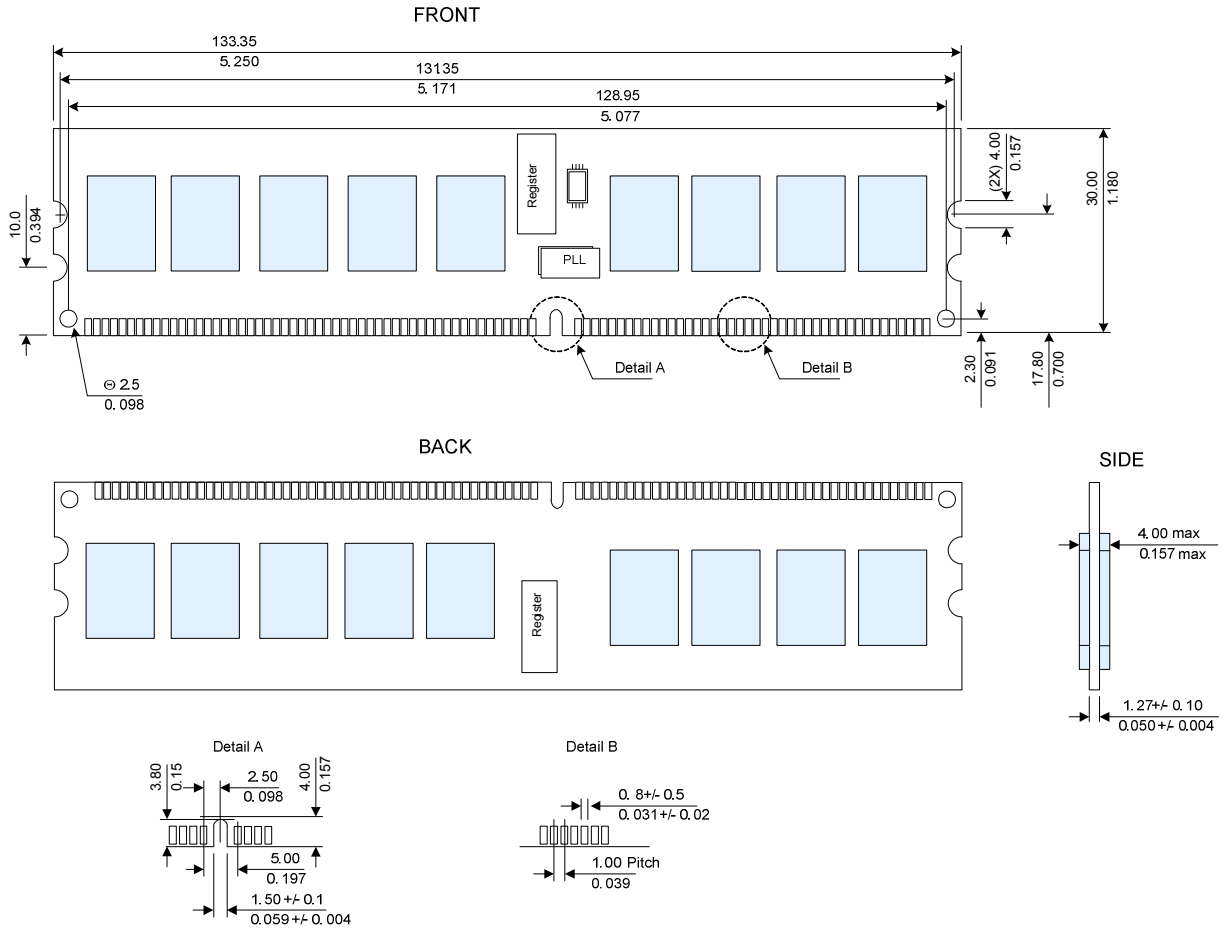
Note: All dimensions are typical with tolerances of +/- 0.15(0.006) unless otherwise stated

Units: Millimeters (Inches)

Package Dimensions

(2GB, 1Rank, 256MX4 DDR2 SDRAMs)

(2GB, 2Rank, 128MX8 DDR2 SDRAMs)

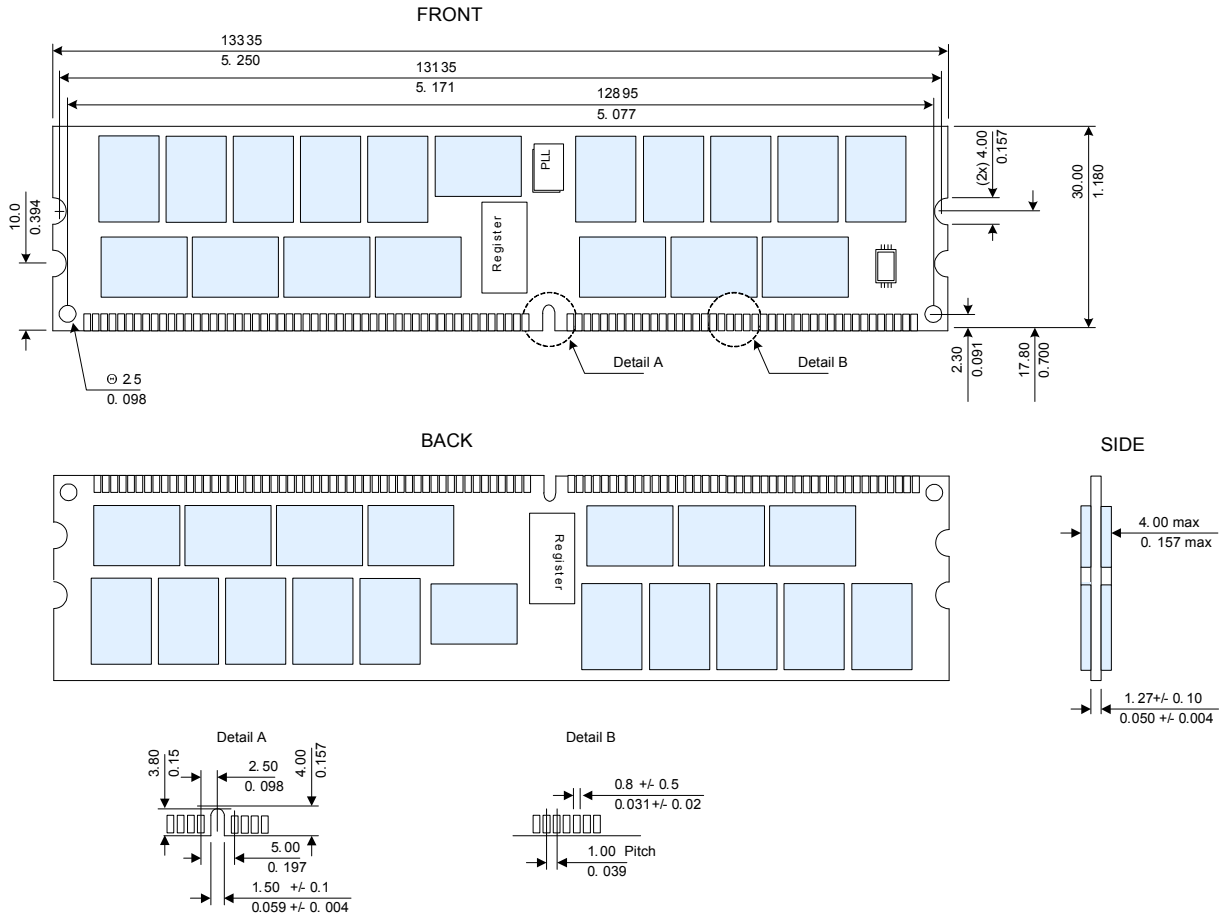


Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated

Units: Millimeters(Inches)

Package Dimensions

(4GB, 2Ranks, 256MX4 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated

Units: Millimeters (Inches)

Revision Log

Rev	Date	Modification
0.1	02/2008	Preliminary Release
1.0	04/2008	Official Release
1.1	01/2009	Add NT2GT72U8PD0BV-3C/AD