Signetics

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Status	Product Specification
FAST Products	

FAST 74F835
Shift Register

8-Bit Shift Register with 2:1 Mux-In, Latched "B" Inputs, and Serial Out

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F835	150MHz	45mA

FEATURES

- **Specifically designed for Video applications**
- **Combines the 'F373, two 'F157s, and the 'F166 functions in one package**
- **Interleaved loading with 2:1 mux**
- **Dual 8-bit Parallel Inputs**
- **Transparent Latch on all "B" inputs**
- **Guaranteed Serial Shift Frequency to 100MHz**
- **Expandable to 16-bits or more with serial input**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F835N
24-Pin Plastic SOL	N74F835D

DESCRIPTION

The 74F835 is a high speed 8-bit parallel/serial-in, serial-out shift register whose parallel inputs have been connected to an internal octal two-to-one multiplexer with all the 'B' inputs connected to an octal latch.

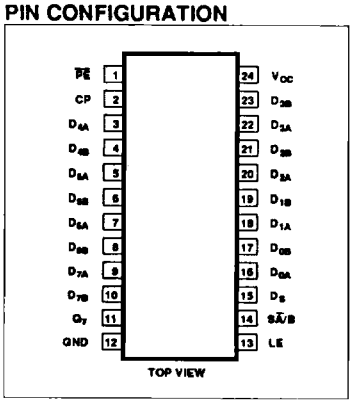
This 24 pin part is specifically designed for video bit shifting, where interleaved loading is desired and parts count is critical. However, and It is useful in any design where a 2:1 mux input with a transparent latch is needed.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

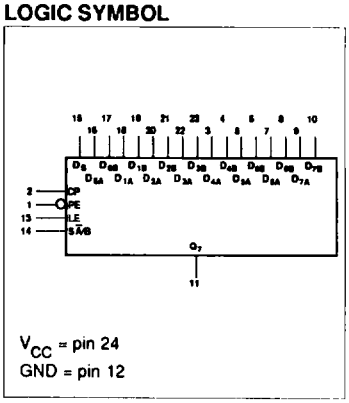
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{0A} - D_{7A}	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{0B} - D_{7B}	Latched Parallel data inputs	1.0/1.0	20µA/0.6mA
D_S	Serial data input	1.0/1.0	20µA/0.6mA
CP	Shift Register Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$S\overline{A}/B$	Mux Select	1.0/1.0	20µA/0.6mA
LE	Latch Enable input (for B inputs)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20µA/0.6mA
Q_7	Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

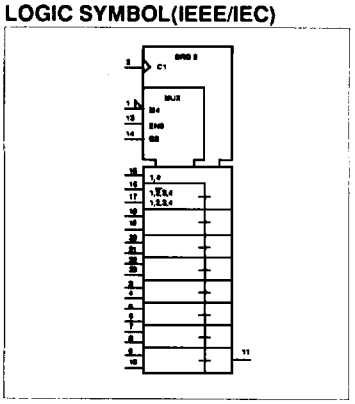
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximun input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} =MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} =MAX			45	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

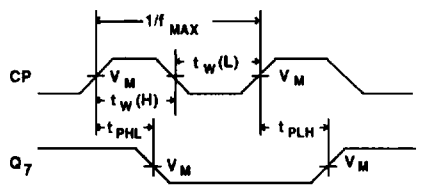
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	130	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Load)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Shift)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns

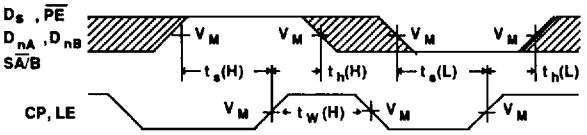
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_{nA} or D_{nB} to CP	Waveform 2	3.5 3.5			3.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nA} or D_{nB} to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time D_S to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_S to CP	Waveform 2	2.0 2.0			2.5 2.5		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{PE}$ to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{PE}$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_{nB} to LE	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nB} to LE	Waveform 2	3.0 3.0			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time $S\overline{A}/B$ to CP	Waveform 2	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time $S\overline{A}/B$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	4.5 4.5			5.5 5.0		ns
$t_w(H)$	Latch Enable pulse width, High	Waveform 1	4.5			5.0		ns

AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data and Select Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.