RAMBUS®
RIMM™ MODULE

MT4VR3216A, MT4VR3218A, MT8VR6416A,
MT8VR6418A, MT16VR12816A,
MT16VR12818A

For the latest data sheet revisions, please refer to the Micron Web site: www.micronsemi.com/datasheets/modds.html

FEATURES

- 184-pin RIMM module with 1mm pad spacing
- 64MB (32 Meg x 16/18), 128MB (64 Meg x 16/18), 256MB (128 Meg x 16/18)
- Uses (4, 8, or 16) 8 Meg x 16/18 RDRAM® devices
- High-speed 300 MHz, 356 MHz, and 400 MHz clocks with 2x data rates
- 1.6 GB/s peak I/O bandwidth at 400 MHz clock rate
- Packet-oriented Rambus protocol transmitted in 8-bit long packets
- Separate control and data buses for increased data bandwidth capability
- Control bus with separate row and column buses for easier command scheduling
- Programmable output delay timing for round-trip delay of one to five cycles
- Write buffer to reduce READ latency
- Three precharge mechanisms for controller flexibility
- Programmable power states for flexibility in power consumption versus data access time
- Power-down Self Refresh and active refresh
- 32ms, 16,384 cycle refresh
- 2.5V power supply
- Serial Presence Detect (SPD)

OPTIONS — MARKING

- Package
  184-pin RIMM module (gold) — G

- Timing (Cycle Time)
  300 MHz Clock Rate, Access Time = 53ns — -653
  356 MHz Clock Rate, Access Time = 50ns — -750
  356 MHz Clock Rate, Access Time = 45ns — -745
  400 MHz Clock Rate, Access Time = 45ns — -845
  400 MHz Clock Rate, Access Time = 40ns — -840

PIN ASSIGNMENT
184-PIN RIMM MODULE

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
A1	GND	B1	GND	A47	NC	B47	NC
A2	LDQA8*	B2	LDQA7	A48	NC	B48	NC
A3	GND	B3	GND	A49	NC	B49	NC
A4	LDQA6	B4	LDQA5	A50	NC	B50	NC
A5	GND	B5	GND	A51	V_{REF}	B51	V_{REF}
A6	LDQA4	B6	LDQA3	A52	GND	B52	GND
A7	GND	B7	GND	A53	SCL	B53	SA0
A8	LDQA2	B8	LDQA1	A54	V_{DD}	B54	V_{DD}
A9	GND	B9	GND	A55	SDA	B55	SA1
A10	LDQA0	B10	LCFM	A56	SV_{DD}	B56	SV_{DD}
A11	GND	B11	GND	A57	SWP	B57	SA2
A12	LCTMN	B12	LCFMN	A58	V_{DD}	B58	V_{DD}
A13	GND	B13	GND	A59	RSCK	B59	RCMD
A14	LCTM	B14	NC	A60	GND	B60	GND
A15	GND	B15	GND	A61	RDQB7	B61	RDQB8*
A16	NC	B16	LROW2	A62	GND	B62	GND
A17	GND	B17	GND	A63	RDQB5	B63	RDQB6
A18	LROW1	B18	LROW0	A64	GND	B64	GND
A19	GND	B19	GND	A65	RDQB3	B65	RDQB4
A20	LCOL4	B20	LCOL3	A66	GND	B66	GND
A21	GND	B21	GND	A67	RDQB1	B67	RDQB2
A22	LCOL2	B22	LCOL1	A68	GND	B68	GND
A23	GND	B23	GND	A69	RCOL0	B69	RDQB0
A24	LCOL0	B24	LDQB0	A70	GND	B70	GND
A25	GND	B25	GND	A71	RCOL2	B71	RCOL1
A26	LDQB1	B26	LDQB2	A72	GND	B72	GND
A27	GND	B27	GND	A73	RCOL4	B73	RCOL3
A28	LDQB3	B28	LDQB4	A74	GND	B74	GND
A29	GND	B29	GND	A75	RROW1	B75	RROW0
A30	LDQB5	B30	LDQB6	A76	GND	B76	GND
A31	GND	B31	GND	A77	NC	B77	RROW2
A32	LDQB7	B32	LDQB8*	A78	GND	B78	GND
A33	GND	B33	GND	A79	RCTM	B79	NC
A34	LSCK	B34	LCMD	A80	GND	B80	GND
A35	V_{CMOS}	B35	V_{CMOS}	A81	RCTMN	B81	RCFMN
A36	SOUT	B36	SIN	A82	GND	B82	GND
A37	V_{CMOS}	B37	V_{CMOS}	A83	RDQA0	B83	RCFM
A38	NC	B38	NC	A84	GND	B84	GND
A39	GND	B39	GND	A85	RDQA2	B85	RDQA1
A40	NC	B40	NC	A86	GND	B86	GND
A41	V_{DD}	B41	V_{DD}	A87	RDQA4	B87	RDQA3
A42	V_{DD}	B42	V_{DD}	A88	GND	B88	GND
A43	NC	B43	NC	A89	RDQA6	B89	RDQA5
A44	NC	B44	NC	A90	GND	B90	GND
A45	NC	B45	NC	A91	RDQA8*	B91	RDQA7
A46	NC	B46	NC	A92	GND	B92	GND

*Nonfunctional on x16 devices.

GENERAL DESCRIPTION

The MT4VR3216/18A, MT8VVR6416/18A and MT16VVR12816/18A RDRAM RIMM modules are general-purpose, high-performance, packet-oriented, dynamic random-access memories configured as 64MB/72MB, 128/144MB, and 256MB/288MB densities. The RIMM modules consist of 4, 8, or 16 Direct RDRAM devices organized as 8 words by 16 or 18 bits.

The RIMM modules use Rambus signaling level (RSL) technology to achieve 300 MHz, 356 MHz, or 400 MHz clock speeds using differential clocks. Control and I/O data is transferred on both the rising and falling edges of the clock. This allows data transfers at 1.25ns per two bytes (10ns per 16 bytes) during peak operation.

All DRAM commands are communicated to the RIMM modules through a 3-bit row or 5-bit column bus in packets which are 8 bits in length. These packets are then decoded on the RDRAM into the operation and address requiring access.

Initialization and mode configurations for the RIMM modules are accessed through slow speed CMOS Serial I/O interface.

The architecture of Direct RDRAMs allows high sustained bandwidth memory transactions for multiple, simultaneous, semi-random addresses. Each Direct RDRAM's thirty-two banks can support up to four simultaneous transactions (within bank restrictions).

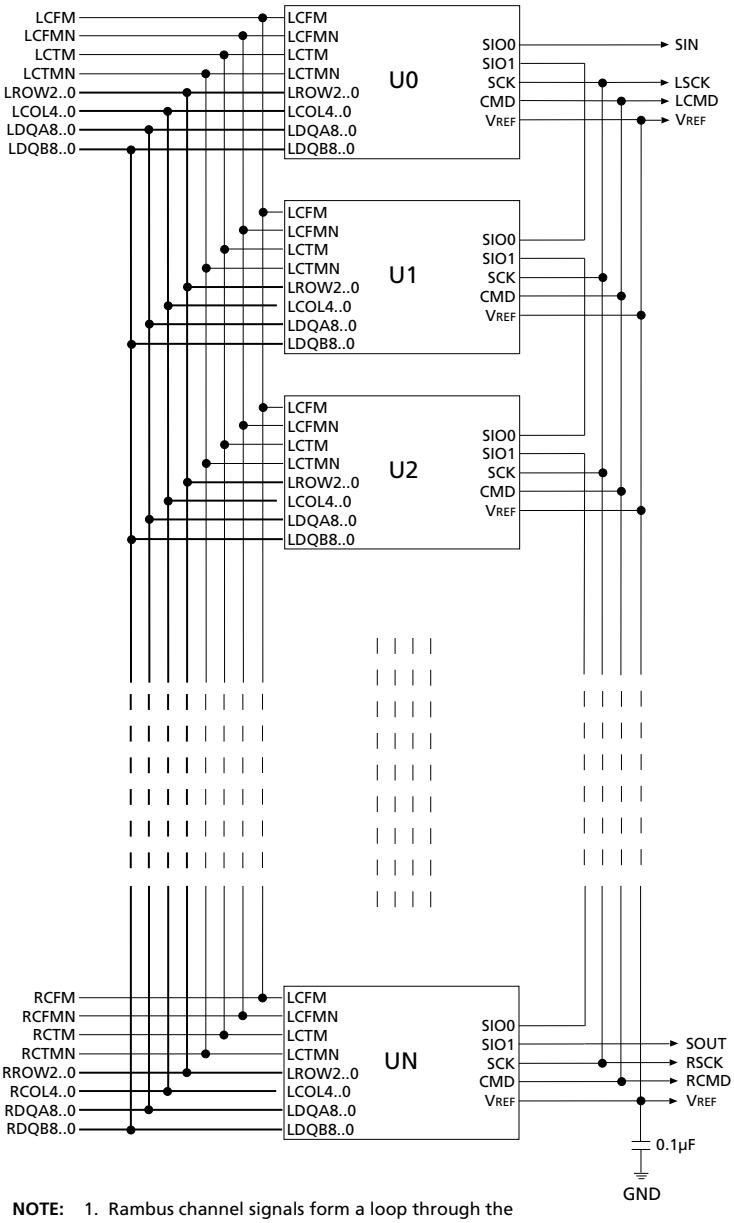
System-oriented features include power management, byte masking and x16/18 organization. The two data bits in the x18 organization are general and can be used for additional storage, bandwidth, or for error correction.

PART NUMBERS

PART NUMBER	CONFIGURATION	CLK FREQ. (MHz)	ACCESS TIME (ns)
MT4VR3216AG-653__	32 Meg x 16	300	53
MT4VR3216AG-750__	32 Meg x 16	356	50
MT4VR3216AG-745__	32 Meg x 16	356	45
MT4VR3216AG-845__	32 Meg x 16	400	45
MT4VR3216AG-840__	32 Meg x 16	400	40
MT4VR3218AG-653__	32 Meg x 18	300	53
MT4VR3218AG-750__	32 Meg x 18	356	50
MT4VR3218AG-745__	32 Meg x 18	356	45
MT4VR3218AG-845__	32 Meg x 18	400	45
MT4VR3218AG-840__	32 Meg x 18	400	40
MT8VR6416AG-653__	64 Meg x 16	300	53
MT8VR6416AG-750__	64 Meg x 16	356	50
MT8VR6416AG-745__	64 Meg x 16	356	45
MT8VR6416AG-845__	64 Meg x 16	400	45
MT8VR6416AG-840__	64 Meg x 16	400	40
MT8VR6418AG-653__	64 Meg x 18	300	53
MT8VR6418AG-750__	64 Meg x 18	356	50
MT8VR6418AG-745__	64 Meg x 18	356	45
MT8VR6418AG-845__	64 Meg x 18	400	45
MT8VR6418AG-840__	64 Meg x 18	400	40
MT16VR12816AG-653__	128 Meg x 16	300	53
MT16VR12816AG-750__	128 Meg x 16	356	50
MT16VR12816AG-745__	128 Meg x 16	356	45
MT16VR12816AG-845__	128 Meg x 16	400	45
MT16VR12816AG-840__	128 Meg x 16	400	40
MT16VR12818AG-653__	128 Meg x 18	300	53
MT16VR12818AG-750__	128 Meg x 18	356	50
MT16VR12818AG-745__	128 Meg x 18	356	45
MT16VR12818AG-845__	128 Meg x 18	400	45
MT16VR12818AG-840__	128 Meg x 18	400	40

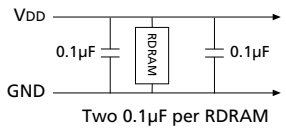
NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8VR6416AG-750B1

FUNCTIONAL BLOCK DIAGRAM

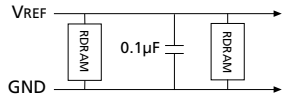


NOTE: 1. Rambus channel signals form a loop through the RIMM module, with the exception of the SIO chain.

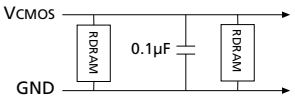
DECOUPLING



Two 0.1µF per RDRAM

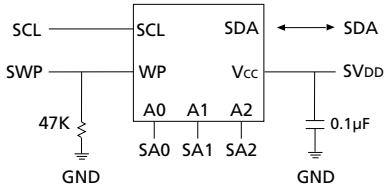


One 0.1µF per two RDRAMs



One 0.1µF per two RDRAM

Serial Presence Detect (SPD)



MODULE CAPACITY	N
256MB	16
128MB	8
64MB	4

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	I/O	TYPE	DESCRIPTION
B10	LCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
B12	LCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
A20, B20, A22, B22, A24	LCOL4–LCOL0	I	RSL	Column Bus. 5-bit bus containing control and address information for column accesses.
A14	LCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
A12	LCTMN	I	RSL	Clock to Master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
B16, A18, B18	LROW2–LROW0	I	RSL	Row Bus. 3-bit bus containing control and address information for row accesses.
B83	RCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
B81	RCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
A73, B73, A71, B71, A69	RCOL4–RCOL0	I	RSL	Column Bus. 5-bit bus containing control and address information for Column accesses.
A79	RCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
A81	RCTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals from the Channel. Negative polarity.
B77, A75, B75	RROW2–RROW0	I	RSL	Row Bus. 3-bit bus containing control and address information for row accesses.
B53	SA0	I	SV_{DD}	Serial Presence Detect Address 0
B55	SA1	I	SV_{DD}	Serial Presence Detect Address 1
B57	SA2	I	SV_{DD}	Serial Presence Detect Address 2
A53	SCL	I	SV_{DD}	Serial Presence Detect Clock.
A57	SWP	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
B34	LCMD	I	V_{CMOS}	Serial Command used to read from and write to the control registers. Also used for power management.
A34	LSCK	I	V_{CMOS}	Serial Clock Input. Clock source used to read from and write to the RDRAM control registers.
B59	RCMD	I	V_{CMOS}	Serial Command Input used to read from and write to the control registers. Also used for power management.
A59	RSCK	I	V_{CMOS}	Serial Clock Input. Clock source used to read from and write to the RDRAM control registers.

(Continued on the next page)

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	I/O	TYPE	DESCRIPTION
A2, B2, A4, B4, A6, B6, A8, B8, A10	LDQA8–LDQA0	I/O	RSL	Data Bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on x16 modules.
B32, A32, B30, A30, B28, A28, B26, A26, B24	LDQB8–LDQB0	I/O	RSL	Data Bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on x16 modules.
A91, B91, A89, B89, A87, B87, A85, B85, A83	RDQA8–RDQA0	I/O	RSL	Data Bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on x16 modules.
B61, A61, B63, A63, B65, A65, B67, A67, B69	RDQB8–RDQB0	I/O	RSL	Data Bus B. A 9-bit bus carrying a byte of read or writedata between the Channel and the RDRAM. RDQB8 is non-functional on x16 modules.
A55	SDA	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O).
B36	SIN	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
A36	S_{OUT}	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
A35, B35, A37, B37	V_{CMOS}			CMOS I/O Voltage. Used for signals CMD, SCK, S_{IN}, and S_{OUT}.
A41, A42, A54, A58, B41, B42, B54, B58	V_{DD}			Supply voltage for the RDRAM core and interface logic.
A56, B56	SV_{DD}			SPD voltage. Used for signals SCL, SDA, SWE, SA0, SA1, and SA2.
A51, B51	V_{REF}			Logic threshold reference voltage for RSL signals.
A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, A82, A84, A86, A88, A90, A92, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B39, B52, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80, B82, B84, B86, B88, B90, B92	GND			Ground reference for RDRAM core and interface.
A16, A38, A40, A43, A44, A45, A46, A47, A48, A49, A50, A77, B43, B44, B45, B46, B47, B48, B49, B50, A77, B14, B38, B40, B79	NC			No Connection. These 24 pins are all reserved for future use.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 128 bytes programmed by Micron with infomoration such as RDRAM organization and timing parameters. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (RIMM) occur via a standard I^2C bus using the RIMM's SCL (clock) and SDA (data) signals.

CLOCK AND DATA CONVENTIONS

The EEPROM devices used on these modules conform to the I^2C 2-wire protocol. This protocol defines any device that puts data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the transfer is referred to as the master and the device that receives the data is referred to as the slave device. The master always initiates a data transfer and provides the serial clock for synchronization. The EEPROM device on these modules is always the slave. Data states on the SDA line can change only during SCL LOW indicated in Figure 1. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

START COMMAND

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. Figure 2 shows an example of the START command timing definition.

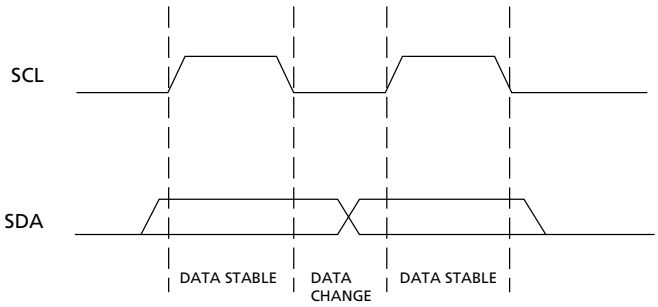


Figure 1
Data Validity

STOP COMMAND

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. A STOP at the end of a READ cycle places the EEPROM into STANDBY power mode. Figure 2 shows an example of the STOP command timing definition.

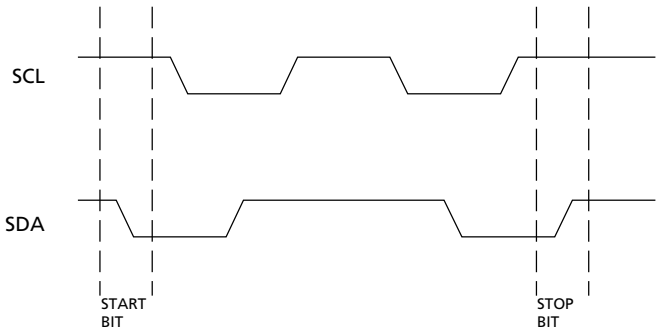


Figure 2
Definition of Start and Stop

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

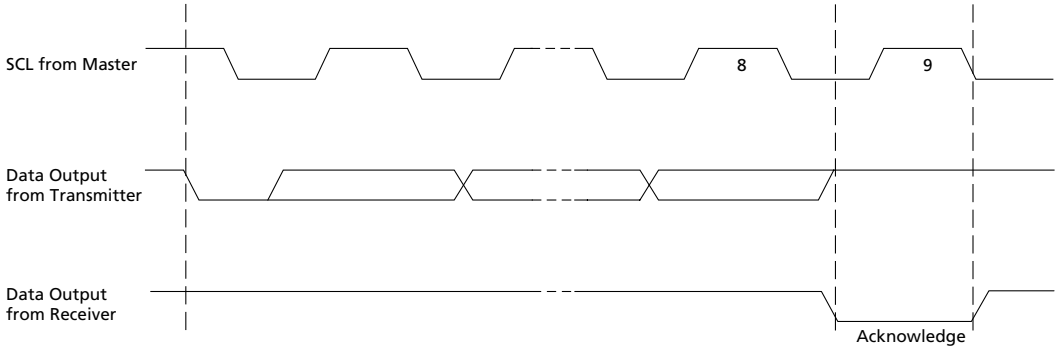


Figure 3
SPD Acknowledge Response From Receiver

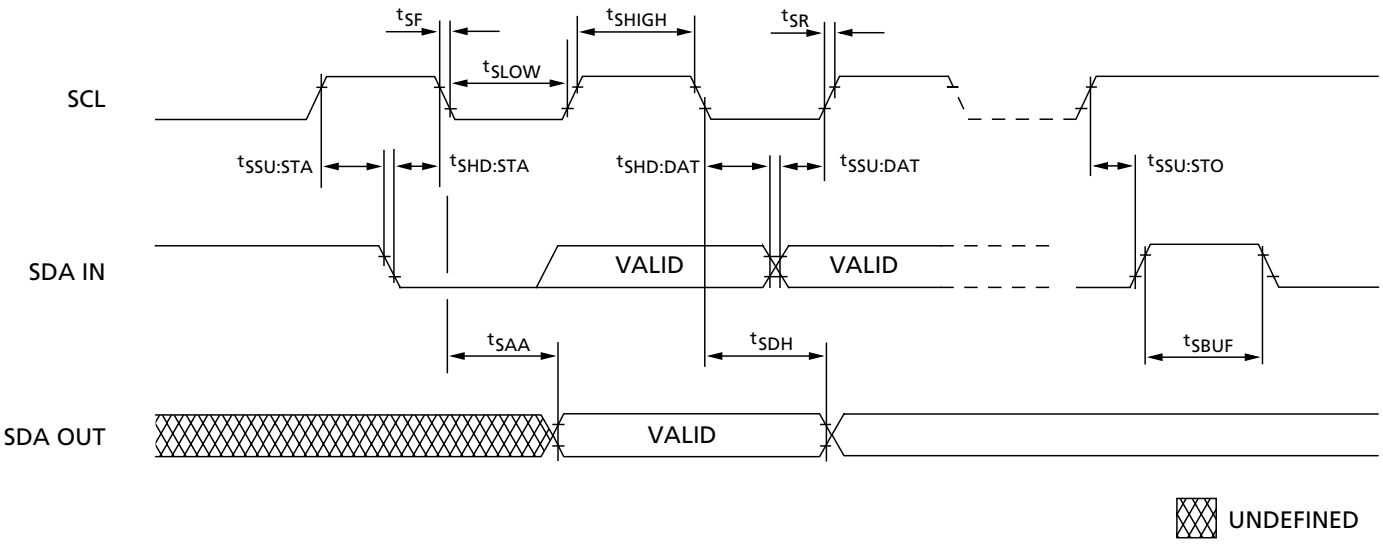


Figure 4
SPD EEPROM Timing

SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
^{t}SAA	0.3	7.0	µs
^{t}SBUF	6.7		µs
^{t}SDH	300		ns
^{t}SF		300	ns
^{t}SHD:DAT	0		µs
^{t}SHD:STA	4.5		µs

SYMBOL	MIN	MAX	UNITS
^{t}SHIGH	4.5		µs
^{t}SLOW	6.7		µs
^{t}SR		1	µs
^{t}SSU:DAT	500		ns
^{t}SSU:STA	6.7		µs
^{t}SSU:STO	6.7		µs

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	OPTION	ENTRY	x16 VALUE (HEX)	x18 VALUE (HEX)
0	SPD Revision Level	2	02	02	
1	Total number of bytes in the SPD		256	08	08
2	Device Type		DRDRAM	01	01
3	Module Type		RIMM	01	01
4	Row Address Bits, Column Address Bits		9,6	96	96
5	Bank Address Bits and Type		16d (5 bank bits)	C5	C5
6	Refresh Bank Bits		5	05	05
7	tREF (Refresh Interval)		32	20	20
8	Protocol version		2	02	02
9	Miscellaneous device configuration field	tDQS = 1.5 no -LP S28IECO S3 supported	1 tSCK	05	05
10	tRP-R (MIN)	-653 -745 -750 -845 -840	8 cycles 8 cycles 8 cycles 8 cycles 8 cycles	08 08 08 08 08	08 08 08 08 08
11	tRAS-R (MIN)	-653 -745 -750 -845 -840	20 cycles 20 cycles 20 cycles 20 cycles 20 cycles	14 14 14 14 14	14 14 14 14 14
12	tRCD-R (MIN)	-653 -745 -750 -845 -840	8 cycles 8 cycles 10 cycles 10 cycles 8 cycles	08 08 0A 0A 08	08 08 0A 0A 08
13	tRR-R (MIN)	-653 -745 -750 -845 -840	8 cycles 8 cycles 8 cycles 8 cycles 8 cycles	08 08 08 08 08	08 08 08 08 08
14	tPP-R (MIN)	-653 -745 -750 -845 -840	8 cycles 8 cycles 8 cycles 8 cycles 8 cycles	08 08 08 08 08	08 08 08 08 08
15	Min tCYCLE for range A	-653 -745 -750 -845 -840	3.33ns 2.80ns 2.80ns 2.50ns 2.50ns	1A 15 15 13 13	1A 15 15 13 13

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	OPTION	ENTRY	x16 VALUE (HEX)	x18 VALUE (HEX)
16	Max ^{t}CYCLE for range A	-653	3.83ns	1E	1E
		-745	3.33ns	1B	1B
		-750	3.33ns	1B	1B
		-840	3.33ns	1B	1B
		-845	3.33ns	1B	1B
17	^{t}CDLY range for range A	-653	5–9	59	59
		-745	5–9	59	59
		-750	5–9	59	59
		-840	5–9	59	59
		-845	5–9	59	59
18	^{t}CLS and ^{t}CAS range for range A	-653	^{t}CLS = 2	AA	AA
		-745	^{t}CAS = 2	AA	AA
		-750		AA	AA
		-845		AA	AA
		-840		AA	AA
19	Min ^{t}CYCLE for range B	-653	–	00	00
		-745	3.33ns	1A	1A
		-750	3.33ns	1A	1A
		-840	3.33ns	1A	1A
		-845	3.33ns	1A	1A
20	Max ^{t}CYCLE for range B	-653	–	00	00
		-745	3.83ns	1E	1E
		-750	3.83ns	1E	1E
		-840	3.83ns	1E	1E
		-845	3.83ns	1E	1E
21	^{t}CDLY range for range B	-653	–	00	00
		-745	4–9	49	49
		-750	4–9	49	49
		-840	4–9	49	49
		-845	4–9	49	49
22	^{t}CLS and ^{t}CAS range for range B	-653	^{t}CLS = 2	00	00
		-745	^{t}CAS = 2	AA	AA
		-750		AA	AA
		-840		AA	AA
		-845		AA	AA
23	Min ^{t}CYCLE for range C	-653	–	00	00
		-745	–	00	00
		-750	–	00	00
		-840	–	00	00
		-845	–	00	00
24	Max ^{t}CYCLE for range C	-653	–	00	00
		-745	–	00	00
		-750	–	00	00
		-840	–	00	00
		-845	–	00	00

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	OPTION	ENTRY	x16 VALUE (HEX)	x18 VALUE (HEX)
25	^{t}CDLY range for range C	-653	–	00	00
		-745	–	00	00
		-750	–	00	00
		-840	–	00	00
		-845	–	00	00
26	^{t}CLS and tCAS range for range C	-653	–	00	00
		-745	–	00	00
		-750	–	00	00
		-840	–	00	00
		-845	–	00	00
27	Min ^{t}CYCLE for range D	-653	–	00	00
		-745	–	00	00
		-750	–	00	00
		-840	–	00	00
		-845	–	00	00
28	Max ^{t}CYCLE for range D	-653	–	00	00
		-745	–	00	00
		-750	–	00	00
		-840	–	00	00
		-845	–	00	00
29	^{t}CDLY range for range D	-653	–	00	00
		-745	–	00	00
		-750	–	00	00
		-840	–	00	00
		-845	–	00	00
30	^{t}CLS and ^{t}CAS range for range D	-653	–	00	00
		-745	–	00	00
		-750	–	00	00
		-840	–	00	00
		-845	–	00	00
31	^{t}PDNXA (MAX)	-653	4µs	04	04
		-745	4µs	04	04
		-750	4µs	04	04
		-840	4µs	04	04
		-845	4µs	04	04
32	^{t}PDNXB (MAX)	-653	9000 cycles	8D	8D
		-745	9000 cycles	8D	8D
		-750	9000 cycles	8D	8D
		-840	9000 cycles	8D	8D
		-845	9000 cycles	8D	8D
33	^{t}NAPXA (MAX)	-653	50ns	32	32
		-745	50ns	32	32
		-750	50ns	32	32
		-840	50ns	32	32
		-845	50ns	32	32

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	OPTION	ENTRY	x16 VALUE (HEX)	x18 VALUE (HEX)
34	^{t}NAPXB (MAX)	-653	40ns	28	28
		-745	40ns	28	28
		-750	40ns	28	28
		-840	40ns	28	28
		-845	40ns	28	28
35	^{f}I(MIN) [11:8]	-653	1,1	11	11
		-745	1,1	11	11
		-750	1,1	11	11
		-840	1,1	11	11
		-845	1,1	11	11
36	^{f}I(MIN) [7:0]	-653	05	05	05
		-745	05	05	05
		-750	05	05	05
		-840	05	05	05
		-845	05	05	05
37	^{f}I(MAX) [7:0]	-653	2C	2C	2C
		-745	65	65	65
		-750	65	65	65
		-840	90	90	90
		-845	90	90	90
38	ODF Mapping		0%	00	00
39	^{t}CCTRL (MAX)		100ms	64	64
40	^{t}TEMP (MAX)		100ms	64	64
41	^{t}TCE (MIN)		150 ^{t}CYCLE	96	96
42	^{t}RAS-R (MAX)		64µs	40	40
43	^{t}NLIMIT (MAX)		10µs	0A	0A
44	ACTREFPT, PCHREFPT		6,6 ^{t}CYCLE	66	66
45	CPCHREFPT_DC, RDREFPT_DC		5,5 ^{t}CYCLE	55	55
46	RETREFPT_DC, WRREFPT_DC		5,13 ^{t}CYCLE	5D	5D
47	Reserved			00	00
48	Reserved			00	00
49	Reserved			00	00
50	^{f}RAS [11:8]	-653	01	01	01
		-745	01	01	01
		-750	01	01	01
		-840	01	01	01
		-845	01	01	01
51	^{f}RAS [7:0]	-653	2C	2C	2C
		-745	65	65	65
		-750	65	65	65
		-840	90	90	90
		-845	90	90	90

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	OPTION	ENTRY	x16 VALUE (HEX)	x18 VALUE (HEX)
52	PMAX,HI [7], PMAX,LO [6], Tj [5:0]	-653	0,0,(100-64)	24	24
		-745	0,0,(100-64)	24	24
		-750	0,0,(100-64)	24	24
		-840	0,0,(100-64)	24	24
		-845	0,0,(100-64)	24	24
53	HeatSpreader [7], Thermal Sensor [6], Tplate [5:0]	-653	1,0,0	80	80
		-745	1,0,0	80	80
		-750	1,0,0	80	80
		-840	1,0,0	80	80
		-845	1,0,0	80	80
54	PSTBY,HI	-653	90	5A	5A
		-745	95	5F	5F
		-750	95	5F	5F
		-840	105	69	69
		-845	105	69	69
55	PACTI,HI	-653	125/2	3F	3F
		-745	140/2	46	46
		-750	140/2	46	46
		-840	150/2	4B	4B
		-845	150/2	4B	4B
56	PACTRW,HI	-653	510/8	40	40
		-745	580/8	49	49
		-750	580/8	49	49
		-840	635/8	50	50
		-845	635/8	50	50
57	PSTBY,LO	-653	85	55	55
		-745	85	55	55
		-750	85	55	55
		-840	85	55	55
		-845	85	55	55
58	PACTI,LO	-653	115/2	3A	3A
		-745	115/2	3A	3A
		-750	115/2	3A	3A
		-840	115/2	3A	3A
		-845	115/2	3A	3A
59	PACTRW,LO	-653	470/8	3B	3B
		-745	470/8	3B	3B
		-750	470/8	3B	3B
		-840	470/8	3B	3B
		-845	470/8	3B	3B
60	PNAP	-653	4.2mA/128µA	21	21
		-745	4.2mA/128µA	21	21
		-750	4.2mA/128µA	21	21
		-840	4.2mA/128µA	21	21
		-845	4.2mA/128µA	21	21

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	OPTION	ENTRY	x16 VALUE (HEX)	x18 VALUE (HEX)
61	PRESA			00	00
62	PRESB			00	00
63	Checksum for Bytes 0–62				
64–71	Manufacturer ID code		44	2C	2C
72	Module manufacturing location				
73–90	Module part number				
91–92	Module revision code				
93	Module manufacturing year				
94	Module manufacturing week				
95-98	Module serial number				
99	Number of devices on module	MT4VR3216/18A MT8VR6416/18A MT16VR12816/18A	4 8 16	04 08 10	04 08 10
100	Module data widthx16	16 x18	10 18		 12
101	Device enables		255	FF	FF
102	Device enables		0	00	00
103	Device enables		0	00	00
104	Device enables		0	00	00
105	Module Vdd [7:4] Module Voltage Interface Level [3:0]		2.5V 1.8V	10	10
106	Module Vdd DC Tolerance [7:4] Module Vdd AC Tolerance [3:0]		5%	52	52
107–113	Reserved		0 0	00 00	00 00
114	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=3			00	00
115	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=4		2/0	20	20
116	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=5		3/0	30	30
117	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=6		3/1	31	31
118	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=7		3/2	32	32
119	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=8		4/2	42	42
120	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=9		5/2	52	52
121	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=10			00	00
122	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=11			00	00
123	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=12			00	00
124	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=13			00	00
125	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=14			00	00
126	^{t}CDLY0 [7:4], ^{t}CDLY1 [3:0], tCDLY=15			00	00
127	Checksum for bytes 99–126				

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note : 1) (SV_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	SV_{DD}	2.2	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{SIH}	SV_{DD} x 0.7	SV_{DD} + 0.3	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{SIL}	- 0.3	SV_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{SOL} = 3.0 mA	V_{SOL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to SV_{DD}	I_{SLI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to SV_{DD}	I_{SLO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SVDD1}	–	100	µA
POWER SUPPLY CURRENT: ^{f}SCL = 100 KHz	I_{SVDD}	–	5.0	mA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 1) (SV_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL clock frequency	^{f}SCL		100	KHz	
Noise suppression time constant at SCL, SDA	^{t}1		100	ns	
SCL LOW to SDA data-out valid	^{t}SAA	0.3	7	µs	
Time the bus must be free before a new transition can start	^{t}SBUF	6.7		µs	
Start condition hold time	^{t}SHD:STA	4.5		µs	
Clock LOW period	^{t}SLOW	6.7		µs	
Clock HIGH period	^{t}SHIGH	4.5		µs	
Start condition setup time	^{t}SSU:STA	6.7		µs	
Data-in hold time	^{t}SHD:DAT	0		µs	
Data-in setup time	^{t}SSU:DAT	500		ns	
SDA and SCL rise time	^{t}SR		1	µs	
SDA and SCL fall time	^{t}SF		300	ns	
Stop condition setup time	^{t}SSU:STO	6.7		µs	
Data-out hold time	^{t}SDH	300		ns	
WRITE cycle time	^{t}SWR		15	ms	2

NOTE: 1. All voltages referenced to V_{SS}.
2. This parameter is sampled. SV_{DD} = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} ($V_{I, ABS}$) ..... -0.3V to V_{DD} +0.3V

Voltage on inputs, NC or I/O Pins Relative to V_{SS} ($V_{DD, ABS}$) ..... -0.5V to V_{DD} +1.0V

Operating Temperature (T_{PLATE}), T_A (ambient) ..... 0°C to +70°C

Storage Temperature (T_{STORE}, plastic) ..... -50°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	2.50 - 0.13	2.50 + 0.13	V
CMOS I/O SUPPLY VOLTAGE FOR 2.5V CONTROLLERS CMOS I/O SUPPLY VOLTAGE FOR 1.8V CONTROLLERS	V_{CMOS}	2.50 - 0.13 1.8 - 0.1	2.50 + 0.25 1.8 + 0.2	V V
VOLTAGE REFERENCE	V_{REF}	1.4 - 0.2	1.4 + 0.2	V
RSL INPUT LOW VOLTAGE	V_{IL}	V_{REF} - 0.5	V_{REF} - 0.2	V
RSL INPUT HIGH VOLTAGE	V_{IH}	V_{REF} + 0.2	V_{REF} + 0.5	V
CMOS INPUT LOW VOLTAGE	$V_{IL, CMOS}$	-0.3	$0.5V_{CMOS}$ - 0.25	V
CMOS INPUT HIGH VOLTAGE	$V_{IH, CMOS}$	$0.5V_{CMOS}$ + 0.25	V_{CMOS} + 0.3	V
CMOS OUTPUT LOW VOLTAGE @ $I_{OL,CMOS}$ = 1mA	$V_{OL, CMOS}$		0.3	V
CMOS OUTPUT HIGH VOLTAGE @ $I_{OH,CMOS}$ = -0.25mA	$V_{OH, CMOS}$	V_{CMOS} - 0.3		V
V_{REF} CURRENT @ V_{REF} (MAX)	I_{REF}	-10 x nRDRAMS[2]	10 x nRDRAMS[2]	µA
CMOS INPUT LEAKAGE CURRENT @ ($0 \le V_{CMOS} \le V_{DD}$)	$I_{SCK, CMD}$	-10 x nRDRAMS[2]	10 x nRDRAMS[2]	µA
CMOS INPUT LEAKAGE CURRENT @ ($0 \le V_{CMOS} \le V_{DD}$)	$I_{SIN, SOUT}$	-10.0	10.0	µA

NOTES: 1. All voltages referenced to V_{SS}.
2. Number of RDRAMS (nRDRAMS) for a specific RIMM module; MT4VR3216/18A = 4, MT8VR6416/18A = 8, MT16VR12816/18A = 16

I_{DD} SPECIFICATIONS AND CONDITIONS (MAX)

PARAMETER/CONDITION	CLOCK RATE	SYMBOL	MT4VR32		MT8VR64		MT16VR128		UNITS
			x16	x18	x16	x18	x16	x18	
One RDRAM in Read, balance in NAP mode	300 MHz	I_{DD1}	410	420	420	430	445	455	mA
	357 MHz		465	475	475	485	500	510	
	400 MHz		515	525	525	535	555	565	
One RDRAM in Read, balance in Standby mode	300 MHz	I_{DD2}	805	815	820	830	880	890	mA
	357 MHz		900	910	915	925	960	970	
	400 MHz		970	980	990	1000	1040	1050	
One RDRAM in Read, balance in Active mode	300 MHz	I_{DD3}	1215	1225	1240	1250	1305	1315	mA
	357 MHz		1270	1280	1295	1305	1360	1370	
	400 MHz		1345	1355	1370	1380	1440	1450	
One RDRAM in Write, balance in NAP mode	300 MHz	I_{DD4}	390	400	395	405	415	425	mA
	357 MHz		440	450	450	460	475	485	
	400 MHz		480	490	490	500	515	525	
One RDRAM in Write, balance in Standby mode	300 MHz	I_{DD5}	785	795	800	810	840	850	mA
	357 MHz		875	885	890	900	935	945	
	400 MHz		940	950	960	970	1010	1020	
One RDRAM in Write, balance in Active mode	300 MHz	I_{DD6}	1110	1120	1130	1140	1190	1200	mA
	357 MHz		1230	1240	1255	1265	1320	1330	
	400 MHz		1335	1345	1360	370	1430	1440	

NOTES: 1. Actual power will depend on individual RDRAM component specifications, memory controller usage patterns. Power does not include Refresh Current.

2. I/O current is a function of the % of 1's, to add I/O power for 50% 1's for a x16 need to add 257mA or 290mA for x18 ECC module for the following: V_{DD} = 2.5V, V_{TERM} = 1.8V, V_{REF} = 1.4V and V_{DIL} = V_{REF} - 0.5V.

AC ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Module Impedance of RSL Signals	Z_L	25.2	28	30.8	Ω
Module Impedance of SCK and CMD signals	$Z_{UL-CMOS}$	23.8	28	32.2	Ω
Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN)	T_{PD}[2]	–		See Table[1]	ns
Propagation delay variation of RSL signals with respect to T_{PD}^{BC} for MT4VR3216/18A and MT8VR6416/18A	ΔT_{PD}	-21		21	ps
Propagation delay variation of RSL signals with respect to T_{PD}^{BC} for MT16VR12816/18A	ΔT_{PD}	-21		21	ps
Propagation delay variation of SCK and CMD signals with respect to an average clock delay *b*	$\Delta T_{PD-CMOS}$	-100		100	ps
Attenuation Limit	V/V_{IN}			See Table[1]	%
Fwrd crosstalk coefficient (300ps input rise time @ 20%–80%)	V_{XF}/V_{IN}			See Table[1]	%
Bkwrd crosstalk coefficient (300ps input rise time @ 20%–80%)	V_{XB}/V_{IN}			See Table[1]	%

NOTES: 1. The "Adjusted DTpd Specification" table lists parameters and specifications for different storage capacity RIMM modules that use 128Mb or 144Mb RDRAM.
2. T_{PD} or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).
3. If the RIMM module meets the following specification, then it is compliant to the specification. If the RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted DT_{PD} Specification" table.

ADJUSTED ΔTPD SPECIFICATION

PARAMETER/CONDITION	ADJUSTED MIN/MAX	ABSOLUTE		UNITS
		MIN	MAX	
Propagation delay variation of RSL signals with respect to TPD for MT6VR3216/18A and MT6VR6416/18A	± [17+(18*N*ΔZ0)][1]	-30	30	ps
Propagation delay variation of RSL signals with respect to TPD for MT6VR12816/18A	± [24+(18*N*ΔZ0)][1]	-50	50	ps

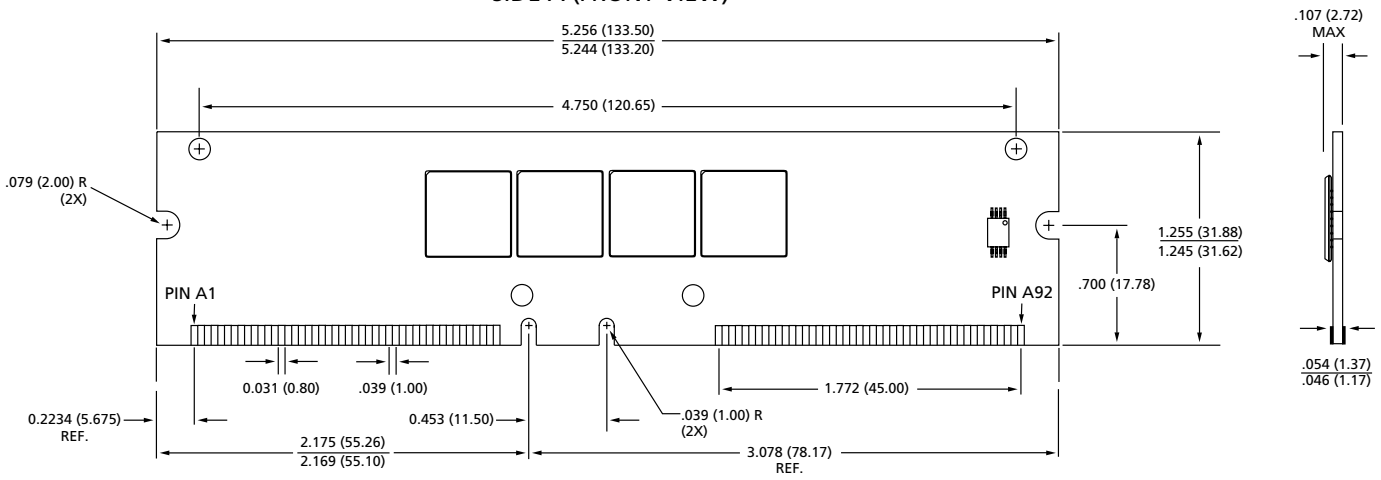
NOTES 1. N = Number of RDRAM devices installed on the RIMM module; MT4VR3216/18A = 4, MT8VR6416/18A = 8, MT4VR12816/18A = 16
ΔZ0 = delta Z0% = (MAX Z0 - MIN Z0) / (MIN Z0)
(MAX Z0 and MIN Z0 are obtained from the loaded (High-Z) impedance coupons of all RSL layers on the modules)

AC ELECTRICAL SPECIFICATIONS FOR RIMM MODULE

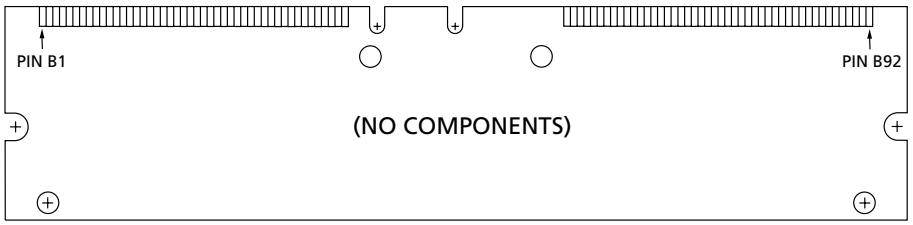
PARAMETER/CONDITION	CLOCK RATE	SYMBOL	MT4VR32		MT8VR64		MT16VR128		UNITS
			x16	x18	x16	x18	x16	x18	
Propagation Delay, all RSL signals.	300 MHz	TPD	1.25	1.25	1.60	1.60	2.10	2.10	ns
	357 MHz		1.25	1.25	1.56	1.56	2.06	2.06	
	400 MHz		1.25	1.25	1.56	1.56	2.06	2.06	
Attenuation Limit	300 MHz	Vα/VIN	8	8	10	10	21	21	%
	357 MHz		12	12	16	16	25	25	
	400 MHz		12	12	16	16	25	25	
Forward crosstalk coefficient 300ps input rise time @ 20%–80%	300 MHz	VXF/VIN	2	2	4	4	8	8	%
	357 MHz		2	2	4	4	8	8	
	400 MHz		2	2	4	4	8	8	
Backward crosstalk coefficient 300ps input rise time @ 20%–80%	300 MHz	VXB/VIN	1.5	1.5	2.0	2.0	2.5	2.5	%
	357 MHz		1.5	1.5	2.0	2.0	2.5	2.5	
	400 MHz		1.5	1.5	2.0	2.0	2.5	2.5	
DC Resistance Limit	300 MHz	RDC	0.6	0.6	0.8	0.8	1.2	1.2	Ω
	357 MHz		0.6	0.6	0.8	0.8	1.2	1.2	
	400 MHz		0.6	0.6	0.8	0.8	1.2	1.2	

184-PIN RIMM MODULE
32 MEG x 16 (64MB), 32 MEG x 18 (72MB)

SIDE A (FRONT VIEW)



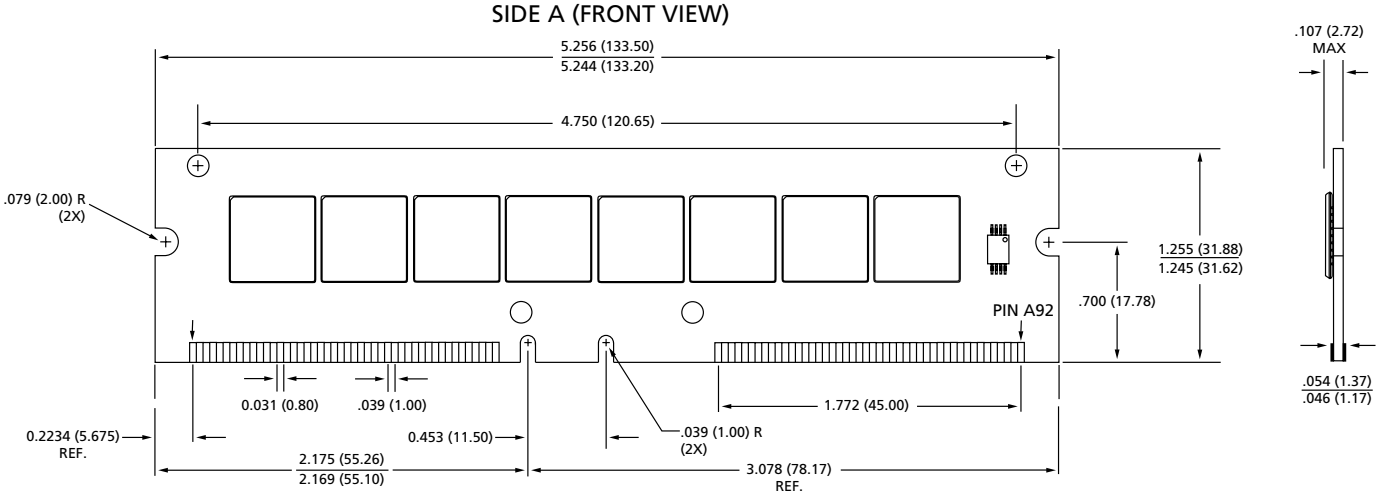
SIDE B (BACK VIEW)



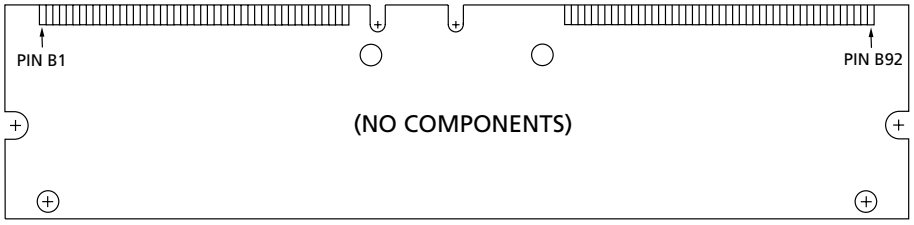
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

184-PIN RIMM MODULE
64 MEG x 16 (128MB), 64 MEG x 18 (144MB)

SIDE A (FRONT VIEW)



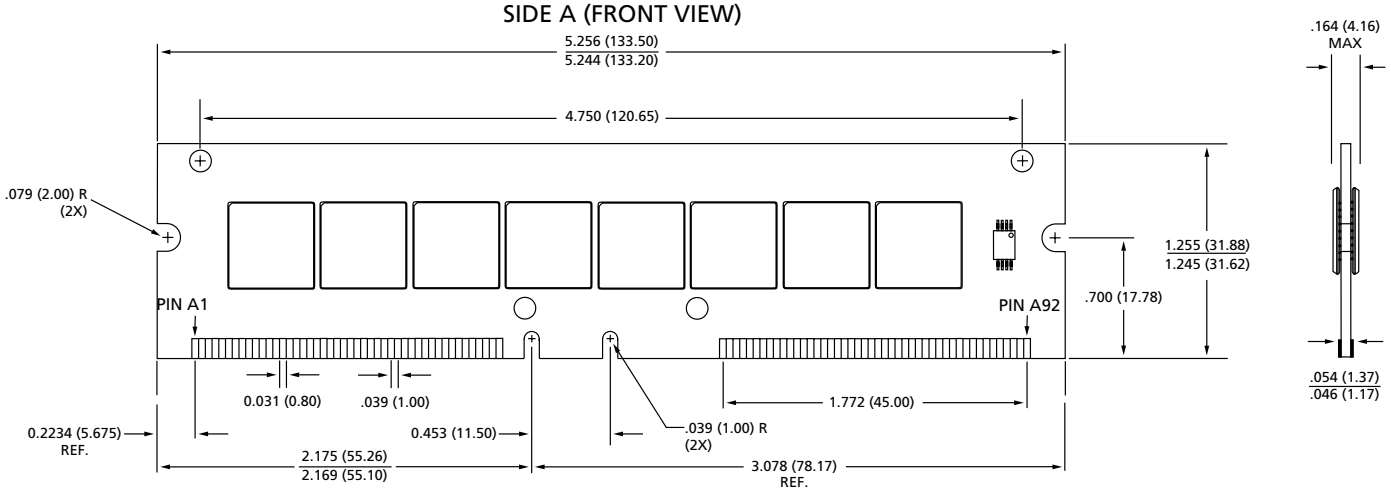
SIDE B (BACK VIEW)



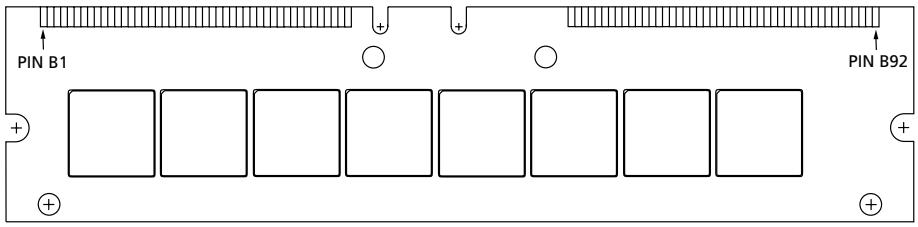
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

184-PIN RIMM MODULE
128 MEG x 16 (256MB), 128 MEG x 18 (288MB)

SIDE A (FRONT VIEW)



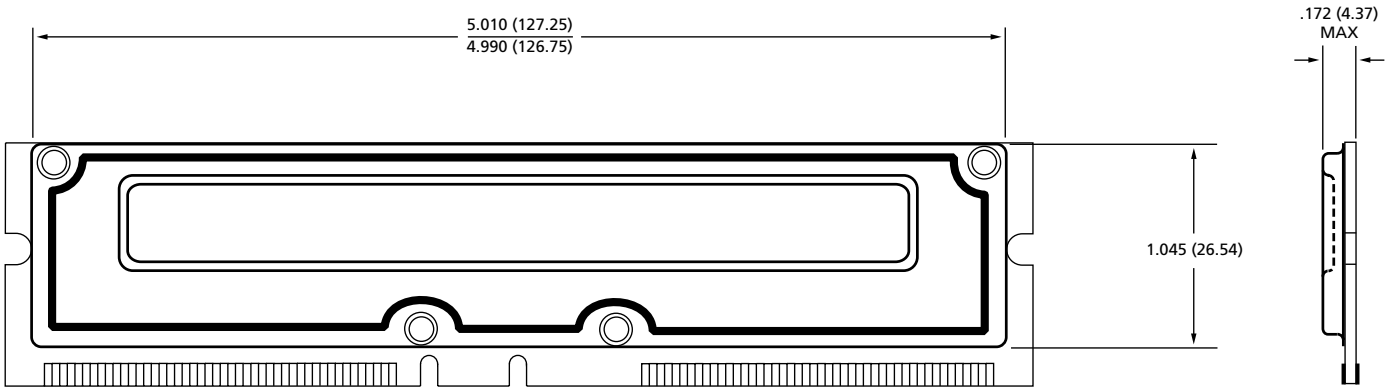
SIDE B (BACK VIEW)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

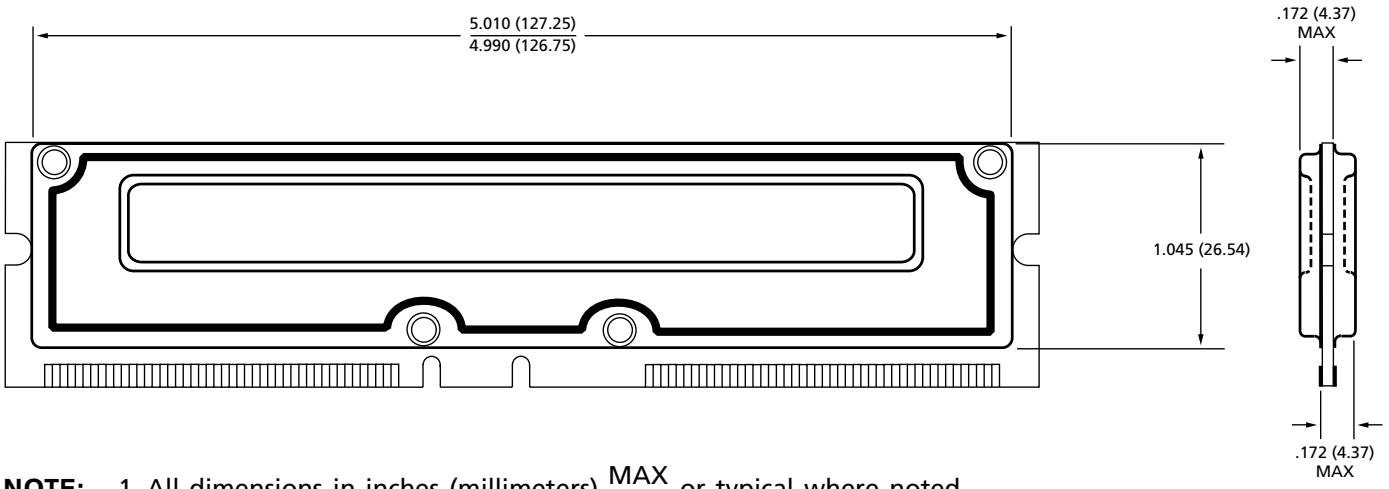
32 MEG x 16 (64MB), 32 MEG x 18 (72MB)
64 MEG x 16 (128MB), 64 MEG x 18 (144MB)

SIDE A (FRONT VIEW) WITH HEAT SPREADER



128 MEG x 16 (256MB), 128 MEG x 18 (288MB)

SIDE A (FRONT VIEW) WITH HEAT SPREADER



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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