19-2416; Rev 1; 10/02

+14dBm to +20dBm LO Buffers/Splitters with ±1dB Variation

General Description

The MAX9987 and MAX9988 LO buffers/splitters each integrate a passive two-way power splitter with high-isolation input and output buffer amplifiers. These buffers are designed to provide the high output (+14dBm to +20dBm) necessary to drive the LO inputs of high-linearity passive mixers, while offering 40dB reverse isolation to prevent LO pulling. The MAX9987 is internally matched for the cellular/GSM bands, and the MAX9988 is matched for the DCS/PCS/UMTS bands.

The typical application circuit provides a nominal +17dBm output power with ±1dB variation over supply, temperature, and input power. With two optional resistors, the output power can be precision set from +14dBm to +20dBm. The devices offer more than 30dB output-to-output port isolation, and are offered in 5mm × 5mm 20-pin QFN packages with exposed paddle.

Applications

Cellular/GSM/DCS/PCS/UMTS Base Station Tx/Rx LO Drive

Base Station Main and Diversity Channels

Coherent Receivers

ISM Wireless LAN

Wireless Local Loop

Local Multipoint Distribution Service

Point-to-Point Systems

Features

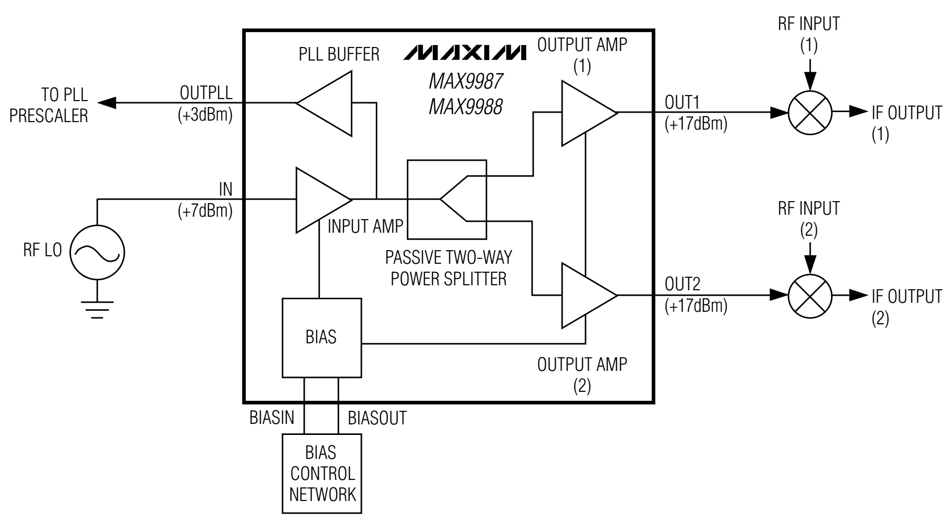
- ♦ ±1dB Output Power Variation
- ♦ +14dBm to +20dBm Adjustable Output Power
- ♦ Two-Way Power Splitting
- ♦ 40dB Reverse Isolation
- ♦ More than 30dB Output-to-Output Isolation
- ♦ Low Output Noise: -170dBc/Hz at +17dBm
- ♦ 160mA Supply Current at +17dBm
- ♦ ESD Protection
- ♦ Isolated PLL Output (+3dBm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FREQUENCY RANGE
MAX9987EGP	-40°C to 85°C	20 QFN-EP*	700MHz to 1100MHz
MAX9988EGP	-40°C to 85°C	20 QFN-EP*	1500MHz to 2200MHz

**EP = Exposed paddle.*

Typical Operating Circuit and Block Diagram



+14dBm to +20dBm LO Buffers/Splitters with ±1dB Variation

ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2, VCC3,
VCCREF to GND...-0.3V to +6.0V
IN to GND..-0.3V to (V_{CC} + 0.3V)
OUT1, OUT2,
OUTPLL to GND.....................................-0.3V to (V_{CC} + 0.3V)
REF to GND ....Source/Sink 5mA
INBIAS, OUTBIAS, to GND.................................-0.3V to +0.75V
PLLBIAS ....Sink 25mA
RF Input Power ....+20dBm

Continuous Power Dissipation (T_A = +70°C)
5mm × 5mm 20-Pin QFN (derate 20mW/°C above +70°C)...1600mW
θ_{JA}..50°C/W
Junction Temperature ....+150°C
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—MAX9987

(Typical Application Circuit, V_{CC} = 4.75V to 5.25V, input and outputs terminated in 50Ω, T_A = -40°C to +85°C. Typical specifications are for V_{CC} = 5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Supply Current	I_{CC}	Low power setting (see Table 1 for resistor values)		110		mA
		Nominal power setting (R_1, R_2, R_4, and R_5 not installed)	139	155	171	
		High power setting (see Table 1 for resistor values)		221		

DC ELECTRICAL CHARACTERISTICS—MAX9988

(Typical Application Circuit, V_{CC} = 4.75V to 5.25V, input and outputs terminated in 50Ω, T_A = -40°C to +85°C. Typical specifications are for V_{CC} = 5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Supply Current	I_{CC}	Low power setting (see Table 1 for resistor values)		120		mA
		Nominal power setting (R_1, R_2, R_4, and R_5 not installed)	150	162	175	
		High power setting (see Table 1 for resistor values)		229		

AC ELECTRICAL CHARACTERISTICS—MAX9987

(Typical Application Circuit, V_{CC} = 4.75V to 5.25V, 50Ω environment, +4dBm < P_{IN} < +10dBm, 700MHz < f_{IN} < 1100MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are for V_{CC} = 5.0V, P_{IN} = +7dBm, f_{IN} = 900MHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f		700		1100	MHz
Output Power (Main Drivers)	P_{OUTLO}	Low power setting, P_{IN} = +4dBm (see Table 1 for resistor values)		14.3		dBm
		Nominal power setting, +4dBm < P_{IN} < +10dBm, 4.75V < V_{CC} < 5.25V, -40°C < T_A < +85°C (R_1, R_2, R_4, and R_5 not installed)		17.3 ±0.8		
		High power setting, P_{IN} = +10dBm (see Table 1 for resistor values)		19.7		
Output Power (PLL Driver)	P_{OUTPLL}			3.7		dBm
Input VSWR	$VSWR_{IN}$			1.2:1		
Output VSWR	$VSWR_{OUT}$			1.7:1		
Output-Noise Power Density	P_{NOISE}	V_{CC} = 5.0V, ±100MHz offset (R_1, R_2, R_4, and R_5 not installed)		-152		dBm/Hz
OUT1 to OUT2 Isolation	S23	V_{CC} = 5.0V, nominal power setting (R_1, R_2, R_4, and R_5 not installed)		45		dB
OUT2 to OUT1 Isolation	S32	V_{CC} = 5.0V, nominal power setting (R_1, R_2, R_4, and R_5 not installed)		39		dB
OUT1 to RFIN Isolation	S12	V_{CC} = 5.0V, nominal power setting (R_1, R_2, R_4, and R_5 not installed)		48		dB
OUT2 to RFIN Isolation	S13	V_{CC} = 5.0V, nominal power setting (R_1, R_2, R_4, and R_5 not installed)		50		dB

AC ELECTRICAL CHARACTERISTICS—MAX9988

(Typical Application Circuit, V_{CC} = 4.75V to 5.25V, 50Ω environment, +6dBm < P_{IN} < +12dBm, 1500MHz < f_{IN} < 2200MHz, and T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are for V_{CC} = 5.0V, P_{IN} = +9dBm, f_{IN} = 1800MHz, and T_A = +25°C unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f		1500		2200	MHz
Output Power (Main Drivers)	P_{OUTLO}	Low power setting, P_{IN} = +6dBm (see Table 1 for resistor values)		14.2		dBm
		Nominal power setting, +6dBm < P_{IN} < +12dBm, 4.75V < V_{CC} < 5.25V, -40°C < T_A < +85°C (R_1, R_2, R_4, and R_5 not installed)		17.3 ±0.8		
		High power setting, P_{IN} = +12dBm (see Table 1 for resistor values)		19.5		
Output Power (PLL Driver)	P_{OUTPLL}			3.6		dBm
Input VSWR	$VSWR_{IN}$			1.5:1		
Output VSWR	$VSWR_{OUT}$			1.4:1		
Output-Noise Power Density	P_{NOISE}	V_{CC} = 5.0V, ±100MHz offset		-152		dBm/Hz
OUT1 to OUT2 Isolation	S23	V_{CC} = 5.0V, nominal power setting (R_1, R_2, R_4, and R_5 not installed)		33		dB
OUT2 to OUT1 Isolation	S32	V_{CC} = 5.0V, nominal power setting (R_1, R_2, R_4, and R_5 not installed)		44		dB
OUT1 to RFIN Isolation	S12	V_{CC} = 5.0V, nominal power setting (R_1, R_2, R_4, and R_5 not installed)		49		dB
OUT2 to RFIN Isolation	S13	V_{CC} = 5.0V, nominal power setting (R_1, R_2, R_4, and R_5 not installed)		47		dB

Note 1: Devices are 100% DC screened and AC production tested for functionality. Data sheet typical specifications are derived from the average of 30 units from a typical lot, and are tested under the conditions specified for the typical specifications.

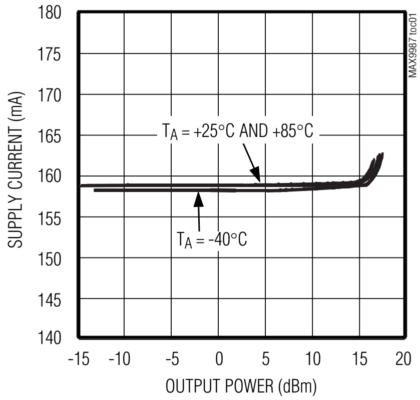
+14dBm to +20dBm LO Buffers/Splitters with ±1dB Variation

Typical Operating Characteristics

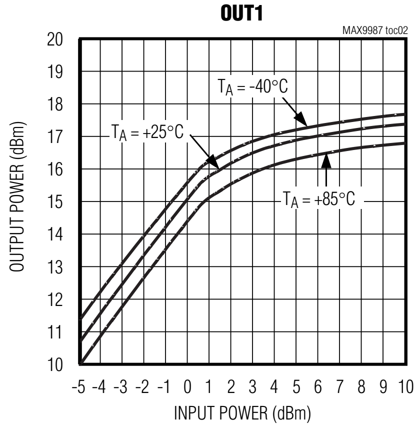
(V_{CC} = 5.0V, nominal bias, f_{IN} = 900MHz, P_{IN} = +7dBm, T_A = +25°C, unless otherwise noted.) (Shaded regions are outside the guaranteed operating range, and are provided for reference only.)

MAX9987

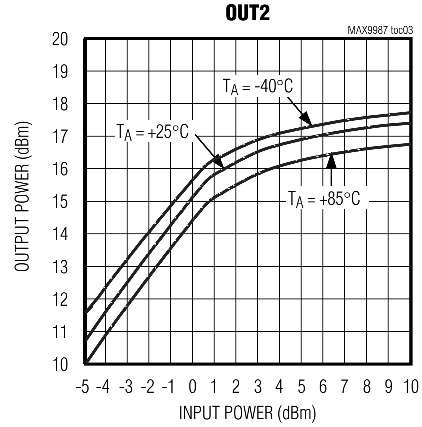
SUPPLY CURRENT vs. OUTPUT POWER OUTMAIN



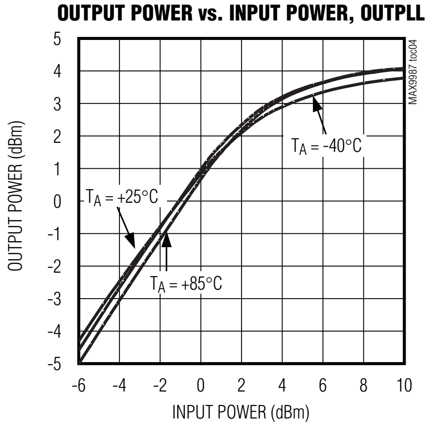
OUTPUT POWER vs. INPUT POWER OUT1



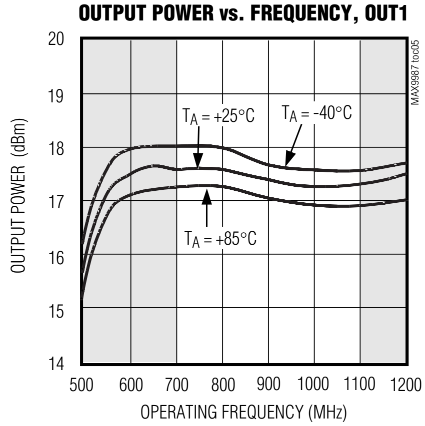
OUTPUT POWER vs. INPUT POWER OUT2



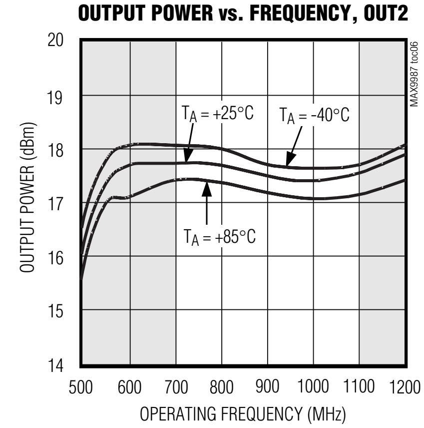
OUTPUT POWER vs. INPUT POWER, OUTPLL



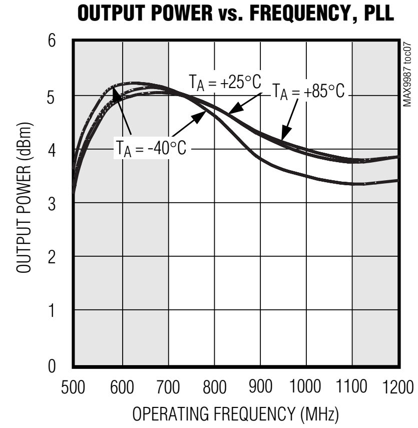
OUTPUT POWER vs. FREQUENCY, OUT1



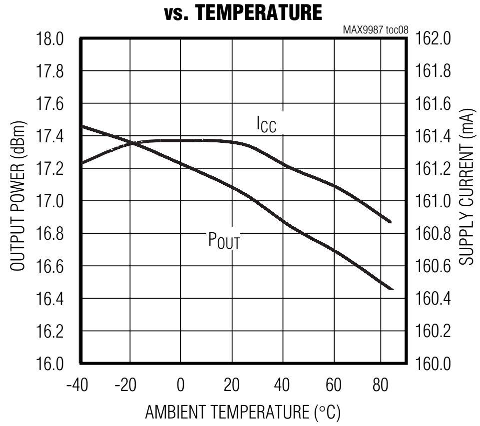
OUTPUT POWER vs. FREQUENCY, OUT2



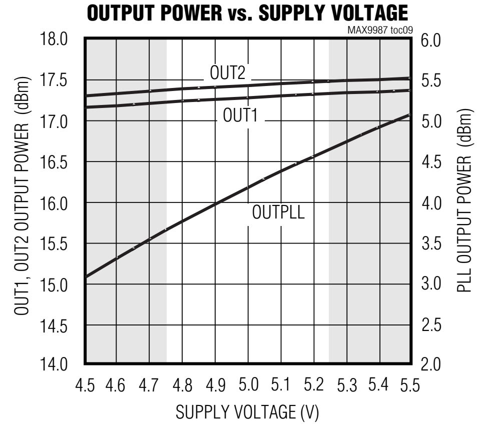
OUTPUT POWER vs. FREQUENCY, PLL



OUTPUT POWER AND SUPPLY CURRENT vs. TEMPERATURE



OUTPUT POWER vs. SUPPLY VOLTAGE



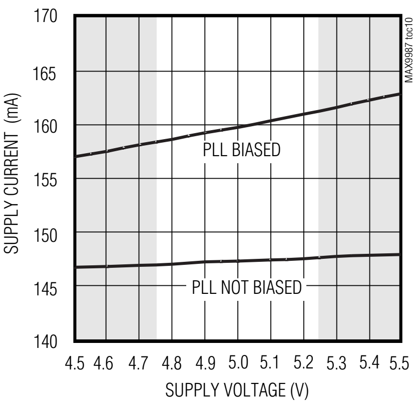
+14dBm to +20dBm LO Buffers/Splitters with ±1dB Variation

Typical Operating Characteristics (continued)

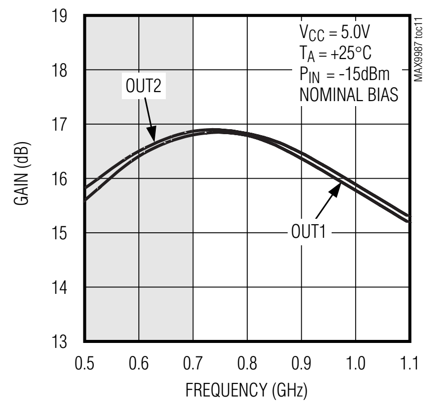
(V_{CC} = 5.0V, nominal bias, f_{IN} = 900MHz, P_{IN} = +7dBm, T_A = +25°C, unless otherwise noted.) (Shaded regions are outside the guaranteed operating range, and are provided for reference only.)

MAX9987

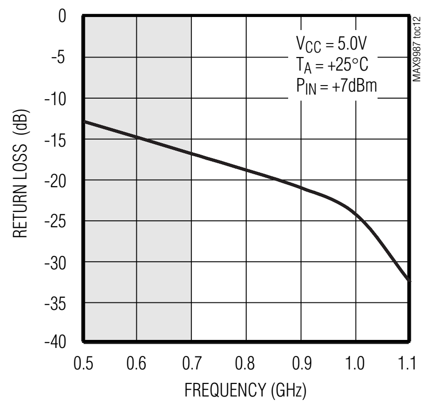
SUPPLY CURRENT vs. SUPPLY VOLTAGE



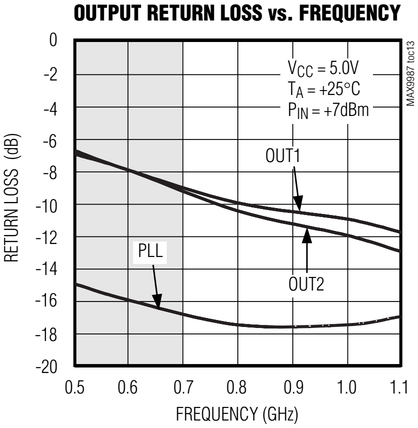
SMALL-SIGNAL GAIN vs. FREQUENCY



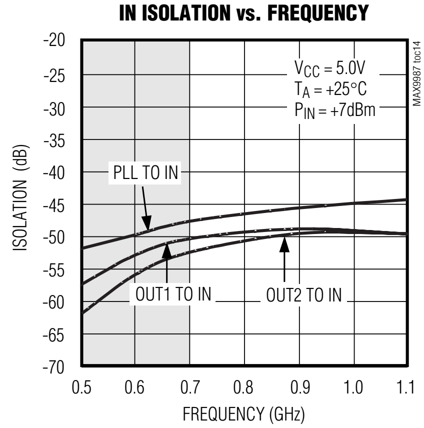
INPUT RETURN LOSS vs. FREQUENCY



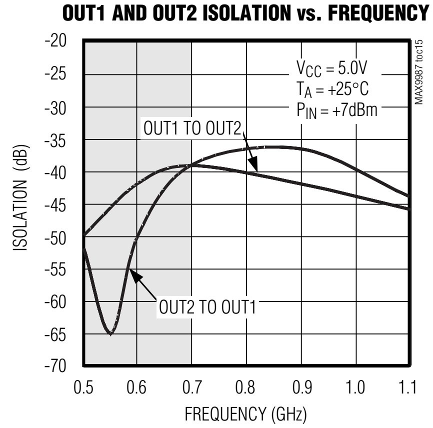
OUTPUT RETURN LOSS vs. FREQUENCY



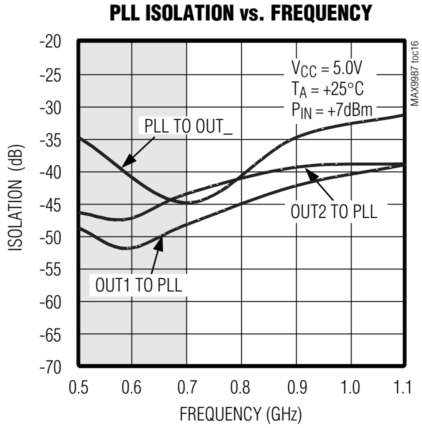
IN ISOLATION vs. FREQUENCY



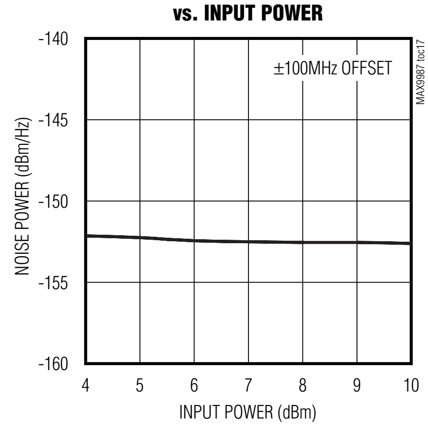
OUT1 AND OUT2 ISOLATION vs. FREQUENCY



PLL ISOLATION vs. FREQUENCY



OUTPUT NOISE POWER vs. INPUT POWER

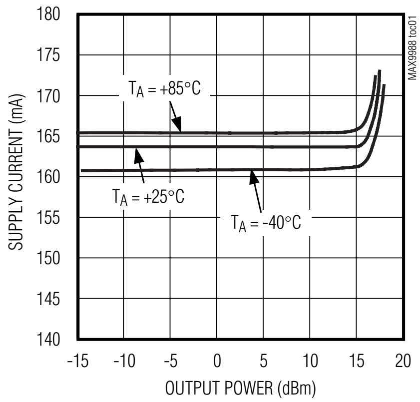


Typical Operating Characteristics (continued)

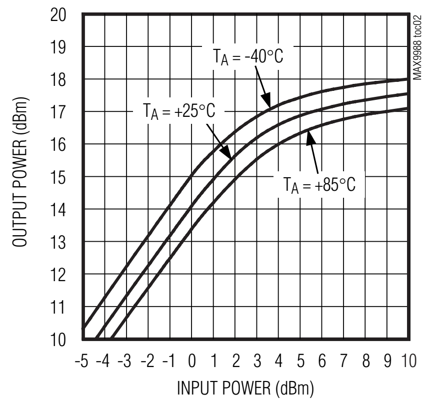
(V_{CC} = 5.0V, nominal bias, f_{IN} = 1800MHz, P_{IN} = +7dBm, T_A = +25°C, unless otherwise noted.) (Shaded regions are outside the guaranteed operating range, and are provided for reference only.)

MAX9988

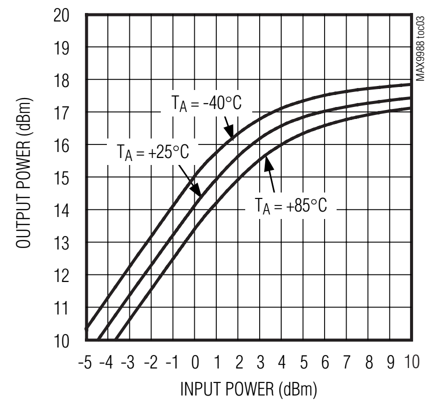
SUPPLY CURRENT vs. OUTPUT POWER



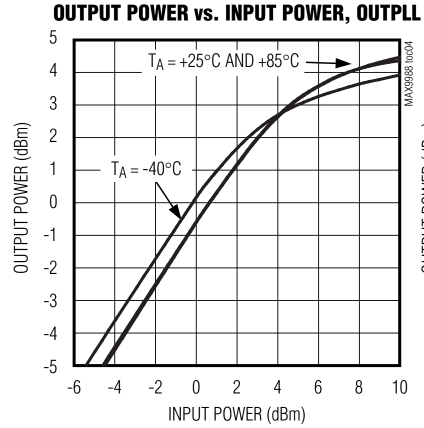
OUTPUT POWER vs. INPUT POWER, OUT1



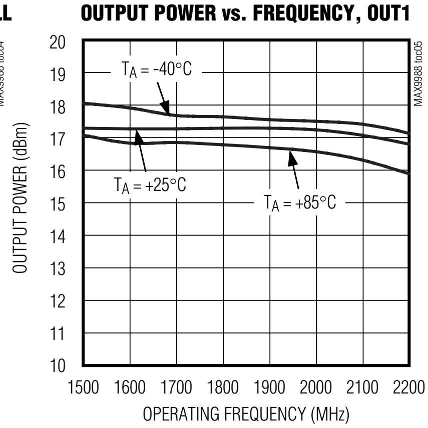
OUTPUT POWER vs. INPUT POWER, OUT2



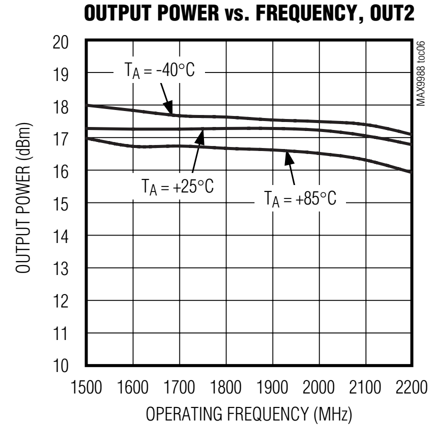
OUTPUT POWER vs. INPUT POWER, OUTPLL



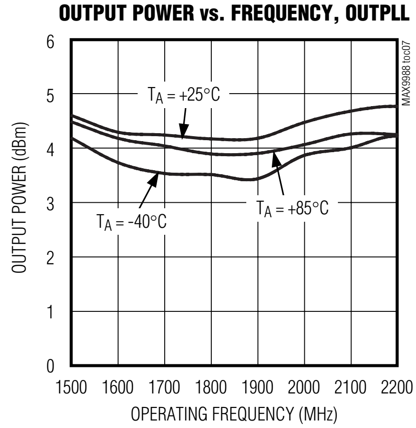
OUTPUT POWER vs. FREQUENCY, OUT1



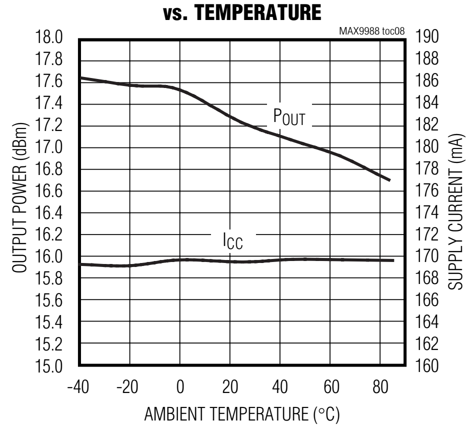
OUTPUT POWER vs. FREQUENCY, OUT2



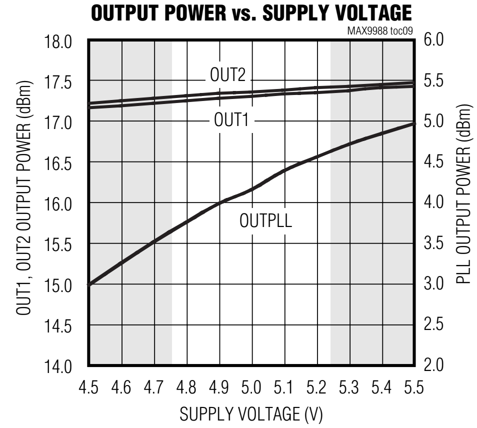
OUTPUT POWER vs. FREQUENCY, OUTPLL



OUTPUT POWER AND SUPPLY CURRENT vs. TEMPERATURE



OUTPUT POWER vs. SUPPLY VOLTAGE



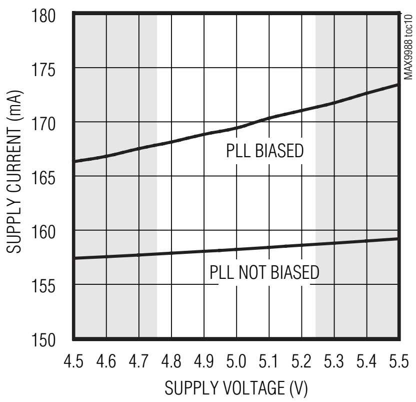
+14dBm to +20dBm LO Buffers/Splitters with ±1dB Variation

Typical Operating Characteristics (continued)

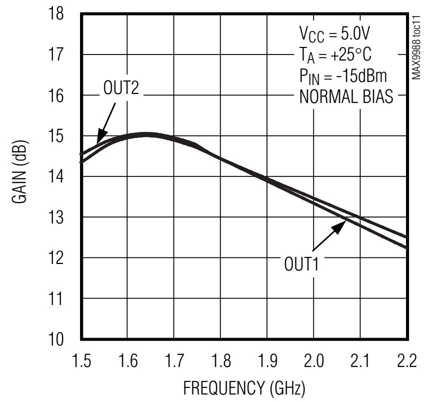
(V_{CC} = 5.0V, nominal bias, f_{IN} = 1800MHz, P_{IN} = +7dBm, T_A = +25°C, unless otherwise noted.) (Shaded regions are outside the guaranteed operating range, and are provided for reference only.)

MAX9988

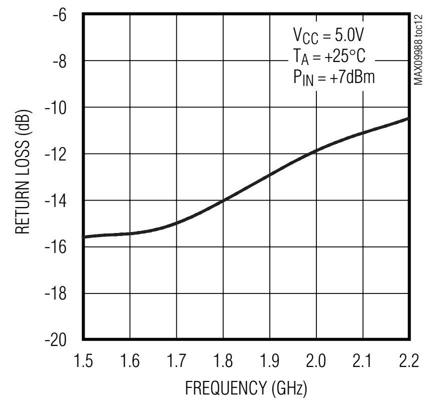
SUPPLY CURRENT vs. SUPPLY VOLTAGE



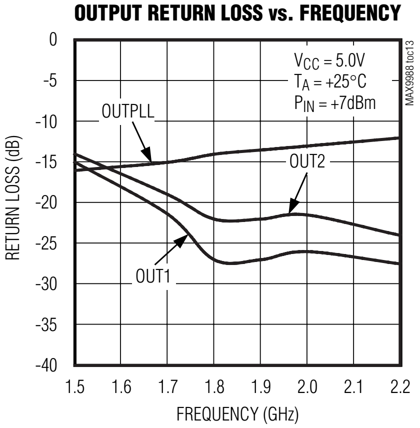
SMALL-SIGNAL GAIN vs. FREQUENCY



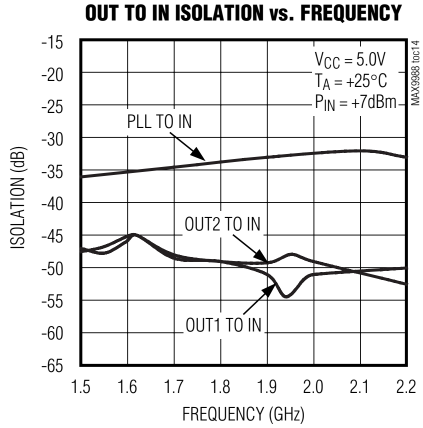
INPUT RETURN LOSS vs. FREQUENCY



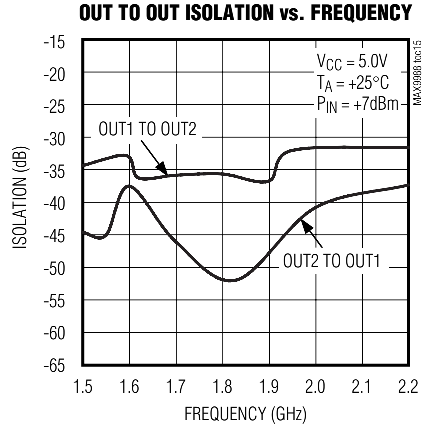
OUTPUT RETURN LOSS vs. FREQUENCY



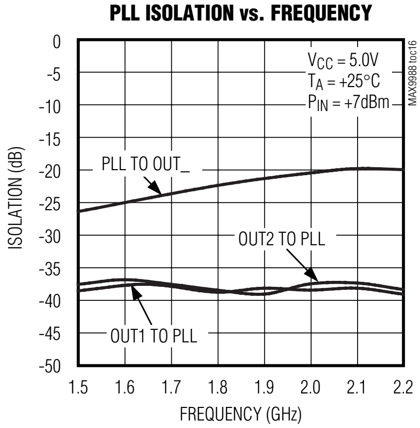
OUT TO IN ISOLATION vs. FREQUENCY



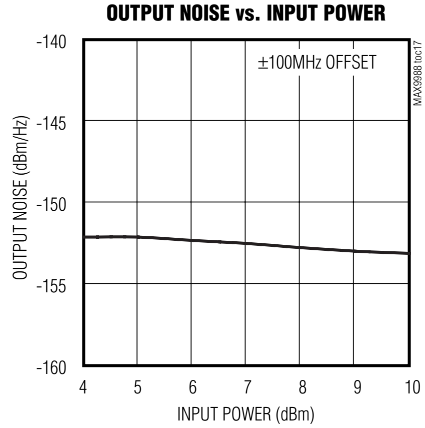
OUT TO OUT ISOLATION vs. FREQUENCY



PLL ISOLATION vs. FREQUENCY



OUTPUT NOISE vs. INPUT POWER



Pin Description

PIN	NAME	FUNCTION
1, 4, 8, 9, 13, 17, 18, EP	GND	Ground
2	IN	Input. Internally matched 50Ω RF input. AC couple to this pin.
3	VCCREF	Supply. Supply connection for on-chip voltage and current references. See *Applications Information* for information on decoupling.
5	REF	Voltage Reference Output. Output for on-chip 1.5V bandgap voltage reference. See *Applications Information* section for information on decoupling.
6	BIASIN	Bias Connection for Input Buffer. Set compressed power point for input amplifier with a resistor to REF or GND. For +17dBm output power, no external biasing resistors are required. See *Applications Information* section for information.
7	BIASOUT	Bias Connection for Output Amplifiers. Set compressed power point for OUT1 and OUT2 with a resistor to REF or ground. For +17dBm output power, no external biasing resistors are required. See *Applications Information* section for information.
10	OUT2	Output 2. Internally matched 50Ω RF output. AC couple to this pin.
11, 12	VCC3	Supply. Supply connection for OUT2.
14, 15	VCC2	Supply. Supply connection for OUT1.
16	OUT1	Output 1. Internally matched 50Ω RF output. AC couple to this pin.
19	VCC1	Supply. Supply connection for input amplifier.
20	OUTPLL	Output PLL. Output for driving optional external PLL.

Detailed Description

The MAX9987/MAX9988 LO amplifiers/splitters each consist of a single input amplifier, a two-way passive power splitter, two separate output amplifiers, as well as a third buffer amplifier to drive the LO's PLL. The bias currents for the amplifiers are adjustable through off-chip resistors. This allows the output level to be precision set anywhere from +14dBm to +20dBm. The PLL output is preset to +3dBm (about 900mV$_{P-P}$ into 50Ω).

Power levels are typically ±1dB over the full supply, input power, frequency, and temperature range. Precision power control is achieved by internal control circuitry. Maintaining tight power control keeps the system engineer from over specifying the LO drive in order to guarantee a linearity specification in the base-station mixer.

More than 40dB isolation between the LO outputs and the input prevents VCO pulling, and the 30dB output-to-output isolation reduces branch-to-branch coupling.

The MAX9987 is specified from 700MHz to 1100MHz, and the MAX9988 is specified from 1500MHz to 2200MHz. Both are offered in compact 5mm × 5mm 20-pin QFN packages with exposed paddle.

Input Amplifier

A single low-noise input amplifier before the passive splitter provides gain and isolation. The compressed output power for this stage is controlled by the bias setting resistors R_1 or R_4 (see *Typical Application Circuit*). These resistors are not required for the nominal +17dBm output; see Table 1 for bias resistor values to obtain +14dBm to +20dBm output power.

The input is internally matched to 50Ω, and typical VSWR is no more than 2:1 over all operating conditions. Since the input is internally biased, provide a DC block at the input pin.

PLL Amplifier and Output

A small amount of power is tapped off from the input amplifier's output, and fed to a high-isolation buffer to drive the PLL output at +3dBm. If the PLL output is not required, it can be disabled by removing R_3; disabling the PLL output saves 12mA supply current.

Passive Two-Way Splitter

The input amplifier drives an integrated power splitter. All impedance matching between stages is on-chip, so no external tuning components are required.

+14dBm to +20dBm LO Buffers/Splitters with ±1dB Variation

Table 1. External Resistor Values for +14dBm to +20dBm Output Power

NOMINAL OUTPUT POWER (dBm)	R_1 (Ω)	R_2 (Ω)	R_4 (Ω)	R_5 (Ω)	MAX9987 INPUT DRIVE (dBm)	MAX9988 INPUT DRIVE (dBm)
+20	1.35k	2.0k	Open	Open	10 ±3	12 ±3
+19	2.2k	3.0k	Open	Open	9 ±3	11 ±3
+18	5.0k	6.0k	Open	Open	8 ±3	10 ±3
+17	Open	Open	Open	Open	7 ±3	9 ±3
+16	Open	Open	1.8k	3.0k	6 ±3	8 ±3
+15	Open	Open	0.9k	1.1k	5 ±3	7 ±3
+14	Open	Open	0.6k	0.6k	4 ±3	6 ±3

Table 2. Component Values for Typical Application Circuit

DESIGNATION	COMPONENT VALUE	
	MAX9987 (LOWBAND)	MAX9988 (HIGHBAND)
C1, C6	100nF	100nF
C3	100pF	100nF
C2, C4, C5, C7, C8, C9, C12, C13, C14	47pF	22pF
C10, C11	5pF	10pF
R1, R2, R4, R5	See Table 1	See Table 1
R3	100Ω	100Ω

Driver Amplifiers and Outputs

Each of the output amplifiers are similar to the input amplifier, except they are biased higher to provide more output power. For example, with an input power of +10dBm, the MAX9987 can deliver +20dBm at both outputs. The bias is adjustable; see Table 1 for details.

Both RF outputs are internally matched to 50Ω, with a typical VSWR limit of 2:1. Provide DC blocking capacitors at the outputs.

Applications Information

Input and Output Matching

All input and output matching is accomplished on-chip; no external matching circuitry is required. Use a DC block of about 47pF (lowband) or 22pF (highband) at the input and the outputs. Because these parts are internally broadband matched, adjusting external component values can optimize performance for a particular band.

Input Drive Level

In the case of the MAX9987, the typical required input drive level is +7dBm for +17dBm output, or +10dBm for +20dBm output. The MAX9988 uses slightly higher input levels (see Table 1). The typical VCO cannot provide sufficient drive by itself; the typical application follows the VCO with attenuation (about +3dB), and then with a low-noise gain block. This allows the VCO to drive the MAX9987/MAX9988 input at the required level without being load-pulled.

Output Drive Level

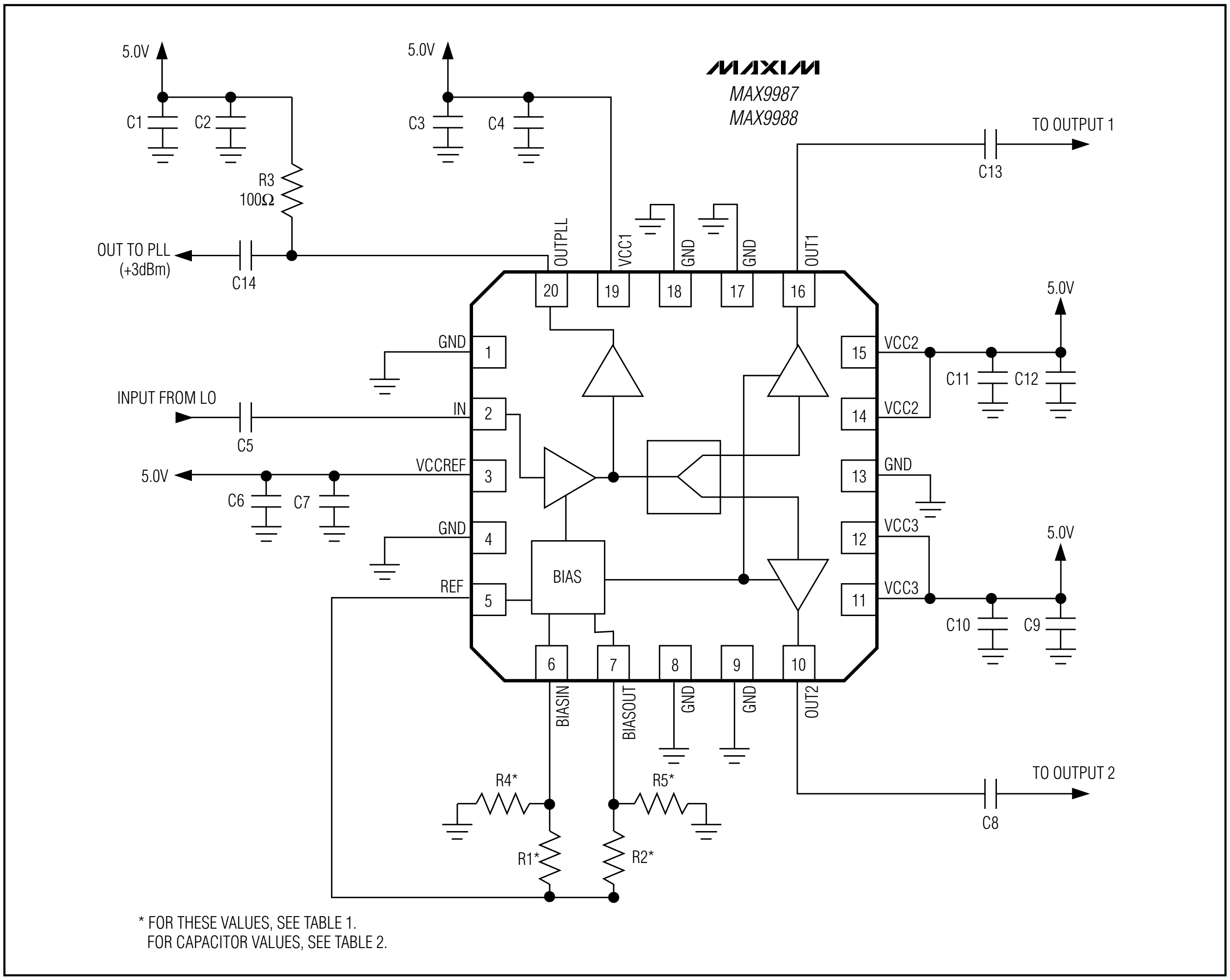
The output drive of the MAX9987/MAX9988 is nominally +17dBm ±1dB. This is the typical application, with no external bias-setting resistors at INBIAS and OUTBIAS. Output power can be set from +14dBm to +20dBm by using the bias-setting resistor values listed in Table 1.

Chip Information

TRANSISTOR COUNT: 89

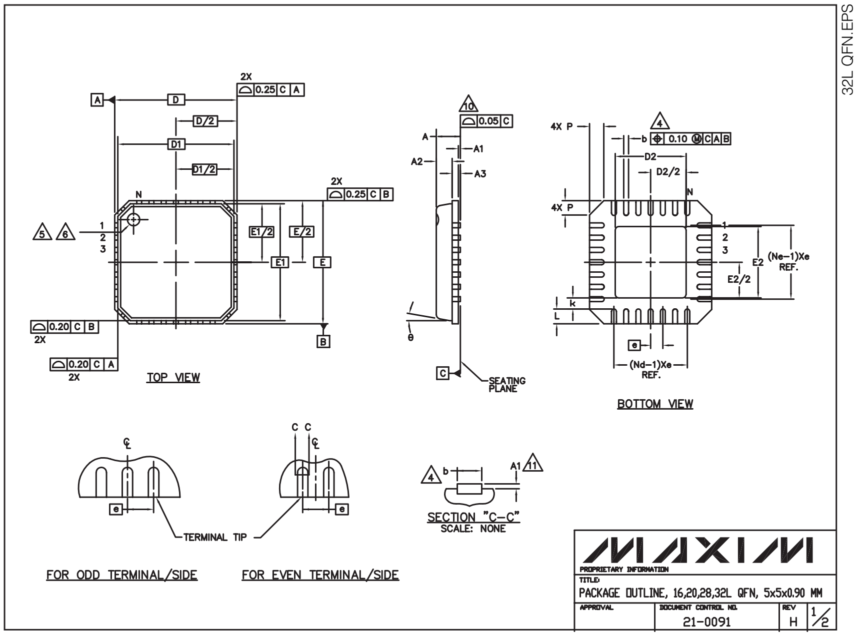
PROCESS: BiCMOS

Typical Application Circuit/Pin Configuration



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0091 | REV H | 2/2