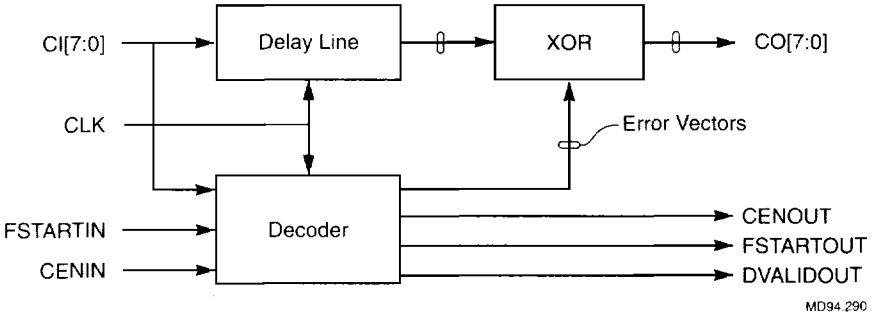
Chapter 6
L64712, L64713, L64714
Decoder Architecture

This section describes the architecture of the LSI Logic family of ECC decoders. The principle of operation in each decoder is the same; they differ in the number of redundant correction bytes that each can decode.

6.1 L64712-14 Decoder Architecture

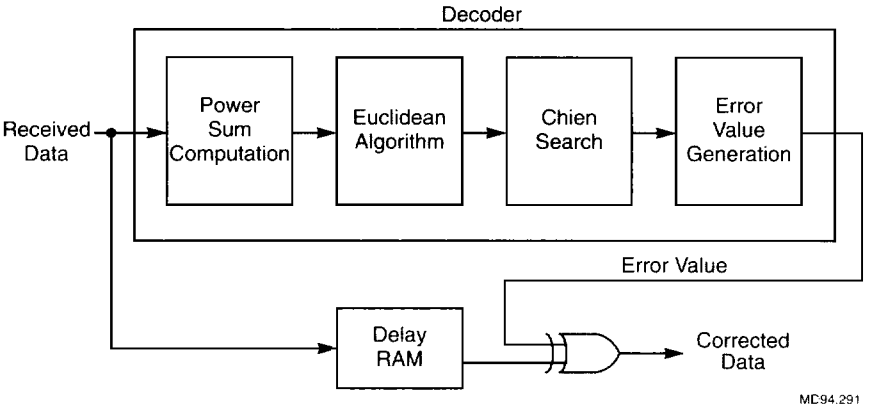
The basic components in the decoder are shown in Figure 6.1. Incoming data is retained in a delay line until error correction has been applied to data in the decoder block.

Figure 6.1
Block Diagram of L6471X Series Decoders



To achieve a high throughput, three decoding stages are mapped into three separate, fully pipelined, hardware units that apply finite field computations to decoder input. The pipeline design requires the internal decoder to run on a bit rate clock. Bit rate is defined as the throughput of information plus parity and gap data. Each hardware unit is dedicated to the computation of one stage of the encoder algorithm, as shown in Figure 6.2. A brief description of each stage of the decoding process follows the figure.

Figure 6.2
Decoder Block Diagram



6.1.1 Power Sum Computation

A finite field polynomial whose degree is one less than the code length is evaluated at various finite field elements. The number of such evaluations is equal to the number of check bytes in a codeword. The result of the computation is summarized in a finite field polynomial called the power sum polynomial.

6.1.2 Euclidean Algorithm

This Euclidean block determines which, if any, bytes are erroneous and finds the value of the byte errors. The decoder uses a version of the Euclidean algorithm (similar to the one for finding the greatest common divisor of two integers), which is applied to the power sum polynomial and another predefined polynomial.

6.1.3 Chien Search

The Chien Search functional block finds the roots of the error locator polynomial at the appropriate field elements to obtain the actual location of the error.

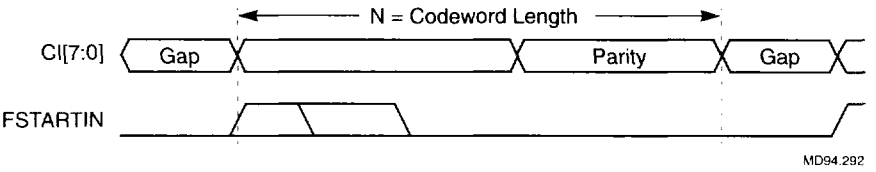
6.1.4 Error Value Generation

The error value generation circuit outputs the bit errors in the incoming message if the number of errors is correctable.

6.2 Decoder Waveforms

Figure 6.3 shows the relation of data in a codeword to the FSTARTIN signal. Channel output is byte parallel or bit serial and contains the corrected channel, parity, and — if desired — the uncorrected GAP data, as shown in Figure 6.3.

Figure 6.3
Decoder CI[7:0] and FSTARTIN

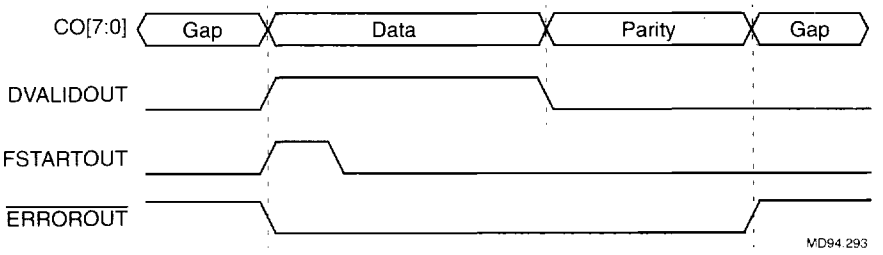


New data is valid on the output in cycles in which DVALIDOUT is HIGH, as shown in Figure 6.4. DVALIDOUT is not asserted during the propagated parity and gap bytes, but $\overline{\text{ERROROUT}}$ goes LOW for both data and parity bytes when an uncorrectable error is detected.

FSTARTOUT is asserted during the first bit of the first symbol of every frame, except when in PLL mode with parallel data out. Then FSTARTOUT is asserted during the first symbol of every frame. A gap is not required in the frame structure, and gap data is not affected by the decoding process.

Note: Gap data must be an integer multiple of eight clock cycles.

Figure 6.4
CO[7:0], $\overline{\text{DVALIDOUT}}$, and $\overline{\text{ERROROUT}}$



6.3 Check Bytes

The number of check bytes generated by the encoder or used by each decoder are shown in Table 6.1

Table 6.1
Check Bytes per Codeword

Encoder	Check Bytes (CB)	Decoders	Check Bytes (CB)
L64711	2 to 32	L64712	2 to 10
		L64713	2 to 20
		L64714	2 to 32

Together, the family of encoder and decoder chips are designed for systems with transfer rates up to 50 Mbits/s. They are ideally suited to transmit digital television and radio signals over microwave or cable. Other applications with similar channel characteristics and data rates are also

possible. Since the digital TV and radio markets are cost sensitive, the ECC chips from LSI Logic are optimized for low-cost integration into embedded systems. In addition, the LSI Logic chips allow direct connection to LSI Logic's MPEG video and audio digital decoders in bit serial mode.

6.4 Codeword Length

In the L64712, L64713, and L64714 decoders, the codeword length is programmable up to 255 bytes. Minimum codeword length is determined by the number of check bytes (CB) programmed into the encoder. The minimum codeword length (N *min*) is determined by the following formula:

$$\left(\frac{(CB)^2}{8} + \frac{CB}{2} + 6\right) \text{to the largest integer.}$$

6.5 Decoder Latency

Input and output channel data may be either bit serial or byte (symbol) parallel. The maximum channel rate is 50 Mbits/s. When decoder input is parallel, latency in data clock cycles is determined by the following formula:

$$\left\lfloor \frac{16N + (CB)^2 + 4CB + 73}{8} \right\rfloor \times 8 + 5$$

When decoder input is serial, latency in data clock cycles is determined by a slightly revised formula, as follows:

$$\left\lfloor \frac{16N + (CB)^2 + 4CB + 73}{8} \right\rfloor \times 8 + 12$$

The value in the inner bracket is truncated to the lowest integer whether the input is parallel or serial.

6.6 PLL and Clock Synthesizer

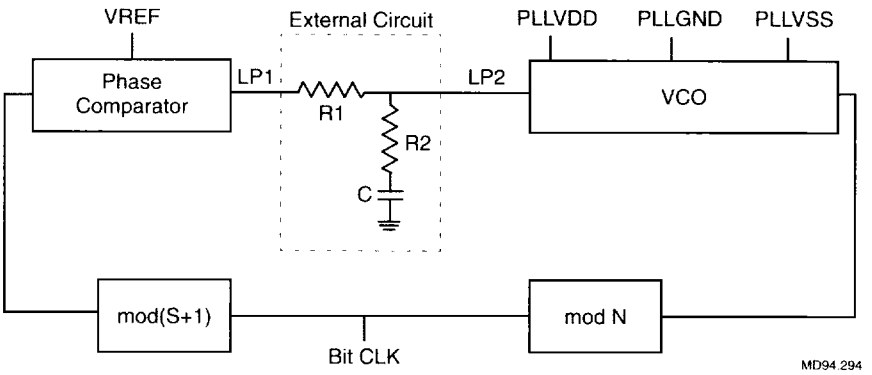
L64712-14 decoders contain a clock synthesizer for deriving the device and bit clocks from a symbol clock operating in the range 156 kHz to 5 MHz. The decoders directly support bit clocks with frequencies that are up to eight times the symbol clock rate. Two registers must be set to derive the appropriate clocks from the symbol clock. The Symbol Division register sets an S counter to the number of bits per symbol. The allowable value of S is 7 which corresponds to 8 bits per symbol. The Clock Synthesis register sets an N counter so that the internal PLL is in its

operating range. Allowable values that the user can select for the N counter are 2, 4, 8, 16, and 32.

Caution: The divide-by-one option in the PLL is currently non-functional. This restricts the operation of the symbol clock to a maximum of 2.5 MHz, or a maximum data rate of 20 MHz in PLL Mode.

A block diagram in Figure 6.5 shows the relation of components in the Phase Locked Loop. Explanatory text follows the figure.

Figure 6.5
PLL Block Diagram



The PLL circuit contains a phase/frequency detector capable of locking on large frequency deviations in a short time. In Figure 6.5, LP1 is the phase detector output to the external R/C circuit. LP2 is the input from the external circuit to the Voltage Controlled Oscillator (VCO). The loop filter components are connected between LP1 and LP2.

The gain of the phase detector is a variable that depends on the charging resistor R1. The suggested values for loop filter components are: R1 = 5 kohms, R2 = 100 ohms, and C = 10 nF. These values allow the proper operation of the synthesizer over its full operating range. A special *sweep feature* has been added to the circuit to ensure proper operation of the synthesizer.

The VCO center frequency is 40 MHz with an operating range of 20 to 65 MHz. VCO gain is approximately 35 MHz/volt with a center frequency control voltage of 2 volts. Special pins for the VCO power and ground are required to isolate the device from the digital power and ground buses. This is suggested to remove the possibility of contributing to the VCO output by digital noise on the power supply lines.

The L64712-14 clock synthesizers operate with a symbol clock in the range 156 kHz to 2.5 MHz. The lower limit of 156 kHz is obtained by setting N = 32 and S = 7, with the VCO running at 40 MHz, and the BITCLK running at 1.25 MHz. The upper limit is obtained by setting N = 2 and S = 7, with the VCO running at 40 MHz and the BITCLK running at 20 MHz.

Note: 1 is not an allowed value for the N counter. To support a BITCLK of 40 MHz, the PLL has to be bypassed.

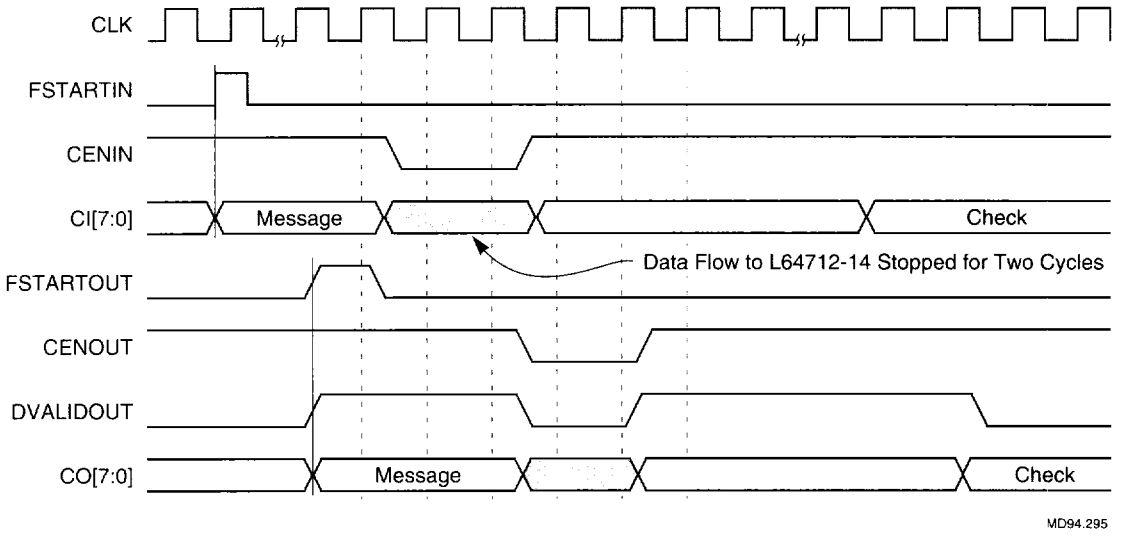
The input symbol clock is taken from the VREF pin. This signal rises in cycles during which CI[7:0] is sampled. If clock synthesis is enabled, VREF and CLK are in the same frequency and phase. The synthesized bit clock is made available as a CLKOUT signal. The symbol clock input may also be connected to an external bit clock and the internal PLL circuit can be bypassed by asserting the CLKSEL pin.

6.7 Clocks and Stopped Processing

The encoder operates from an 8-bit symbol clock or a bit clock. The decoders operate from an 8-bit symbol clock or from a bit clock. A synthesized bit clock output is provided for synchronization with external devices.

The LSI Logic L64712, L64713, and L64714 are able to accept burst or non-continuous data without disrupting the RS decoding process. The clock enable input pin, CENIN, allows the decoder to ignore non-valid data on the input by stopping the decoding function. The decoder can be stopped on a bit clock basis when operating with a data frequency input clock. Figure 6.6 illustrates the use of the CENIN pin in relation to other control and data signals.

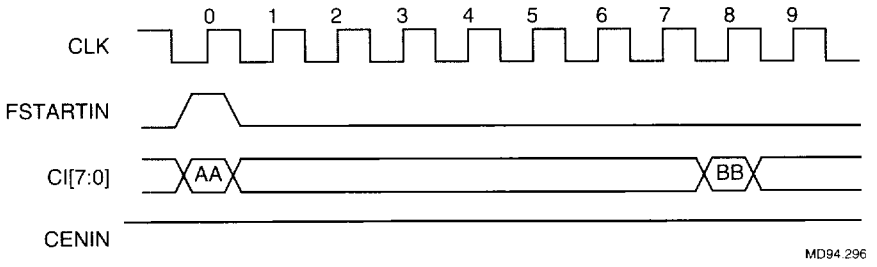
Figure 6.6
Relation of CENIN to Data and Control Signals



Referring to Figure 6.6, the message arrives on CI[7:0]. Processing is interrupted when CENIN is asserted LOW. As long as DVALIDOUT is asserted LOW, external devices ignore CO[7:0] data. The message is continued when DVALIDOUT returns HIGH. Because the DVALIDOUT output tells the next receiving device when the message is valid, burst data can be transferred between devices without additional buffering.

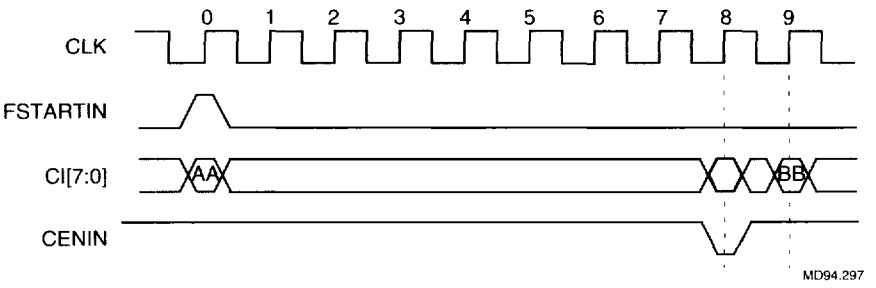
The following example and illustration shows CENIN behavior. When in normal operating mode, data on the CI[7:0] pins is clocked every eight clock cycles. Figure 6.7 illustrates normal operation with CENIN HIGH at all times.

Figure 6.7
CENIN During Normal Operation



If, however, it is determined that a non-valid data bit got through and corrupted the CI bus, that data cycle can be skipped completely by asserting $\overline{\text{CENIN}}$ for one cycle. Correct data is then clocked onto the bus in the next cycle, as shown in Figure 6.8.

Figure 6.8
CENIN Skipping Data Cycle



Note that in PLL mode, CENIN should change on byte boundaries only. To skip a non-valid byte, the user must deassert CENIN LOW for one full system-clock cycle (eight internal bit-clock cycles).