TC35667FTG-006
TC35667FSG-006
Bluetooth® LE Single IC

Rev 2.2

Contents

1. General Description

1.1. Product Concept

TC35667FTG-006 and TC35667FSG-006 (Later omitted TC35667.) is compliant with 2.4 GHz wireless communication Bluetooth® V4.1 low energy standard. With RF analog part and Baseband digital part built-in, TC35667 provides Bluetooth® HCI (Host Control Interface) functions and Bluetooth low energy GATT profile functions defined in Bluetooth® specifications. Connected with external host processors, TC35667 realizes easy development of Bluetooth® Low Energy applications

1.2. Features

- Compliant with Bluetooth® Ver4.1 low energy
  - Built-in Bluetooth® Baseband
  - Built-in Bluetooth® RF analog
  - Built-in ARM7TDMI-S™ core
  - On-chip mask ROM for Bluetooth® program (320 KB)
  - On-chip work RAM for Bluetooth® Baseband process (96 KB)
  - On-chip RAM for application program storing (32 KB)
  - Supports patch program loader function
- General Purpose IO (16 ports)
- General Purpose Serial Interfaces
  - SPI interface (1 ch assigned to a General Purpose IO)
  - I^2C interface (1 ch assigned to a General Purpose IO)
- Host CPU Interface
  - UART interface (9600 bps to 921.6 kbps, 2 channels - RTSX/CTSX are shared with TX2/RX2 and GPIOs)
- Wake-up Interface (1 ch assigned to a General Purpose IO)
  - Wake-up input function from sleep and deep sleep
- PWM Interface (3 ch assigned to General Purpose IOs)
- Reference Clock Input (26 MHz)
  - Built-in oscillator for crystal oscillator connection
- Sleep Clock Input (32.768 kHz)
  - External oscillator input supported
  - Built-in oscillator for crystal oscillator connection
- Sleep and Deep Sleep Functions
- Built-in DCDC converter and LDO
  - Wide range of input power supply voltages supported (1.8 to 3.6 V, low battery voltage detection, > 2.0 V required to start up.)
- Built-in general purpose ADC
  - External analog inputs assigned to GPIOs (3 ch assigned to General Purpose IOs)
  - Internal VDD monitoring (1 ch, connected inside)
- Package**:**
  - TC35667FTG-006**:** P-VQFN40-0606-0.50-001 [40 pin, 6 x 6 mm, 0.5 mm pitch, 0.9 mm thickness]
  - TC35667FSG-006**:** P-VQFN40-0505-0.40-002 [40 pin, 5 x 5 mm, 0.4 mm pitch, 0.9 mm thickness]

2. Pin Function

2.1. Pin Assignment (Top View)

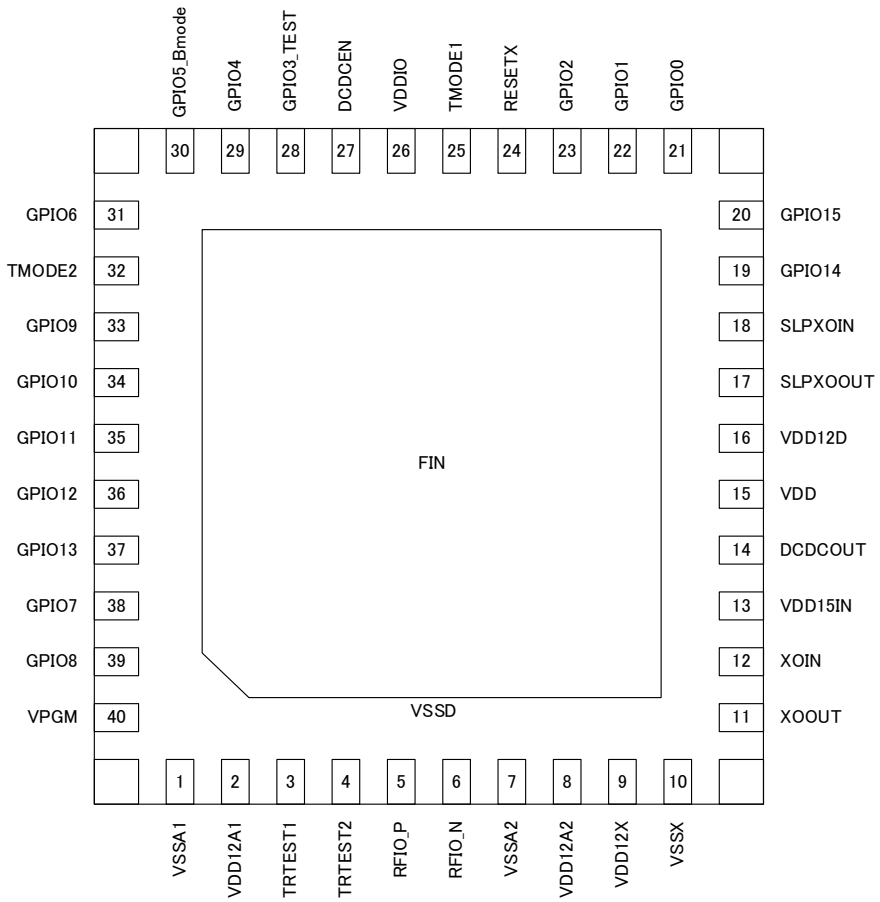


Figure 2-1 Pin Assignment (Top View)

2.2. Pin Function Descriptions

Table 2-1 shows attributes, input/output states for operating modes and descriptions for pin functions. Table 2-4 shows descriptions about power supply pins.

Table 2-1 Pin Functions

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
Reset interface				
RESETX	24	VDDIO IN Schmitt trigger	—	Hardware reset input pin. System initialization signal whose low level indicates reset.
Mode setting				
DCDCEN	27	VDDIO IN Schmitt trigger	IN	DCDC enable pin. High level: internal DCDC is ON Low level: internal DCDC is OFF
Reference clock interface				
XOIN	12	VDD12X IN OSC	IN	Reference clock input pin. A feedback resistor is built between XOIN and XOOUT. Please use oscillator with 26 MHz and < 50 ppm accuracy and connect an output resistor and a capacitor that match the used oscillator.
XOOUT	11	VDD12X OUT OSC	OUT	Reference clock output (feedback) pin. A feedback resistor is built between XOIN and XOOUT. Please connect an output resistor and a capacitor that match the used oscillator.
SLPXOIN	18	VDDIO IN OSC	IN	Sleep clock input pin from oscillator. Please use an oscillator with 32.768 kHz and < 500 ppm accuracy. A feedback resistor is built between SLPXOIN and SLPXOOUT. Connect an output resistor and a capacitor that match the used oscillator. When the oscillator is not used, this pin should be connected to the GND.
SLPXOOUT	17	VDDIO IN/OUT OSC	IN	Sleep clock output pin from oscillator. A feedback resistor is built between SLPXOIN and SLPXOUT. Connect a capacitor that matches the used oscillator. When a sleep clock is supplied from outside, it can be input through this pin. When a sleep clock is not used, this pin should be connected to the GND.

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
RF interface				
RFIO_P RFIO_N	5 6	VDD12A IN/OUT Analog	Hi-Z	RF differential I/O pins. Chapter 6 shows the external connection example of the balanced or unbalanced circuit and the 50 Ω matching circuit. Refer to the connection example, confirm operations in customer's environment, and adjust the components constant. The wiring between 50 Ω matching circuit and an antenna should be 50 Ω transmission line as much as possible for the balanced or unbalanced circuit. For details, refer to the hardware application note of this product.
General purpose I/O port				
GPIO0	21	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Hi-Z	General purpose I/O pin 0. During reset, this pin is input-disabled. Right after reset release, this pin is input-disabled with pull-up resistor off. After reset release, firmware configures the pin function as wake up or general purpose IO. For sleep and deep sleep modes, by software setting and external input, wake up function can be selected, which activates the chip operation. When not used, this pin should be pulled down to the ground with 100 kΩ resistor.
GPIO1	22	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Hi-Z	General purpose I/O pin 1. During reset, this pin is input-disabled. Right after reset release, this pin is input-disabled with pull-up resistor off. After reset, the firmware configures pull-up/pull-down resistors, and the pin can function as general ADC input 0 or general purpose IO. When not used, this pin should be connected to the GND.
GPIO2	23	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Hi-Z	General purpose I/O pin 2. During reset, this pin is input-disabled. Right after reset release, this pin is input-disabled with pull-up resistor off. After reset, the firmware configures pull-up/pull-down resistors, and the pin can function as general purpose IO, general ADC input 1, or PWM output 0. When not used, this pin should be connected to the GND.

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
GPIO3 _TEST	28	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 3. During reset, this pin is set input-disabled with pull-up resistor on. It becomes IC manufacture test mode in a Low level input during the starting processing after reset release. Since the input level of this pin is checked with Pull-up resistance on, please use it with open or setting to high level. By the start processing of after releasing the reset, this pin is assigned to UART1-TX with no pull resistance. Then, in the case of host program download mode, assignment of UART1-TX is canceled, and Pull-up resistance is set up. This pin configures PULL-UP/DOWN resistance, GPIO input or output, UART1-TX (UART2-TX), or SPI-DOUT by a software process after normal starting. When not used, this pin should be opened.
GPIO4	29	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 4. During reset, this pin is disabled with pull-up resistor on. After reset, since the firmware configures this pin to UART1-RX without pull resistance, an external pull-up is always required in stand-alone mode. In the case of host connection, please do not open or fixed to the Low level at the time of start-up. Then, in the case of host program download mode, assignment of UART1-RX will be canceled, and Pull-up resistance will be set up. This pin configures pull-up/pull-down resistors, and general purpose IO, UART1-RX (UART2-RX), or SPI-DIN by a software process after normal starting. When setting up as UART1-RX (UART2-RX), cautions are required so that the terminal may not be fixed to the Low level. (Please confirm firmware specifications for details.)

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
GPIO5 _Bmode	30	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 5. During reset, this pin is input disabled with pull-up resistor on. High input during power up sequence after reset enables host program download mode. After normal power up sequence with low input after reset, the firmware configures pull-up/ Pull-down resistors and general purpose IO, UART1-RTSX, UART2-TX (UART1-TX), or SPI chip select output pin SCS. If this terminal is always set to the Low level, the current will flow through the internal pull-up resistor. Please remove the pull-up resistor by the setting command after starting by the normal mode as processing which reduces this current. (Please confirm firmware specifications for details.)
GPIO6	31	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 6. During reset, this pin is input disabled with pull-up resistor on. After reset, firmware configures pull-up/pull-down resistors and the pin can function as GPIO, UART clear to send pin UART1-CTSX, UART data receiver pin UART2-RX (UART1-RX), or SPI data clock output pin SCLK. When setting up as UART2-RX (UART1-RX), cautions are required so that the terminal may not be fixed to the Low level. When not used, this pin should be opened.
GPIO7	38	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 7. During reset, this pin is input disabled with pull-up resistor on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO, I2C-SCL pin, or SPI data output pin DOUT. When not used, this pin should be opened.
GPIO8	39	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 8. During reset, this pin is input disabled with pull-up resistor on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO, I2C-SDA pin, or SPI data input pin DIN. When not used, this pin should be opened.
GPIO9	33	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 9. During reset, this pin is input disabled with pull-up resistor on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO, I2C-SCL pin, or PWM output pin PWM1. When not used, this pin should be opened.

Pin name	Pin No	Attribute	Condition	Functional description
		VDD category Direction Type	Default (during reset)	
GPIO10	34	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 10. During reset, this pin is input disabled with pull-up resistor on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO, I2C-SDA pin, or PWM output pin PWM2. When not used, this pin should be opened.
GPIO11	35	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 11. During reset, this pin is input disabled with pull-up resistor on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO. When not used, this pin should be opened.
GPIO12	36	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 12. During reset, this pin is input disabled with pull-up resistor on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO. When not used, this pin should be opened.
GPIO13	37	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 13. During reset, this pin is input disabled with pull-up resistor on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO. When not used, this pin should be opened.
GPIO14	19	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin 14. During reset, this pin is input disabled with pull-up resistor on. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO. When not used, this pin should be opened.
GPIO15	20	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Hi-Z	General purpose I/O pin 15. During reset, this pin is input disabled. Right after reset release, it is input enabled with pull-up resistor off. After reset, the firmware configures pull-up/pull-down resistors and the pin can function as GPIO, or general ADC input pin AIN2. When not used, this pin should be connected to the GND.
IC test interface				
TMODE1 TMODE2	25 32	VDDIO IN Schmitt trigger		Test mode setting pins These pins are used for IC manufacturing test and need to be connected to GND when assembled on a board.
TRTEST1 TRTEST2	3 4	VDD12A IN/OUT Analog		Analog test pins. These pins are used for IC manufacturing test and need to be connected to GND when assembled on a board.

2.3. GPIO function list

GPIO pins can be assigned to UART I/Fs, serial memory I/Fs and etc. by TC35667 firmware or command from external Hosts. Table 2-2 shows available functions for each GPIO pin, and Table 2-3 examples of GPIO function settings.

Table 2-2 Available functions for GPIO

Pin	Analog input	Function 1	Function 2	Function 3	Function 4 (Note1)	Function 5
GPIO0	—	GPIO Digital I/O	Wake Up Input	—	—	—
GPIO1	ADC0 Input	GPIO Digital I/O	—	—	—	—
GPIO2	ADC1 Input	GPIO Digital I/O	PWM0 Output	—	—	—
GPIO3_TEST	—	GPIO Digital I/O	UART1-TX Output	—	SPI-DOUT Output	UART2-TX Output
GPIO4	—	GPIO Digital I/O	UART1-RX Input	—	SPI-DIN Input	UART2-RX Input
GPIO5_Bmode	—	GPIO Digital I/O	UART1-RTSX Output	UART2-TX Output	SPI-SCS Output	UART1-TX Output
GPIO6	—	GPIO Digital I/O	UART1-CTSX Input	UART2-RX Input	SPI-SCLK Output	UART1-RX Input
GPIO7	—	GPIO Digital I/O	—	I2C-SCL Output	SPI-DOUT Output	—
GPIO8	—	GPIO Digital I/O	—	I2C-SDA I/O	SPI-DIN Input	—
GPIO9	—	GPIO Digital I/O	PWM1 Output	I2C-SCL Output	—	—
GPIO10	—	GPIO Digital I/O	PWM2 Output	I2C-SDA I/O	—	—
GPIO11 to 14	—	GPIO Digital I/O	—	—	—	—
GPIO15	ADC2 Input	GPIO Digital I/O	—	—	—	—

Note1: SPI-DOUT and SPI-DIN can be assigned to either combination of GPIO3 and GPIO4, or GPIO7 and GIPO8. Both combination GPIO3 and GPIO4, and GPIO7 and GPIO8 cannot be selected at a time.

Table 2-3 GPIO function list (example)

Pin name	Basic example	Example of UART1 + UART2 + I^2C	Example of SPI + I^2C	Example of UART + SPI + I^2C
GPIO0	WakeUp	WakeUp	WakeUp	WakeUp
GPIO1	ADC- AIN0	ADC- AIN0	ADC- AIN0	ADC- AIN0
GPIO2	ADC-AIN1	ADC-AIN1	ADC-AIN1	PWM0
GPIO3_TEST	UART1-TX	UART1-TX	SPI-DOUT	UART1-TX
GPIO4	UART1-RX	UART1-RX	SPI-DIN	UART1-RX
GPIO5_Bmode	UART1-RTSX	UART2-TX	SPI-SCS	SPI-SCS
GPIO6	UART1-CTSX	UART2-RX	SPI-SCLK	SPI-SCLK
GPIO7	I2C-SCL	I2C-SCL	I2C-SCL	SPI-DOUT
GPIO8	I2C-SDA	I2C-SDA	I2C-SDA	SPI-DIN
GPIO9	PWM1	PWM1	PWM1	I2C-SCL
GPIO10	PWM2	PWM2	PWM2	I2C-SDA
GPIO11 to 14	—	—	—	—
GPIO15	ADC-AIN2	ADC-AIN2	ADC-AIN2	ADC-AIN2

Note**:** There are other functions than the above examples. About the detail of the other functions, refer to TC35667 firmware specification.

2.4. Power Supply Pins

Table 2-4 shows the attributes and descriptions of power supply pins for normal operations.

Table 2-4 Power supply pins

Pin name	Pin number	Attribute Type VDD/GND	Description
VPGM	40	TEST —	Test pin Please connect VPGM to GND.
VDD	15	DCDCIN VDD	Power supply pin for DCDC and sleep circuit. When internal DCDC is not used, this pin needs to be connected to the power supply.
VDDIO	26	Digital VDD	IO power supply. Power supply pin for GPIO.
DCDCOUT	14	DCDCOUT —	DCDC output pin. Connect to VDD15IN pin.
VDD15IN	13	LDOIN VDD	Power supply pin for internal regulator. When DCDCON pin is connected to VDD, this pin needs to be connected to DCDCOUT. When DCDCON pin is connected to GND, this pin needs to be connected to external power supply.
VDD12A1	2	Analog VDD	LDO output 1.2 V is supplied to internal analog circuit. A capacitor of 0.1μF or more at the operating temperature range needs to be connected as the load of the LDO.
VDD12D	16	Digital VDD	LDO output 1.1 V is supplied to internal digital circuit. A capacitor of 0.1μF or more at the operating temperature range needs to be connected as the load of the LDO.
VDD12X	9	Analog VDD	LDO output 1.2 V is supplied to internal OSC circuit. A capacitor of 0.1μF or more at the operating temperature range needs to be connected as the load of the LDO.
VDD12A2	8	Analog VDD	LDO output 1.2 V is supplied to internal analog circuit. A capacitor of 0.1μF or more at the operating temperature range needs to be connected as the load of the LDO.
VSSA1	1	Analog GND	GND pin for analog, this pin needs to be connected to GND.
VSSA2	7	Analog GND	GND pin for analog, this pin needs to be connected to GND.
VSSX	10	Analog GND	GND pin for OSC, this pin needs to be connected to GND.
VSSD	FIN	Digital GND	Die pad ground Fin. Connect the exposed Die Pad to GND because this pad is digital ground as well.

3. System Configuration

3.1. Block Diagram

Figure 3-1 shows block diagram of TC35667.

TC35667 is powered by single voltage between 1.8 V and 3.6 V. However, the voltage more than 2.0 V is required for start-up.

The chip has built-in DCDC and LDO requiring external capacitors.

It uses 26 MHz reference clock and 32.768 kHz sleep clock.

External memory is SPI or I^2C, and host CPU interface is UART.

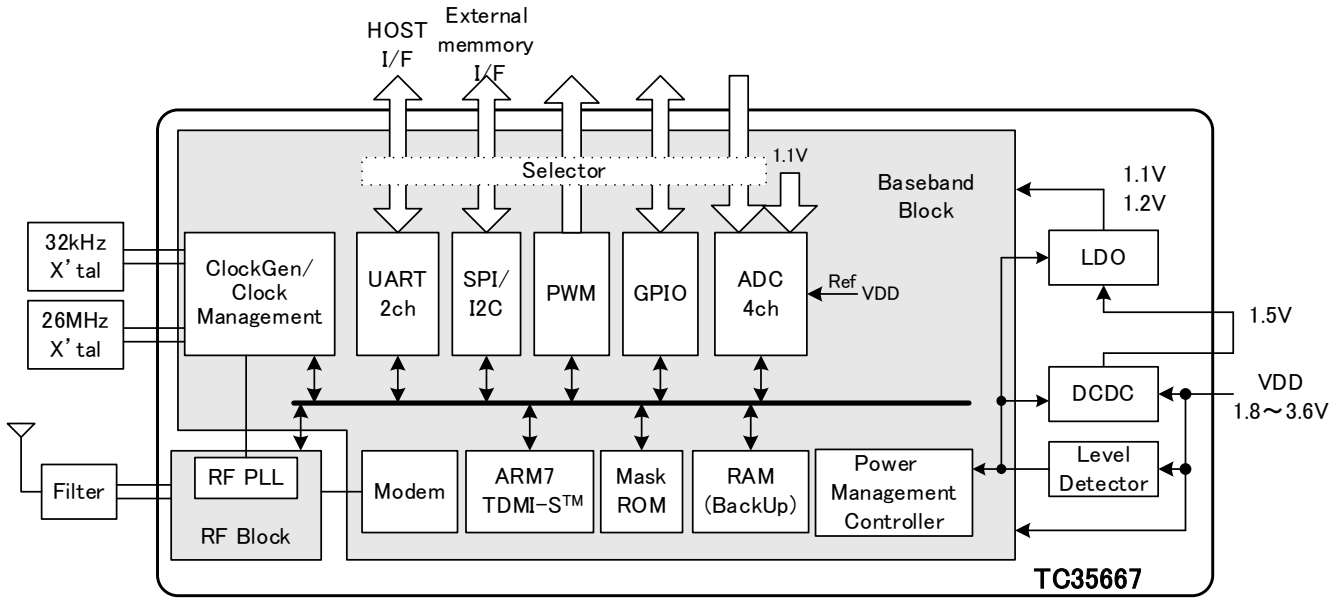


Figure 3-1 It is example of the TC35667 internal block diagram and the peripheral IC connection diagram

4. Hardware Interfaces

4.1. Reset Interface (Power up sequence)

4.1.1. Features

Reset interface has the following features.

- 1.8 to 3.6 V operation
- Level sensitive asynchronous reset (Low level**:** reset)

The reset signal should be at reset status (RESETX = Low) when the power is turned on. After the power supply voltage reaches 2 V or more and becomes stable, disabling the reset signal (RESETX = High) starts the X'tal oscillation after DCDC output has become stable If DCDC is used, or after each LDO output has reached its target voltage. Then, an internal timer releases internal reset 1 ms after the X'tal oscillation has become stable.

Because in the case of soft reset, there are restrictions on the timing, please check the Chapter 4.2.5.1.

4.1.2. Connection Example

Reset signal can be input by an RC time constant circuit or an asynchronous level sensitive reset IC. Figure 4-1 shows a connection example where TC35667 is power-supplied by an RC time constant circuit. Reset signal can be given by RC time constant circuit. Figure 4-2 shows the timings to reset and reset-release for the power supply.

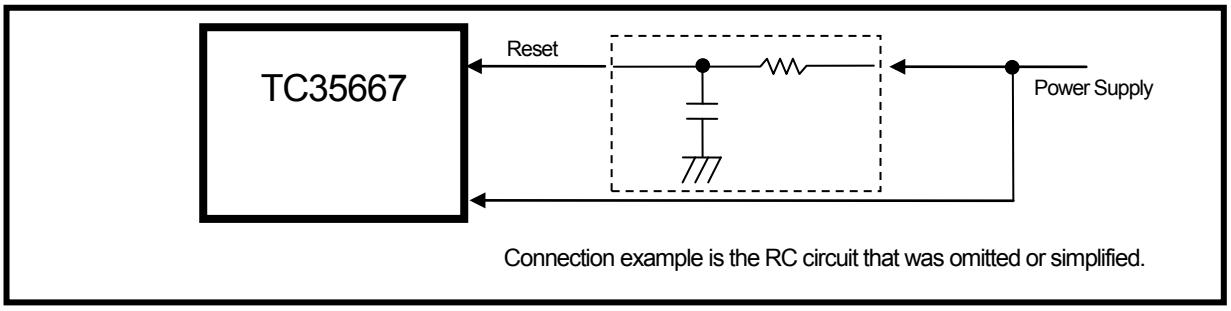


Figure 4-1 Reset signal connection example

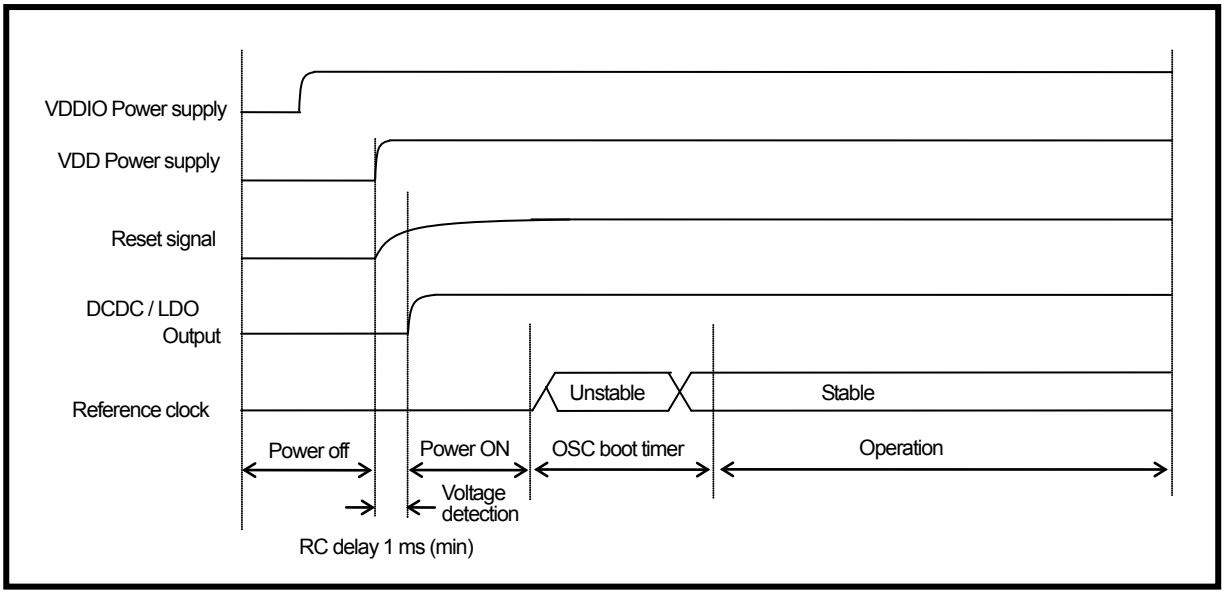


Figure 4-2 Power-on reset release sequence

4.2. UART Interface

4.2.1. Features

TC35667 UART interface has the following features.

- 1.8 to 3.6 V operation
- Full-duplex start-stop synchronization data transfer (RX, TX)
- Two-wire start-stop synchronization data transfer (RX, TX) or four-wire start-stop synchronization data transfer (RX, TX, CTSX, RTSX) are available depending on the settings.
- Start bit field (1 bit), data bit field (8 bits, LSB first), stop bit field (1 bit), no parity bit
- In HCI mode, UART TX/RX pins can be switched by commands (UART2).
- Programmable baud rate**:** 9600 bps to 921.6 kbps (UART2 has only 9600 bps).
- More than 12 characters are inserted between TX messages.
- Error detection (character timeout, overrun error, framing error)
- Host wake up function

TC35667 communicates commands, status, and data with a host CPU through UART interfaces.
The UART interfaces are shared with GPIO pins, and it assigns the GPIO terminal so that it may function as a 2-wire system UART interface in the Boot process after reset release. The UART interfaces can operate at 1.8 to 3.6 V depending on the VDDIO power supply voltage. Because the power supply terminal is shared with UART interface and the other hardware interfaces, UART interface cannot operate at a different voltage of the others.

Table 4-1 UART function overview

	TX/RX pins	Baud rate	Flow control	Host wake up
UART1	GPIO3**:** Transmit data (TX) GPIO4**:** Receive data (RX)	Default**:** 115.2 kbps 9600 bps to 921.6 kbps	**Default: disabled** GPIO5**:** Receive flow control (RTSX) GPIO6**:** Transmit flow control (CTSX)	**Default: disabled** GPIO can be assigned by command Default**:** 10 ms
UART2	**Default: disabled** GPIO5**:** Transmit data (TX) GPIO6**:** Receive data (RX) Note**:** UART2 can be used in HCI mode not with UART1 at a time.	9600 bps	Not supported	Not supported

4.2.2. Connection Example

TC35667 UART can be connected with an UART interface on a host CPU. Figure 4-3 shows an example of two-wire start-stop synchronization data transfer connection with an external host CPU. Figure 4-4 shows the timing when UART is assigned to GPIO and activated.

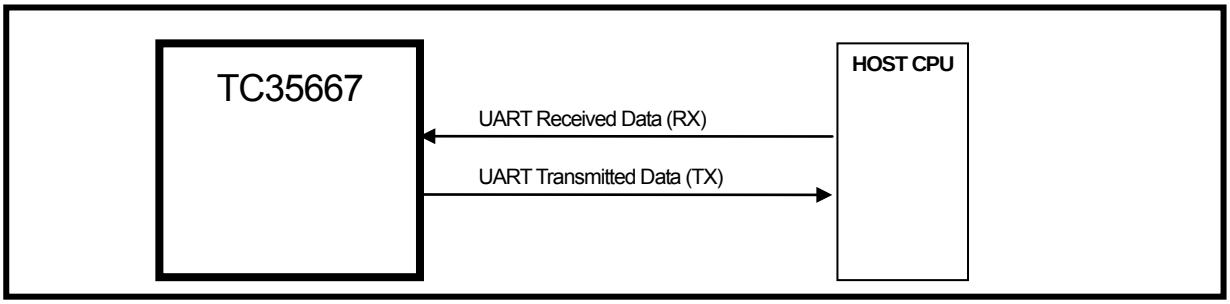


Figure 4-3 UART connection example

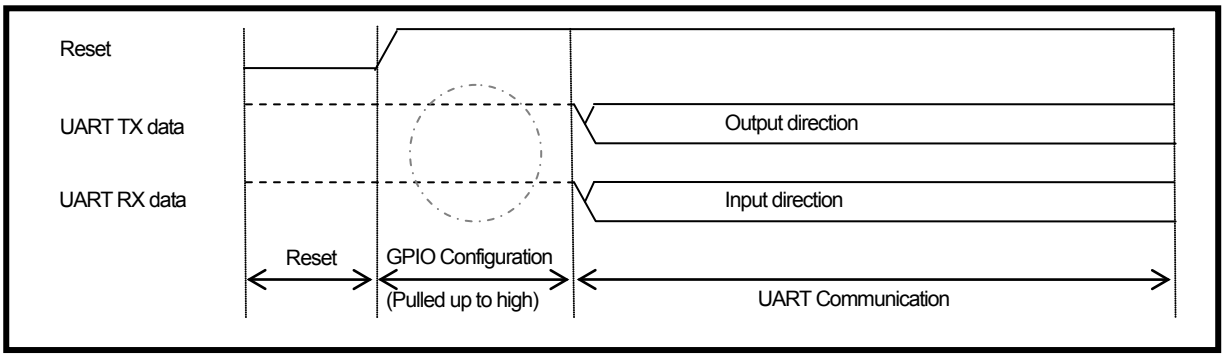


Figure 4-4 Timing for UART function assignment

4.2.3. Frame Format

TC35667 supports the following format:

- Number of data bits: 8 bits (LSB first)
- Parity bit: no parity
- Stop bit: 1 stop bit
- Flow control: RTSX/CTSX

Figure 4-5 shows UART data frame.

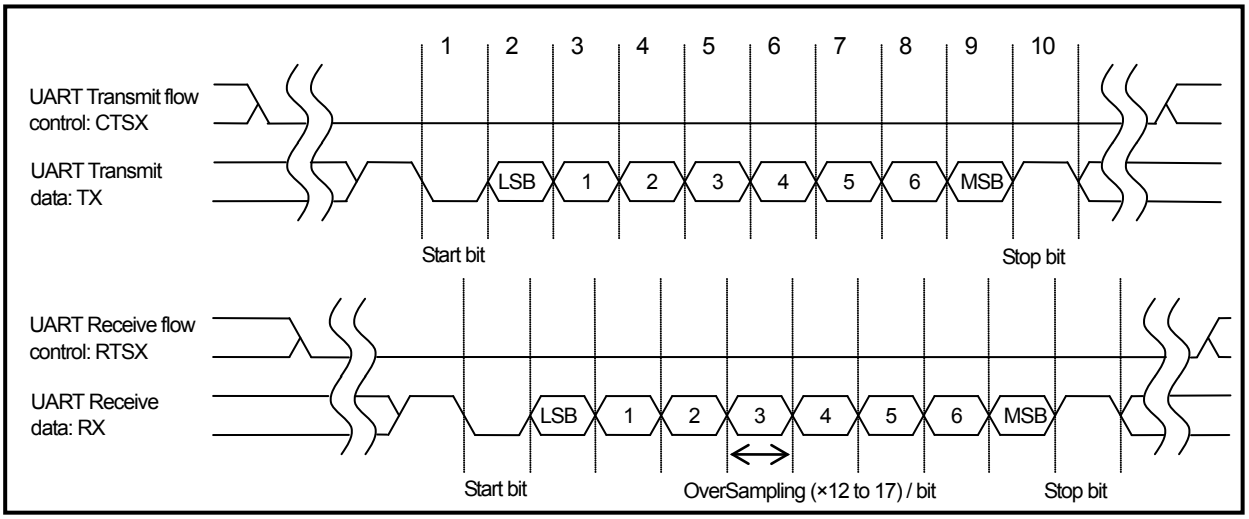


Figure 4-5 UART data frame

4.2.4. Host Wake up Function

TC35667 can wakes up its host CPU before sending UART data to the host CPU. This function is disabled by default, but can be assigned to GPIO by command. Host wake up time can be changed by command (10 ms by default).

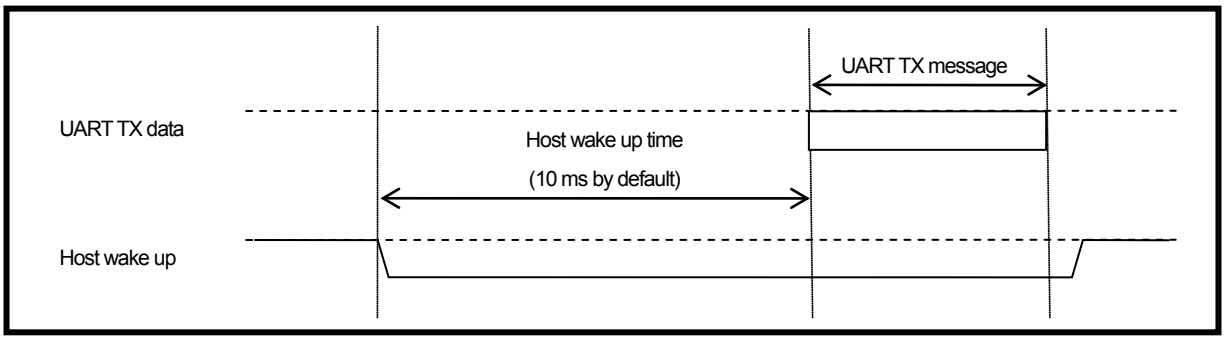


Figure 4-6 Host wake up

4.2.5. HCI mode

In TC35667 HCI mode, UART becomes host interface to enter the HCI command. To test the Bluetooth® wireless performance by connecting the measurement instrument directly to the UART in HCI mode.

4.2.5.1. HCI Reset

To process the following commands successfully, it is needed that at least 150μs waiting from the command complete event after sending a HCI reset command from the host.

4.3. SPI Interface

4.3.1. Features

TC35667 has the following main features for a serial memory interface

- Operation voltage: 1.8 to 3.6 V
- SPI interface
  - Chip select: 1 channel
  - Chip select polarity: Selectable: High-active and Low-active
  - Serial clock master operation: Polarity and phase are adjustable (4 combinations are selectable)
  - Serial clock frequency: 25 kHz to 6.5 MHz
  - Serial data transfer mode: MSB-first, LSB-first

SPI interface can operate at 1.8 to 3.6 V depending on VDDIO, however, because the power supply terminal is shared with SPI interface and the other hardware interfaces, SPI interface cannot operate at a different voltage of the others.

4.3.2. Connection Example

TC35667 SPI interface can be connected to serial EEPROMs and serial Flash-ROMs and has 1 chip select port. Figure 4-7 shows a connection example, where a serial Flash-ROM is connected to TC35667 SPI interface.

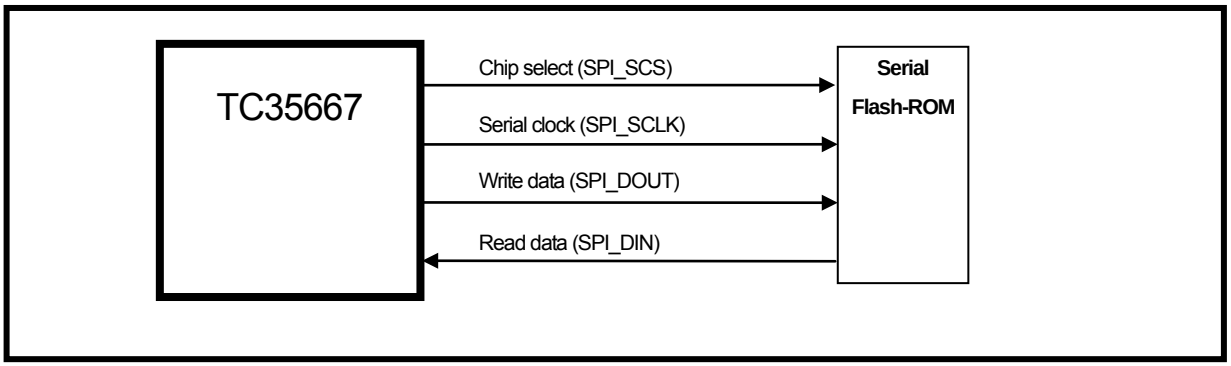


Figure 4-7 Connection example for serial Flash-ROM using SPI interface

4.4. I^2C Interface

4.4.1. Features

TC35667 has the following main features for a serial memory interface.

- Operation voltage: 1.8 to 3.6 V
- I^2C bus interface
  - Operation mode: I^2C bus master
  - Serial clock frequency (I2C_SCL): Standard mode (100 kHz or less), Fast mode (Min 100 kHz to Max 400 kHz)
    Note: When the internal CPU slow clock is operating at 1 MHz, the serial clock frequency is limited to less than 27.8 kHz for standard mode.
  - Output mode: Open-drain output, CMOS output
  - Device address format: 7-bit address (10-bit address is not supported)

I2C interface can operate at 1.8 to 3.6 V depending on VDDIO, however, because the power supply terminal is shared with I2C interface and the other hardware interfaces, I2C interface cannot operate at a different voltage of the others.

4.4.2. Connection Example

Figure 4-8 shows a connection example of a serial EEPROM using I^2C bus interface of the open-drain mode. External pull-up resistors (Rext) are necessary for both serial clock line and serial data line.

Figure 4-9 shows another connection example where I^2C bus is in the CMOS output mode. Only the serial data line needs Rext because this line can be driven by neither TC35667 nor a serial EEPROM.

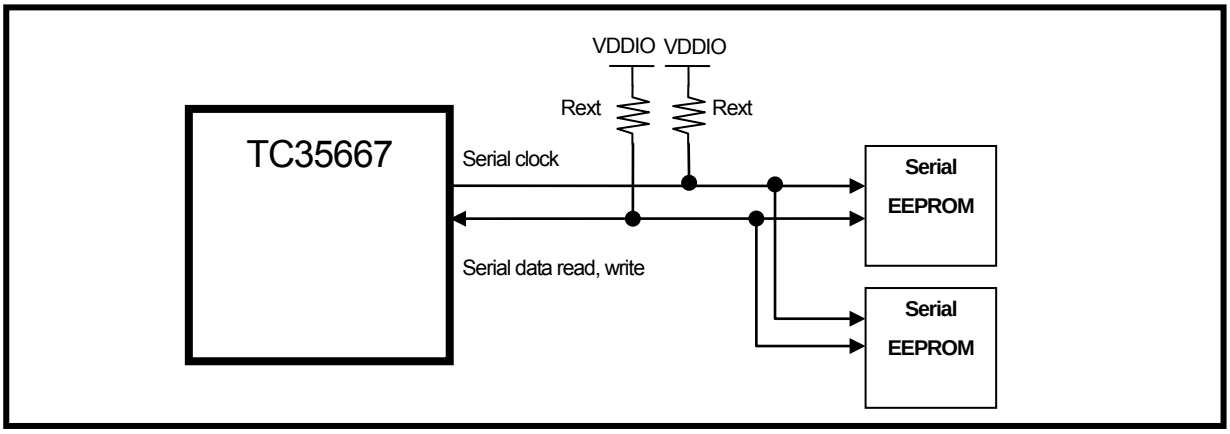


Figure 4-8 Connection example for serial EEPROM with I^2C-bus interface (Open-drain output)

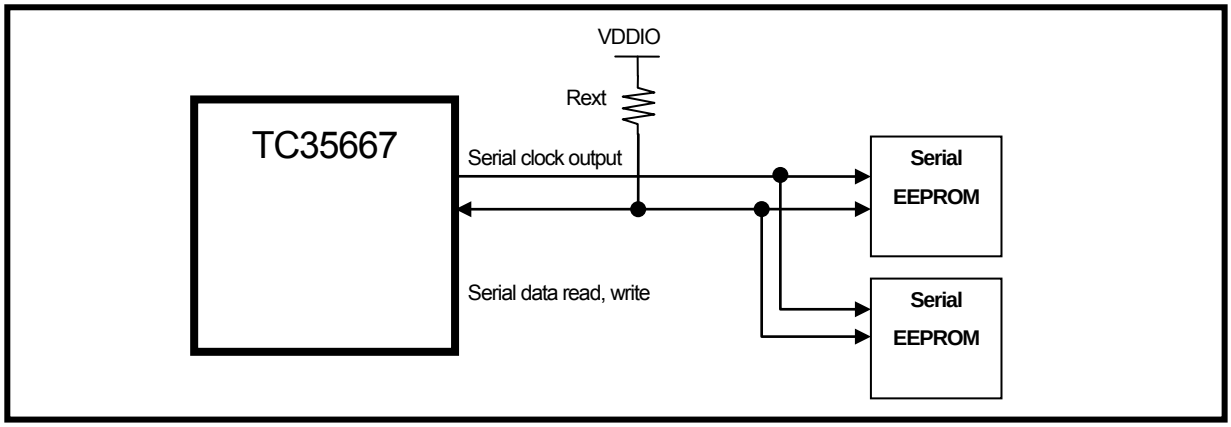


Figure 4-9 Connection example for serial EEPROM with I^2C-bus interface (CMOS output)

4.5. PWM Interface

TC35667 has a PWM interface that can be used for LED, buzzer control, etc.

The PWM interface has the following features.

- Arbitrary pulse generation function
- It can select the source clock from 13 MHz and 32.768 kHz
- It has 12-bit clock division setting up to 1/4096 8 Hz to 16.384 kHz (32.768 kHz), 3.17 kHz to 6.5 MHz (13 MHz)
- It can mask the pulse output on the basis of 50 ms (rhythm function)
- It can generate an interrupt which is synchronized to the rhythm pattern period 1 s.
- It can switch the pulse output to Low / High active
- It can adjust the duty cycle of the pulse output.

4.5.1. Pulse Generation Function

Figure 4-10 shows a brief explanation of the pulse generation. TC35667 can adjust output pulse frequency by changing its cycle. Also it can adjust on/off ratio by changing its duty.

The frequency (Cycle) can be set from 8 Hz to 16.384 kHz for 32.768 kHz clock, and from 3.17 kHz to 6.5 MHz for 13 MHz clock.

The duty can be set from 0 % to 100 %.

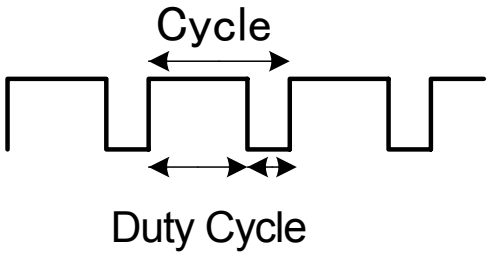


Figure 4-10 PWM pulse generation function

4.5.2. Rhythm Function (Output Masking)

Figure 4-11 shows the brief explanation of PWM rhythm function. In addition to the one for pulse generation, TC35667 has another timer that has 50 ms × 20 = 1 s (rhythm counter). That timer has 20-bit register (pattern register), each bit corresponds to the rhythm counter that counts down in every 50 ms. When the pattern register is zero, the PWM output is masked to zero or one. Using this function, LED or buzzer can be on with 1 s periodical pattern.

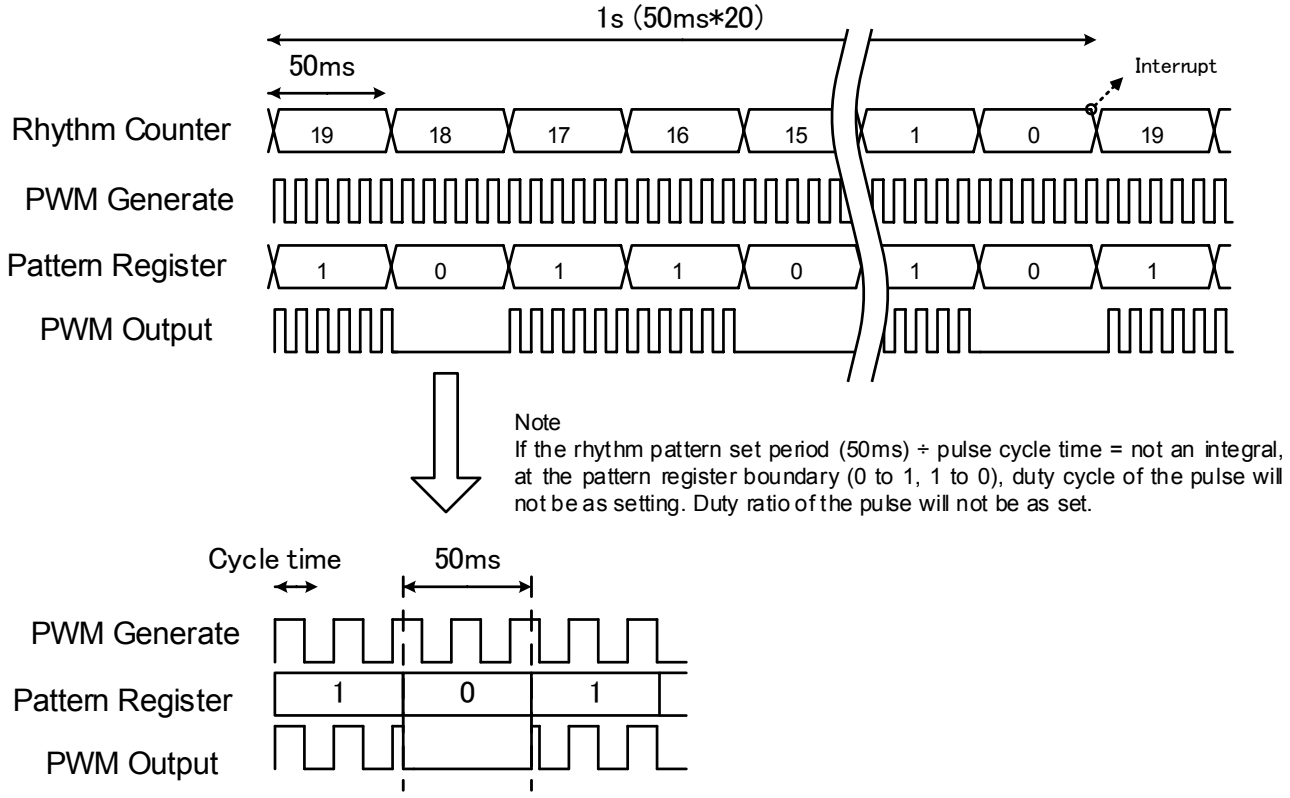


Figure 4-11 PWM Rhythm Function

4.6. ADC

4.6.1. Features

TC35667 has 4 channels of 10-bit ADCs for battery monitoring, analog inputs from external sensors, for example. The ADC has the following features.

- 3 channels for analog inputs (shared with GPIO terminals)
- 1 channels for VDD voltage monitor
  The reference input is connected to VDD, and the analog input is to built-in LDO 1.1 V output.
  Please refer to 4.6.2 for how to calculate VDD absolute value.
- Maximum conversion rate**:** 1 MS/s

4.6.2. Descriptions

The ADC has 10-bit conversion accuracy and can work for input voltages from 0 V to 3.6 V (VDD). It has 4 channels of analog inputs, and the channel 0 is connected to 1.1 V at LDO output, and the channels 1 to 3 are shared with GPIO terminals.
When a battery is used as power source, the reference voltage can slide over time because the battery is connected as reference voltage. AD converted data can be calculated by CPU into voltage values because the channel 0 is supplied with 1.1 V to its input. The following shows the conversion method of the input voltage.

Voltage A at time T can be calculated as follows

(1) LDO output 1.1 V is AD converted. This is X.
(2) Voltage A is AD converted. This is Y
(3) Assuming absolute value of voltage A is Z, 1.1**:**X = Z**:**Y
Z [V] = 1.1 × Y / X Calculation example**:**
Suppose 1.1 V LDO output at ch0 is converted to 0x0188, and measurement target at ch1 0x0134, the absolute voltage at ch1 Z [V] is given by 1.1× 0x0188 / 0x0134 = 1.1 × 392 / 308 = 1.4 [V].

Figure 4-12 shows conceptual of voltage conversion.

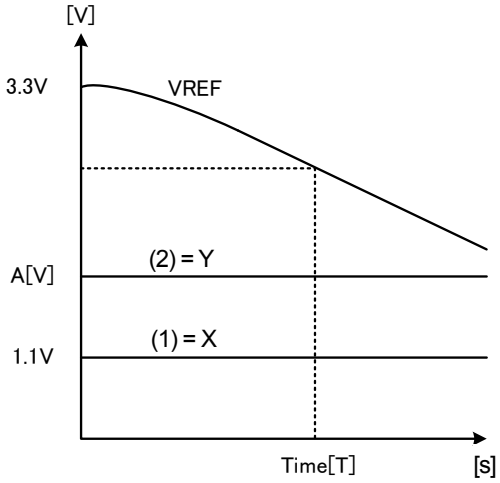


Figure 4-12 Voltage conversion concept

The ADC converts inputs from ch selected by register settings. When a conversion has finished, the CPU detects it by the interrupt or register polling, and then returns the results. The maximum sampling rate depends on software load on the CPU.

4.7. IC Reference Clock Interface

4.7.1. Features

TC35667 has the following features for IC reference clock interface.

- Clock frequency**:** 26 MHz (please adjust the accuracy to < 50 ppm at the temperature in use)

TC35667 doesn't require external feedback resistors because it has an internal feedback resistor between XOIN and XOOUT. Please adjust external capacitors, C_{IN} and C_{OUT}, based on the specification of the used oscillator and PCB layout and assembly.

4.7.2. Connection Example

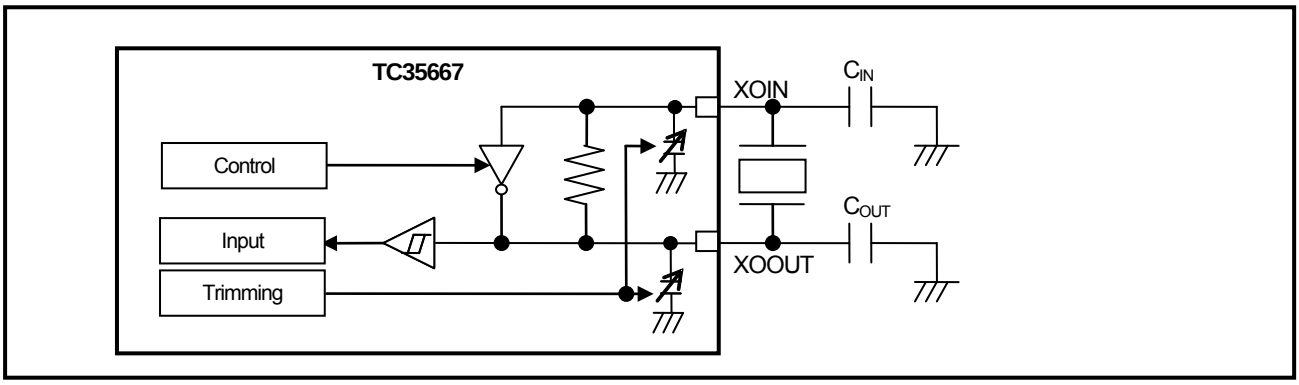


Figure 4-13 Crystal oscillator connection example

4.7.3. Oscillation Frequency Adjust Function

Crystal oscillator circuit has a capacitor array inside, and the oscillator frequency can be trimmed by a register bit value from 0 to 31. Figure 4-14 shows an example of the adjusted frequency measured with our test board using 26 MHz crystal oscillator. This characteristic can vary depending on the crystal oscillator itself, external capacitors, resistors and PCB patterns.

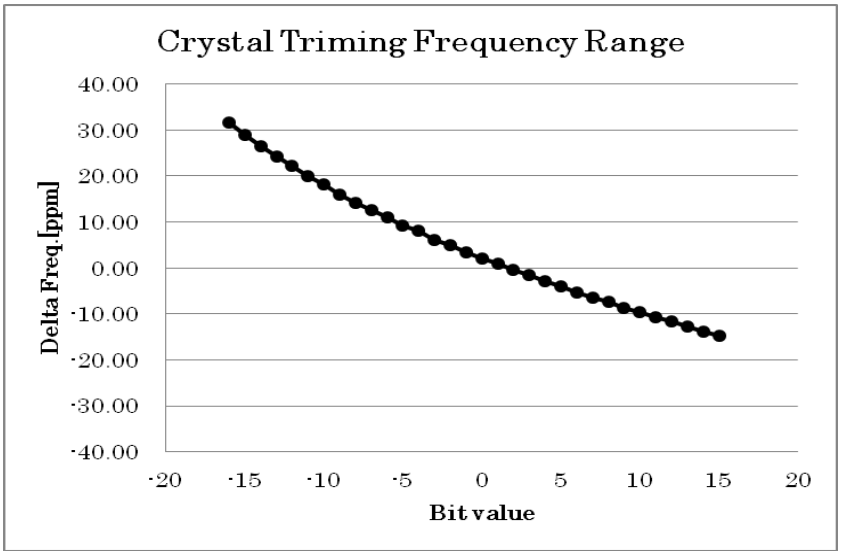


Figure 4-14 Frequency trimming example

4.8. Sleep Clock Interface

TC35667 has the following features for sleep clock interface.

- Crystal oscillator can be connected.
- Clock frequency: 32.768 kHz (please adjust the frequency accuracy to less than or equal to ±500 ppm at the temperature in use.)

Crystal oscillator is connected between SLPXOIN and SLPXOOUT. An external feedback resistor is not required because TC35667 has an internal one between SLPXOIN and SLPXOOUT. Please adjust external capacitors, C_{IN} and C_{OUT}, based on the specification of the used oscillator and PCB layout and assembly. When an external oscillator is connected, connect it to SLPXOOUT and SLPXOIN should be connected to the GND.

4.8.1. Connection Example

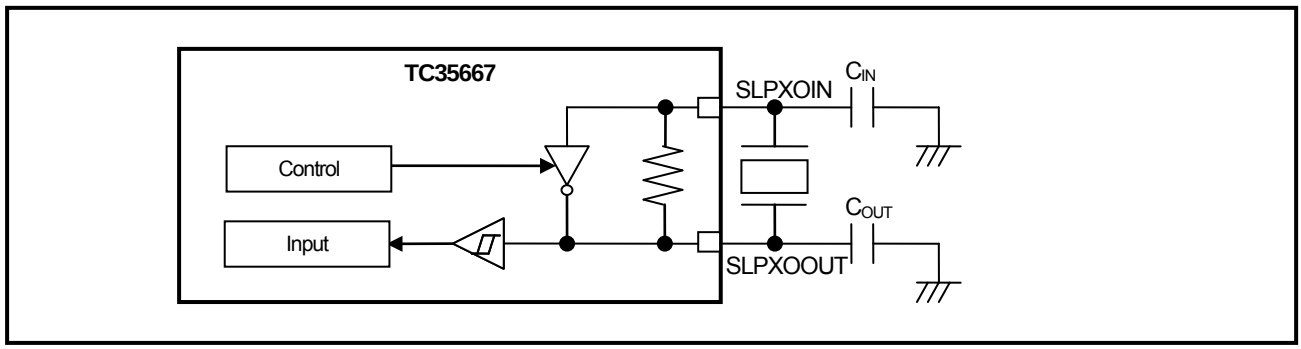


Figure 4-15 Crystal oscillator connection example

4.8.2. Connection Example

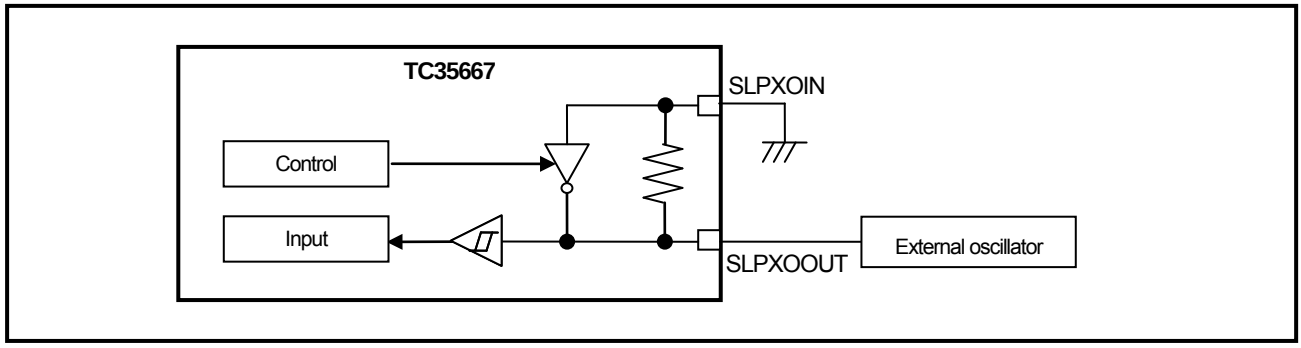


Figure 4-16 External oscillator connection example

5. Electric Characteristics

5.1. Absolute Maximum Ratings

Maximum ratings must not be exceeded even for a moment. Voltages, currents, and temperatures that exceed the maximum ratings can cause break-downs, degradations, and damages not only for ICs but also for other components and boards. Please make sure application designs not to exceed the maximum ratings in any situation.

Table 5-1 Absolute Maximum ratings (VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Items	Symbols	Ratings		Units
		Min	Max	
Power supply	VDD VDDIO (Note1)	-0.3	+3.9	V
Input voltage	VIN	-0.3	VDDIO + 0.3 (Note2)	V
Output voltage	VOUT	-0.3	VDDIO + 0.3 (Note2)	V
Input current	IIN	-10	+10	mA
Input power	RFIO	—	+6	dBm
Storage temperature	Tstg	-40	+125	°C

Note1: Do not connect VDD to GND while VDDIO is powered. Current from VDDIO to VDD through IC may cause damages, break-downs, and degradations.

Note2: Keep VDDIO + 0.3 V < 3.9 V.

5.2. Operating Conditions

TC35667 can operate normally with proven quality under the operating ranges. Any diversion from the operating ranges may cause false operation. Thus, please make sure application design to comply these operating ranges.

Table 5-2 Operating ranges (VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Items	Symbols	Ratings			Units
		Min	Typ.	Max	
Power supply	VDDopr1	1.80	3.00	3.60	V
	VDDopr2	1.96	3.00	3.60	V
	VDDIO	1.80	3.00	3.60	V
	VDD15IN	1.45	1.50	3.60	V
	VDD12A1 / VDD12A2 / VDD12X	—	1.20	—	V
	VDD12D	—	1.10	—	V
RF frequency	Fc	2400.0	—	2483.5	MHz
Clock frequency	Reference clock Fck	25.99870	26.00000	26.00130	MHz
	Sleep clock fslclk	32.751616	32.768000	32.784384	kHz
Ambient temp.	Ta	-40	+25	+85	°C

Note1: VDD pin which has low-voltage detection function is built-in, and it will stop functioning at less than the minimum voltage of VDDopr1. Because the low-voltage detection voltage has a hysteresis so that it will not start again due to the load variation after stopping, it starts at not less than the minimum voltage of the VDDopr2 at the voltage rising time. To make the power supply by an external power source, it must have more than the minimum voltage of the VDDopr2.

Note2: Please refer to other documents for our connection examples.
Please do not input power supply and do connect external capacitors to VDD12A1, VDD12A2, VDD12D, and VDD12X because they are supplied by the internal LDO.

5.3. DC electric characteristics

5.3.1. Current Consumption

This section shows current consumption. When the operating temperature (Ta) is 25°C, and the operation of each power supply terminal is in the recommendation connection state of our company, the current consumption is an average value.

Table 5-3 Current consumption (VDD = VDDIO = 3.0 V, VSSA1 = VSSA2 = VSSD = VSSX = 0 V, DCDCEN = VDD)

Items	Symbols	Conditions	Pins	Ratings			Unit
			(Note)	Min	Typ.	Max	
Digital operation	IDD_{DIG} (Active1)	—	VDD	—	1.8	—	mA
RX	IDD_{RX} (Active2)	—		—	6.3	—	
TX	IDD_{TX} (Active3)	Output Power = -4 dBm		—	6.3	—	
Low power mode With Connection	IDDS1 (Sleep)	26 MHz crystal oscillator disabled 32 kHz external oscillator enabled	VDD	—	10	—	μA
Low power mode Without Connection	IDDS2 (Backup)	26 MHz crystal oscillator disabled 32 kHz external oscillator enabled		—	5	—	
Low power mode Without Connection	IDDS (Deep Sleep)	26 MHz crystal oscillator disabled 32 kHz external oscillator disabled		—	0.05	—	

Note: Current consumption of the IO part will change by the buffer setting.

Table 5-4 shows DC electric characteristics for each terminal under 25°C ambient temperature.

Table 5-4 DC Elecrical Characteristics (VDD = VDDIO = 3.0 V, VSSD = VSSA1 = VSSA2 = VSSX = 0 V)

Item	Symbol	Condition		Measuring Pin (Note 1)	Rating			Unit
		I/F Voltage	Other Condition		Min	Typ.	Max	
High Level Input Voltage	VIH	3.0 V	LVCMOS	VDDIO	0.8×VDDIO	—	—	V
Low Level Input Voltage	VIL	3.0 V	LVCMOS	VDDIO	—	—	0.2×VDDIO	
High Level Input Current	IIH	VDDIO = Input Voltage of each pin	Pull-down Off	VDDIO	-10	—	10	µA
			Pull-down On		10	—	200	
Low Level Input Current	IIL		Pull-up Off		-10	—	10	
			Pull-up On		-200	—	-10	
High Level Output Voltage	VOH	3.0 V	IOH = 1 mA	VDDIO	VDDIO - 0.6	—	—	V
Low Level Output Voltage	VOL	3.0 V	IOL = 1 mA	VDDIO	—	—	0.4	V
External 32 kHz Clock Input level (Note2)	VIH SLPCLK	3.0 V	—	SLPXOOUT	0.8×VDDIO	—	—	V
	VIL SLPCLK	3.0 V	—	SLPXOOUT	—	—	0.2×VDDIO	V

Note1: Please refer to Table 2-4 for power supply line for each pin. It shows the power supply system of each functional pin.

Note2: External oscillator is used for this case instead of crystal oscillator.

5.4. Built-in Regulator Characteristics

Table 5-5 Built-in regulator characteristics (VDD = 1.8 to 3.6 V, VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Item	Symbol	Pin names and conditions	Ratings			Units
			Min	Typ.	Max	
Output voltages	Vout1	DCDCOUT	1.45	1.50	1.60	V
	Vout2	VDD12A1 / VDD12A2 /VDD12X	1.10	1.20	1.30	V
	Vout3	VDD12D	0.70	1.10	1.30	V

5.5. ADC Characteristics

Table 5-6 ADC characteristics (VDD = 1.8 to 3.6 V, VSSA1 = VSSA2 = VSSD = VSSX = 0 V)

Item	Symbol	Condition	Ratings			Unit
			Min	Typ.	Max	
Analog reference voltage	VREFH	—	1.8	3.0	3.6	V
Analog input voltage	VAIN	—	VSSD	—	VREFH	V

5.6. RF Characteristics

The following conditions are applicable unless otherwise specified.

- Ta = 25°C
- VDD = 3.0 V, DCDCEN = VDD
- fx'tal = 26 MHz (Frequency accuracy is adjusted to ±2 ppm at normal temperature)
- PAOUT= 0 dBm

Table 5-7, Table 5-8 shows RF receiving characteristics and RF transmitting characteristics based on Bluetooth® Core Spec. V4.1 low energy. About the characteristics data here, some are design value, not measured value.

Table 5-7 RF Characteristic

Test Item	Packet	bit	ch.	Condition	Spec.			Unit
					Min	Typ.	Max	
Output Power	37 octets	PRBS9	0, 12, 19, 39	peak	—	—	Pavg+ 3 dB	dBm
				average	—	0	—	
In-band Spurious Emissions	37 octets	PRBS9	0, 12, 19, 39	-5 MHz	—	-60	-30	dBm
				-4 MHz	—	-60	-30	
				-3 MHz	—	-57	-30	
				-2 MHz	—	-50	-20	
				2 MHz	—	-50	-20	
				3 MHz	—	-57	-30	
				4 MHz	—	-60	-30	
				5 MHz	—	-60	-30	
Modulation Characteristics	37 octets	11110000	0, 12, 19, 39	Δf1avg (11110000)	225	254	275	kHz
		10101010		Δf2max (min-min) (10101010)	185	208	—	
		—		Δf2avg /Δf1avg	0.80	0.90	—	Ratio
Carrier frequency offset (CFO)	37 octets	10101010	0, 12, 19, 39	average	—	3	—	kHz
				worst	-150	—	150	
Drift	37 octets	10101010		Absolute maximum	—	10	50	kHz
Drift Rate	37 octets	10101010		Absolute maximum	—	4	20	kHz/50 µs

Table 5-8 RF Characteristics

Test Item	Sub Item	Packet	bit	ch.	Condition	Min	Typ.	Max	Unit
Rx Sensitivity	—	37 octets	—	0, 3, 12, 19	PER = 30.8 % at 1500 packets with dirty	—	-92	—	dBm
C/I Performance	PER = 30.8 % at 1500 packets with dirty	37 octets	D wave: PRBS9 U wave: GFSK PRBS15	0, 2, 12, 19, 37, 39	<= -6 MHz	—	-36	—	dB
					-5 MHz	—	-36	—	
					-4 MHz	—	-36	—	
					-3 MHz	—	-36	—	
					-2 MHz	—	-27.5	—	
					-1 MHz	—	5.5	—	
					0 MHz	—	11	—	
					1 MHz	—	5.5	—	
					2 MHz	—	-27.5	—	
					3 MHz	—	-34	—	
					4 MHz	—	-25	—	
					5 MHz	—	-18	—	
					6 MHz	—	-25	—	
					=> 7 MHz	—	-38	—	
Blocking Performance	—	37 octets	D wave: PRBS9 U wave: CW	12	30 - 2000 MHz	-30	—	—	dBm
					2003 - 2399 MHz	-35	—	—	
					2484 - 2997 MHz	-35	—	—	
					3000 M - 12.75 GHz	-30	—	—	
Intermodulation	1500 packets	37 octets	f1=-50 dBm with un-modulation f2 = -50 dBm with PRBS15	0, 12, 19, 39	-4 MHz	30.8	—	—	%
					+4 MHz				
Max Input	PER	37 octets	PRBS9	0, 12, 19, 39	-10 dBm	30.8	0	—	%
Max Input	PER	37 octets	PRBS9	0, 12, 19, 39	-30 dBm	50	50	65.4	%

Note: Blocking characteristic has a disturbance characteristic more than ±3 MHz, the relief specs of the logo attestation test of Bluetooth® maybe applied. The blocking characteristic measures D wave as 12 ch.

5.7. AC Interface Characteristics

5.7.1. UART Interface

Table 5-9 UART Interface AC characteristics

Symbols	Items	Min	Typ.	Max	Unit
tCLDTDLY	Transmit Data ON from CTSX Low level	192	—	—	ns
tCHDTDLY	Transmit Data OFF from CTSX High level	—	—	2	byte
tRLDTDLY	Received Data ON from RTSX Low level	0	—	—	ns
tRHDTDLY	Received Data OFF from RTSX High level	—	—	8	byte

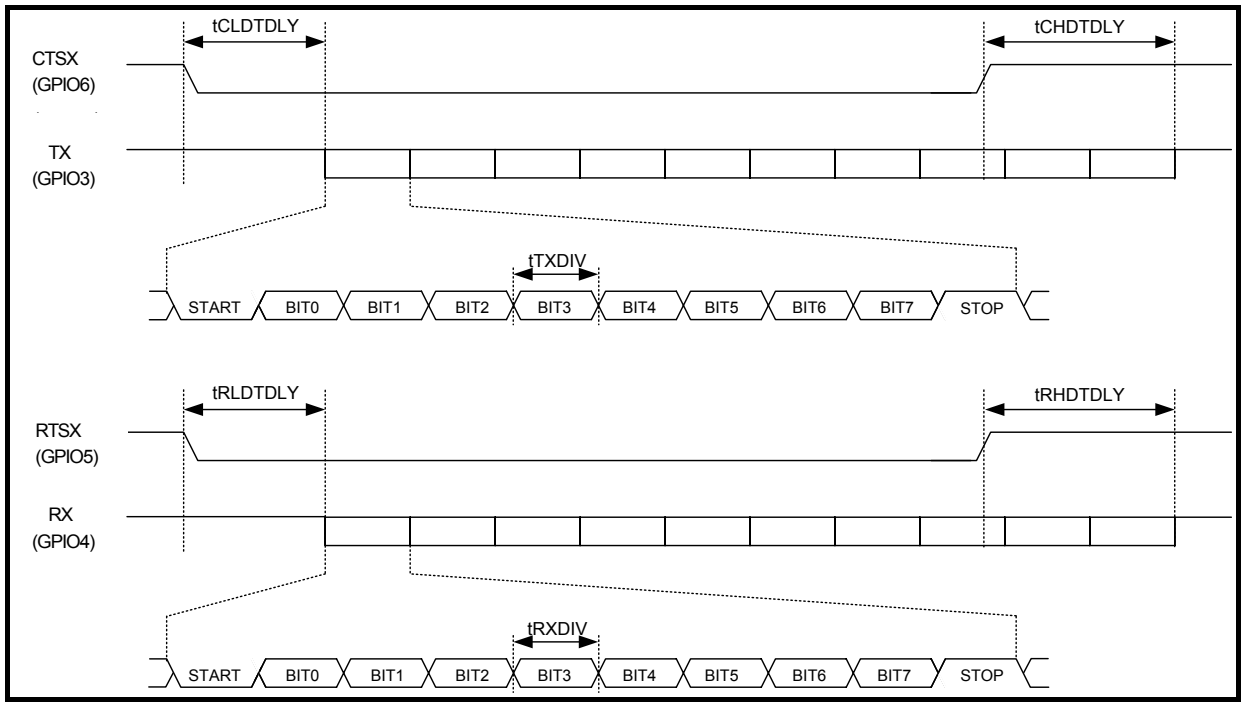


Figure 5-1 UART Interface Timing Diagram

5.7.2. I²C Interface

5.7.2.1. Normal Mode

Table 5-10 I²C Interface Normal mode AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	250	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Data validity period	—	—	3450	ns
tACKVD	ACK validity period	—	—	3450	ns
tSTAS	Restart condition set-up time	4700	—	—	ns
tSTAH	Restart condition hold time	4000	—	—	ns
tSTOS	Stop condition set-up time	4000	—	—	ns
tBUF	Bus open period from stop condition to start condition	4700	—	—	ns
tr	Rise up time	—	—	1000	ns
tf	Fall down time	—	—	300	ns
tHIGH	Serial clock period of High	4000	—	—	ns
tLOW	Serial clock period of Low	4700	—	—	ns
Cb	Bus load capacitance	—	—	400	pF

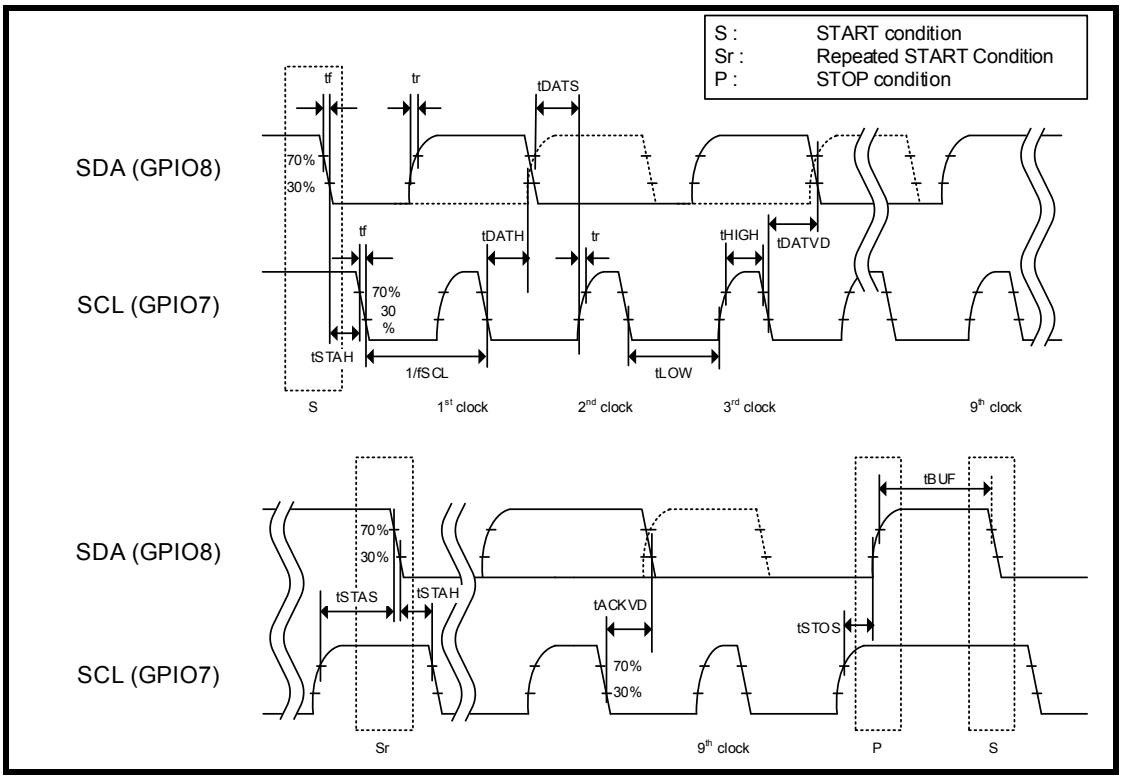


Figure 5-2 I²C Interface Normal mode Timing diagram

5.7.2.2. Fast mode

Table 5-11 I²C Interface Fast mode AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	100	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Data validity period	—	—	900	ns
tACKVD	ACK validity period	—	—	900	ns
tSTAS	Restart condition set-up time	600	—	—	ns
tSTAH	Restart condition hold time	600	—	—	ns
tSTOS	Stop condition set-up time	600	—	—	ns
tBUF	Bus open period from stop condition to start condition	1300	—	—	ns
tr	Rise up time	20 + 0.1Cb	—	300	ns
tf	Fall down time	20 + 0.1Cb	—	300	ns
tSP	Spike pulse width that can be removed	0	—	50	ns
tHIGH	Serial clock period of High	—	1423	—	ns
tLOW	Serial clock period of Low	—	1423	—	ns
Cb	Bus load capacitance	—	—	400	pF

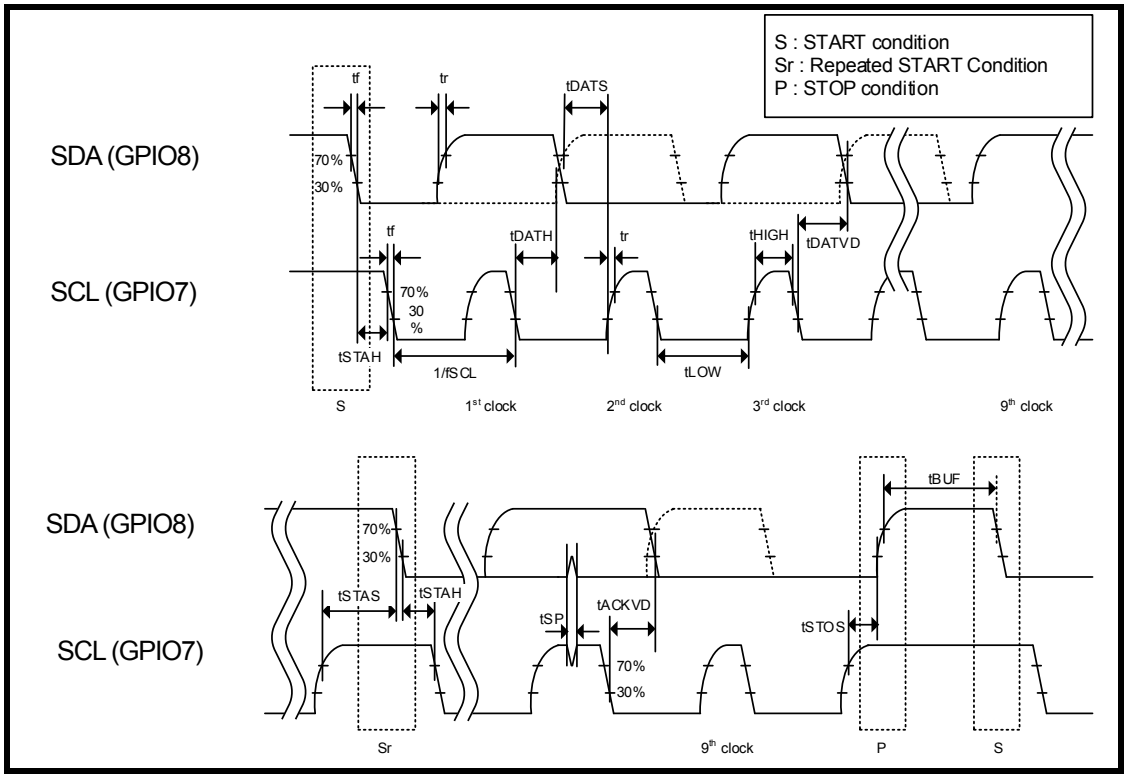


Figure 5-3 I²C Interface Fast mode Timing diagram

5.7.3. SPI Interface

Table 5-12 SPI Interface

Symbols	Items	Min	Typ.	Max	Unit
tSPICLKCYC	SPI clock frequency	154	—	—	ns
tSPICLKHPW	SPI clock high pulse width	77	—	—	ns
tSPICLKLPW	SPI clock low pulse width	77	—	—	ns
tSPICSS	SPI chip select setup time	38	—	—	ns
tSPICSH	SPI chip select hold time	77	—	—	ns
tSPIIW	SPI transfer idle pulse width	54	—	—	ns
tSPIAS	SPI address setup time	38	—	—	ns
tSPIAH	SPI address hold time	77	—	—	ns
tSPIDS	SPI data setup time	38	—	—	ns
tSPIDH	SPI data hold time	77	—	—	ns

Note: SPI Interface operates on the basis of 1/n frequency of half the frequency of ARM7™ core clock (6.5 MHz for 13 MHz core clock)

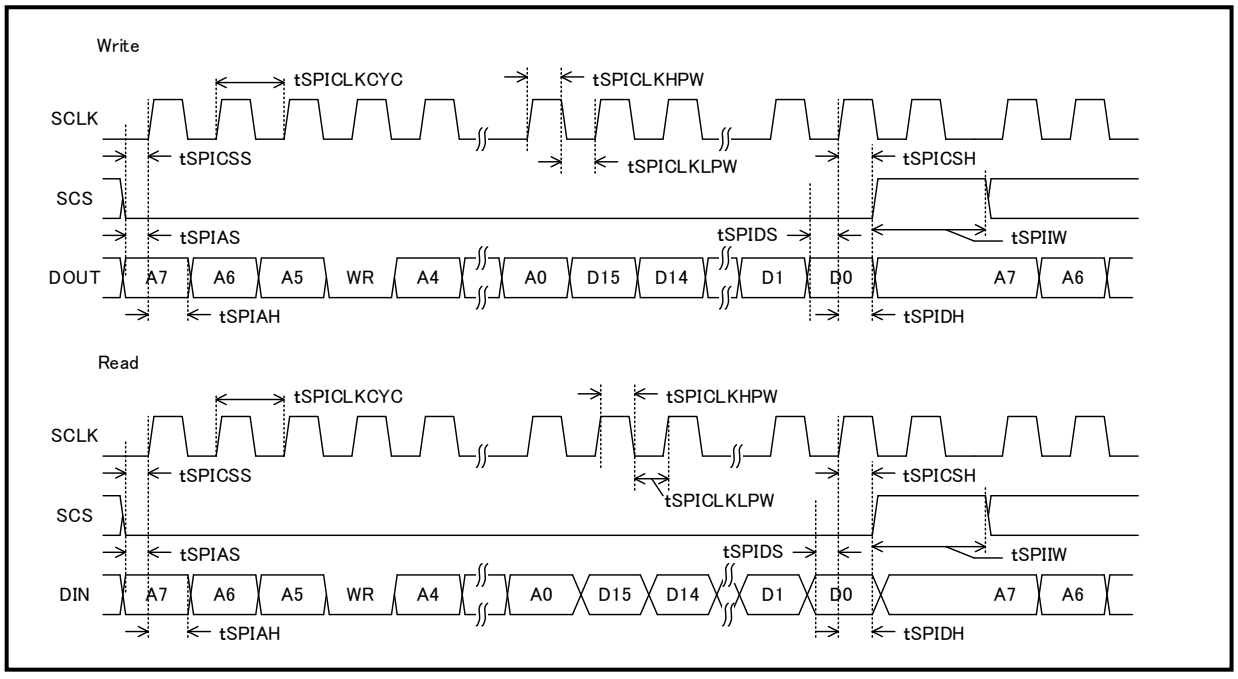


Figure 5-4 SPI Interface timing diagram

6. System Configuration Example

An example of system configuration is shown in the following figures.

6.1. In case of Host CPU connection

- Host interface=UART and 26 MHz Reference Clock= XOSC Connection.
- XOSC (32.768 kHz) of the dotted line enclosure is unnecessary when the external input (HOST common use) is chosen.
- The connection of GPIOs is the example of when they are not in use.

  Note: When the host CPU is connected and GPIO3, 4 are changed to UART2 and SPI, the system becomes uncontrollable because the host CPU cannot send the command.

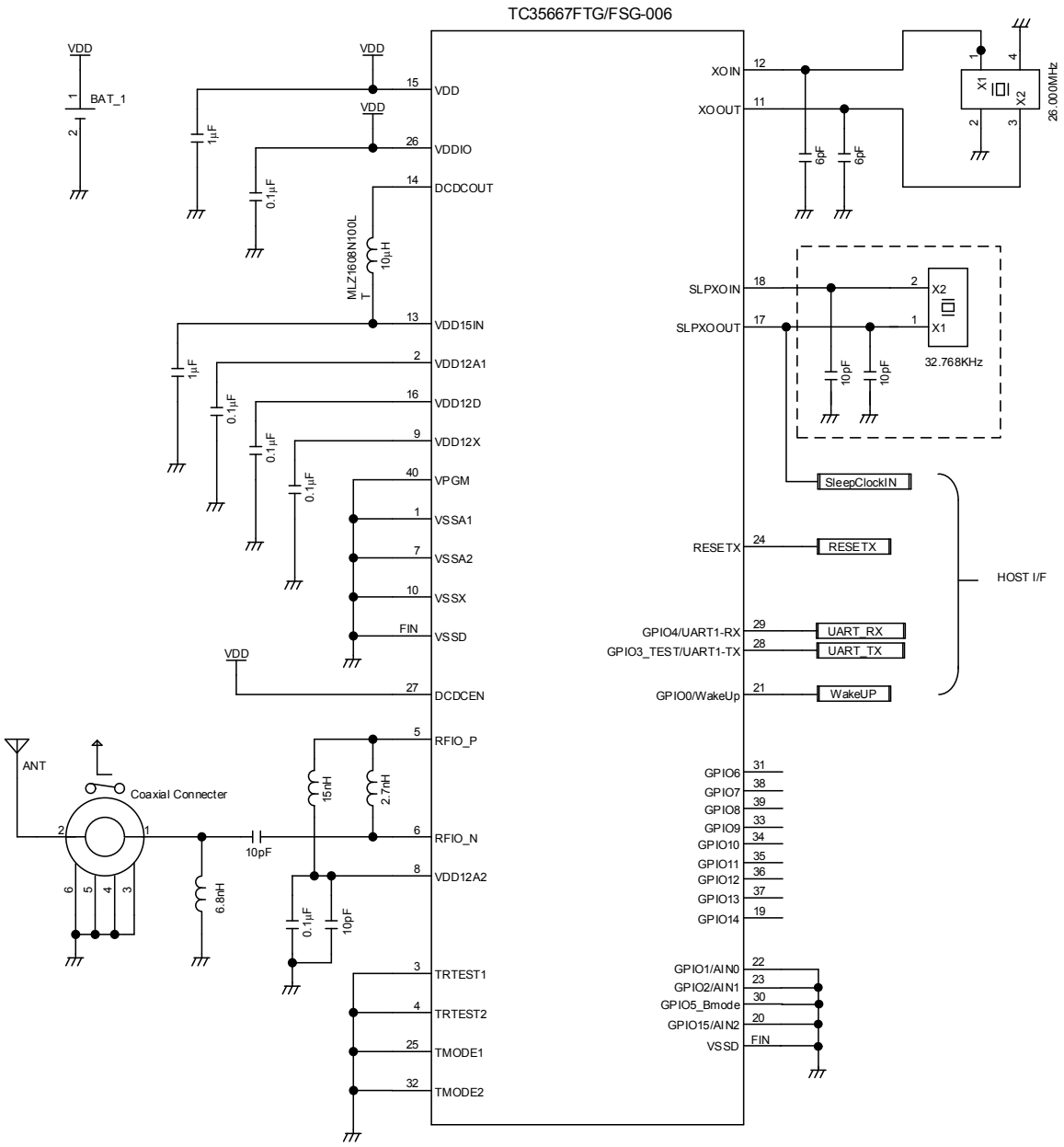


Figure 6-1 Example of TC35667FTG/FSG-006 system configuration (HOST CPU connection)

6.2. In case of Standalone

- XOSC (32.768 kHz) of the dotted line enclosure is unnecessary when the external input (HOST common use) is chosen.
- The connection of GPIOs is the example of when they are not in use.
- To prepare the test for the interface, the GPIO5 in the H (stand-alone) / L (HCI mode) switching control terminal, and then connected to an external control equipment GPIO3,4 as UART1 (command input). Even in this case, please becomes therefore attention an external pull-up is required at all times to GPIO4.

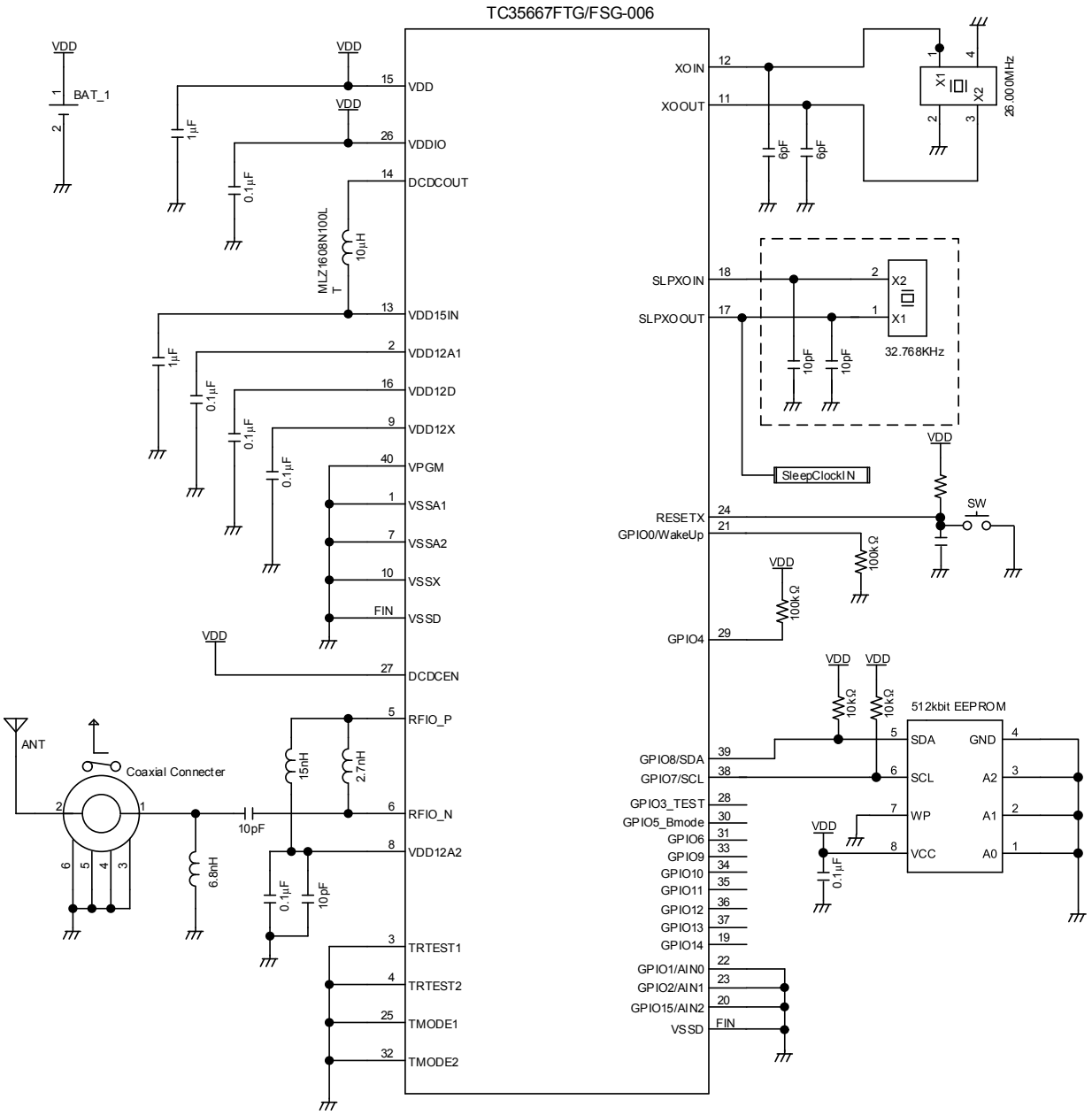
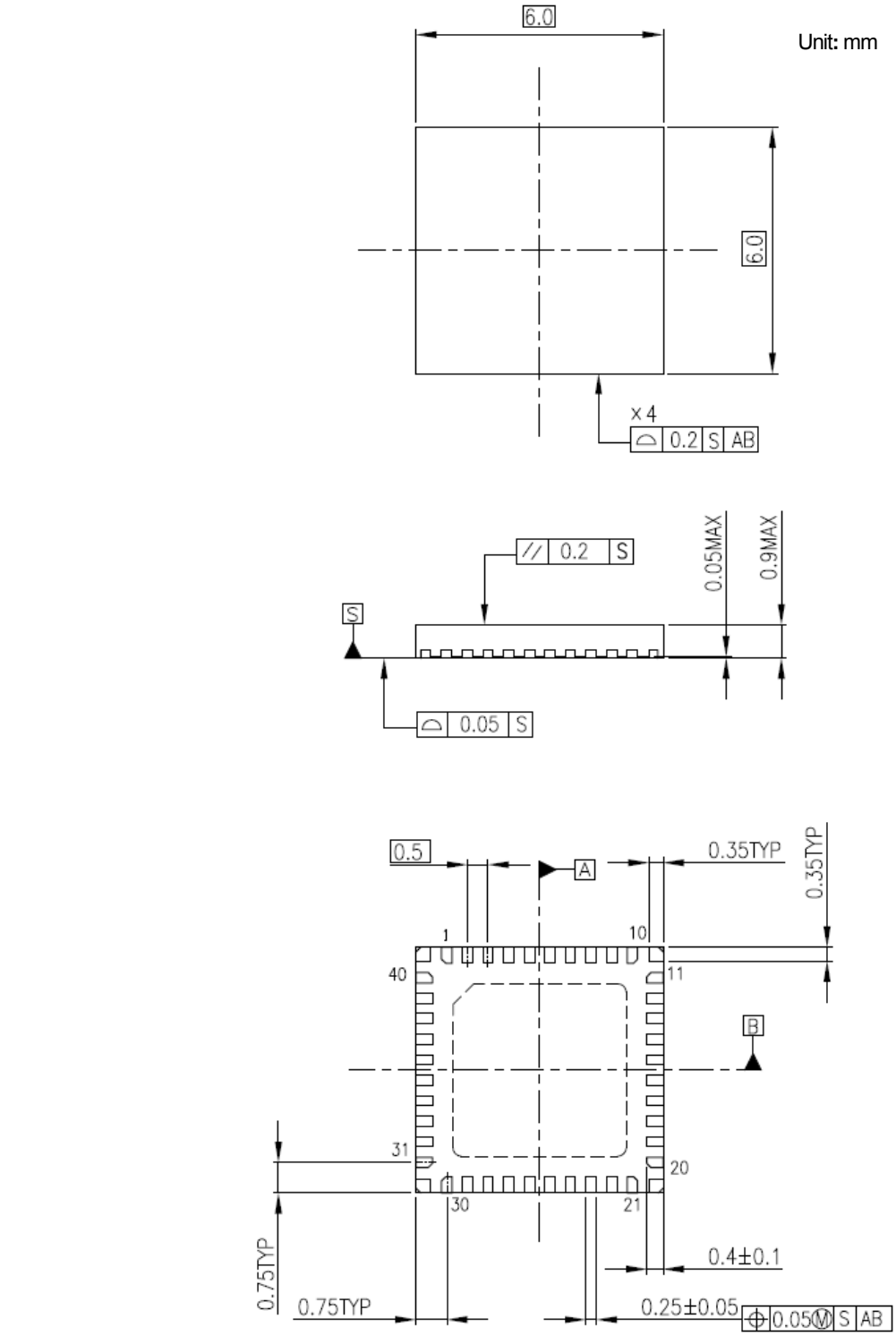


Figure 6-2 Example of TC35667FTG/FSG-006 system configuration (Stand-alone)

7. Package outline

7.1. TC35667FTG-006: Outline dimensional drawing

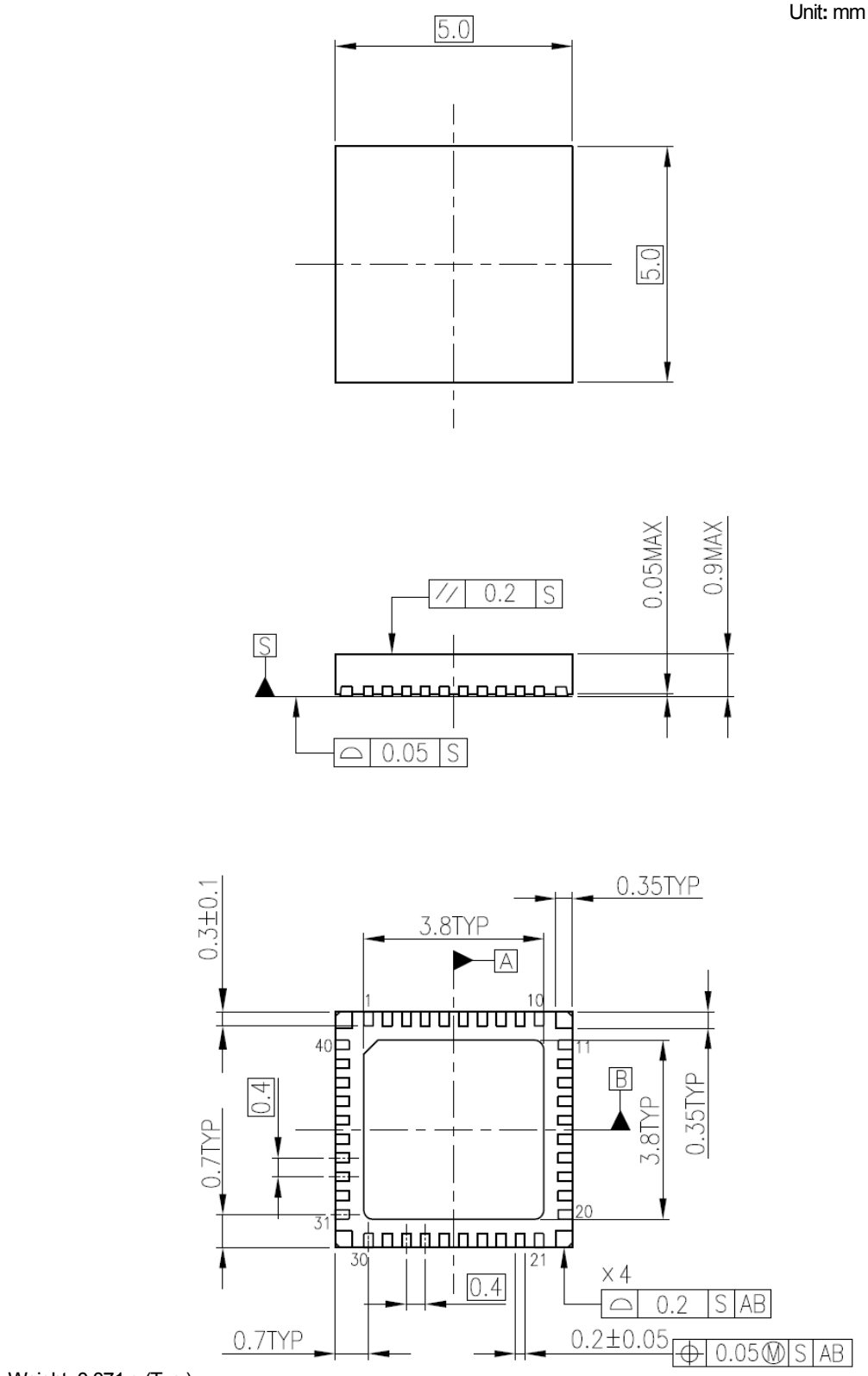


Weight: 0.104 g (Typ.)

Figure 7-1 Package outline (P-VQFN40-0606-0.50-001)

7.2. TC35667FSG-006: Outline dimensional drawing

Unit: mm



Weight: 0.071 g (Typ.)

Figure 7-2 Package outline (P-VQFN40-0505-0.40-002)

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**