MOTOROLA

Programmable Binary Counter

ELECTRICALLY TESTED PER:
MPG54LS718

These monolithic devices are programmable, cascadable, modulo-N-counters. The 54LS716 can be programmed to divide by any number (N) from 0 through 9, the 54LS718 from 0 through 15.

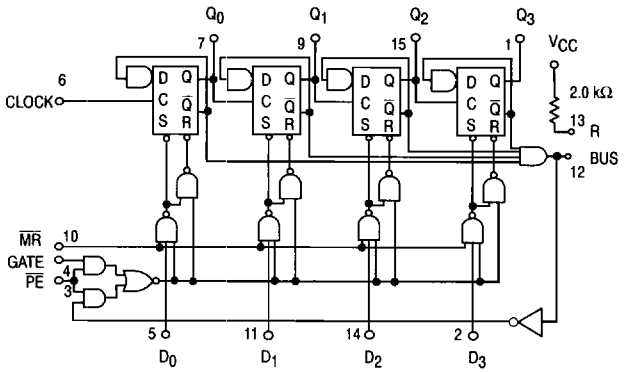
The parallel enable ($\overline{PE}$) input enables the parallel data inputs D_0 through D_3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

Input Loading Factor:
Clock, $\overline{PE}$ = 2
D_0, D_1, D_2, D_3 Gate = 1
$\overline{MR}$ = 4
Output Loading Factor = 8

All Types:
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time:
Clock to Q_3 = 50 ns typ
Clock to Bus = 35 ns typ

LOGIC DIAGRAM



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Military 54LS718

AVAILABLE AS:

1) JAN: N/A
2) SMD: N/A
3) 883: 54LS718/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

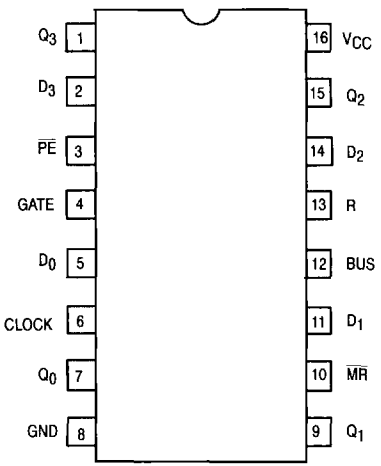
PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
Q_3	1	1	2	V_{CC}
D_3	2	2	3	V_{CC}
$\overline{PE}$	3	3	4	GND
GATE	4	4	5	V_{CC}
D_0	5	5	7	V_{CC}
CLK	6	6	8	V_{CC}
Q_0	7	7	9	V_{CC}
GND	8	8	10	GND
Q_1	9	9	12	V_{CC}
$\overline{MR}$	10	10	13	GND
D_1	11	11	14	V_{CC}
BUS	12	12	15	PN17
R	13	13	17	PN15
D_2	14	14	18	V_{CC}
Q_2	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

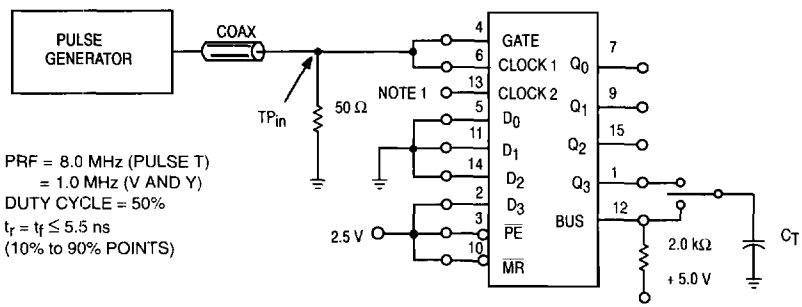
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE				
Count	Outputs			
	Q_3	Q_2	Q_1	Q_0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

CONNECTION DIAGRAM



FUNCTIONAL SWITCHING TIME CIRCUIT



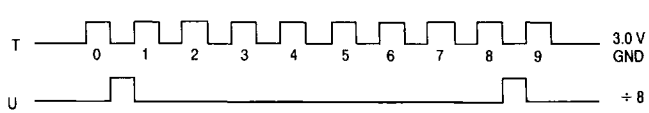
PRF = 8.0 MHz (PULSE T)
= 1.0 MHz (V AND Y)
DUTY CYCLE = 50%
$t_r = t_f \leq 5.5$ ns
(10% to 90% POINTS)

C_T = 50 pF = TOTAL PARASITIC CAPACITANCE WHICH INCLUDES PROBE, WIRING, AND LOAD CAPACITANCE.

NOTE:

1. Counter programmed for ÷ 8 operation, Pin 13 is the resistor pin, and left open.

PRF = 8.0 MHz AT 25°C
PRF = 6.5 MHz AT –55°C AND 125°C



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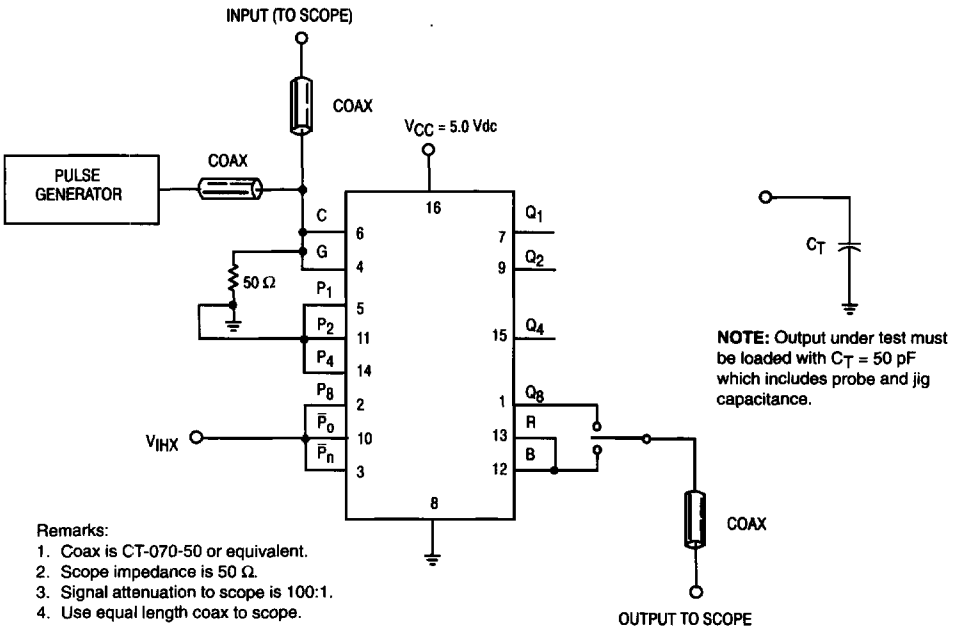
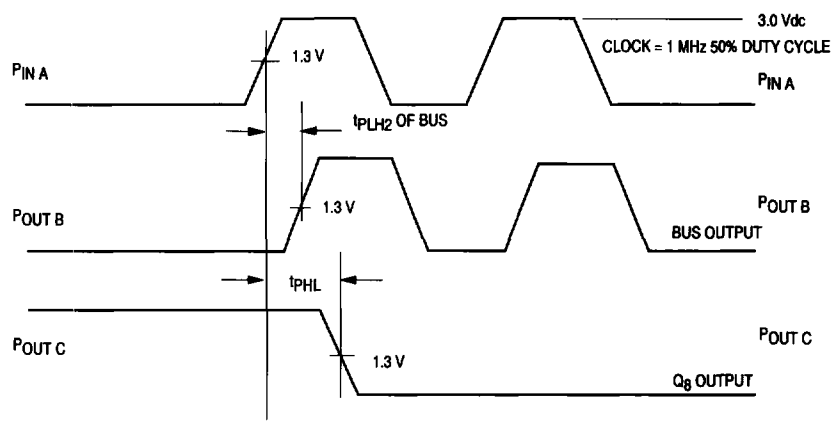
SWITCHING CIRCUIT AND WAVEFORMS

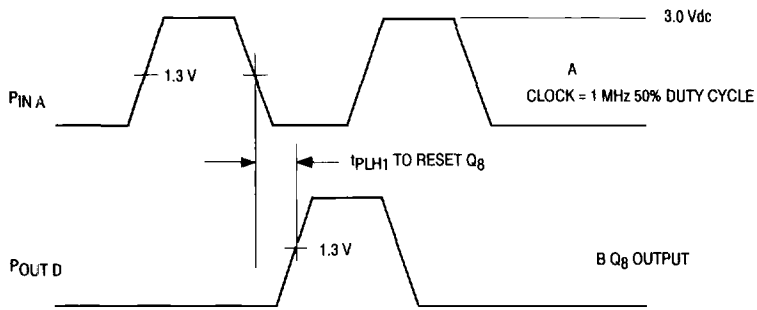


Remarks:
1. Coax is CT-070-50 or equivalent.
2. Scope impedance is 50 Ω.
3. Signal attenuation to scope is 100:1.
4. Use equal length coax to scope.

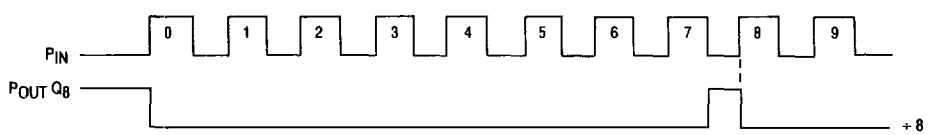
PULSE GENERATOR REQUIREMENTS:
V_{GEN} = 3.0 Vdc, t + = t − ≤ 6.0 ns, PRR = 1 MHz, DUTY CYCLE = 50%.



SWITCHING CIRCUIT WAVEFORM



NOTE:
Check output waveform as shown below prior to measuring propagation delay.



Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V, other inputs are open.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IL} = 0.7 V, V_{IH} = 2.0 V, other inputs are open.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IH}	Logical "1" Input Current		40		40		40	µA	V_{CC} = 5.5 V, $V_{IH(\overline{PE})}$ = 2.7 V, other inputs are open, Gate = GND.
I_{IHH}	Logical "1" Input Current		200		200		200	µA	V_{CC} = 5.5 V, $V_{IHH(\overline{PE})}$ = 5.5 V, other inputs are open, Gate = GND.
I_{IH}	Logical "1" Input Current		80		80		80	µA	V_{CC} = 5.5 V, $V_{IH(\overline{MR})}$ = 2.7 V, other inputs are open, D_0-D_3 = GND.
I_{IHH}	Logical "1" Input Current		400		400		400	µA	V_{CC} = 5.5 V, $V_{IHH(\overline{MR})}$ = 5.5 V, other inputs are open, D_0-D_3 = GND.
I_{IL}	Logical "0" Input Current		− 0.4		− 0.4		− 0.4	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs are open.
I_{IL}	Logical "0" Input Current		− 0.8		− 0.8		− 0.8	µA	V_{CC} = 5.5 V, $V_{IL(\overline{PE})}$ = 0.4 V, other inputs are open, $\overline{MR}$ = 2.7 V.
I_{IL}	Logical "0" Input Current		− 1.6		− 1.6		− 1.6	µA	V_{CC} = 5.5 V, $V_{IL(\overline{MR})}$ = 0.4 V, other inputs are open, D_0-D_3 = 2.7 V.
I_{OS}	Output Short Circuit Current	− 30	− 130	− 30	− 130	−30	− 130	mA	V_{CC} = 5.5 V, V_{IN} = 2.7 V, other inputs are open, $\overline{PE}$ = 0.7 V, V_{OUT} = GND.
I_{CC}	Power Supply Current Off		32		32		32	mA	V_{CC} = 5.5 V, V_{IN} = GND, other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, **(Repeat at)** V_{CC} = 5.5 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay Clock to Q_n		93 78		125 120		125 120	ns	V_{CC} = 5.0 V, C_T = 50 pF, R_L = 50 Ω. V_{CC} = 5.0 V, C_T = 15 pF.
t_{PLH1} t_{PHL1}	Propagation Delay Gate to Q_n		35 35		50 44		50 44	ns	V_{CC} = 5.0 V, C_T = 50 pF, R_L = 50 Ω. V_{CC} = 5.0 V, C_T = 15 pF.
t_{PHL2} t_{PHL2}	Propagation Delay Clock to Bus		80 65		95 90		95 90	ns	V_{CC} = 5.0 V, C_T = 50 pF, R_L = 50 Ω. V_{CC} = 5.0 V, C_T = 15 pF.
f_{tog} f_{tog}	Toggle Frequency	8.0 8.0		6.5 —		6.5 —		MHz	V_{CC} = 5.0 V, C_T = 50 pF, R_L = 50 Ω. V_{CC} = 5.0 V, C_T = 15 pF.

NOTE:
1. The limits specified for C_T = 15 pF is guaranteed but not tested.

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