

MEMORY

CMOS

2 M × 64 BITS

HYPER PAGE MODE DRAM MODULE

MB8502E064AB-60/-70

Buffered, 2 M × 64 BITS Hyper Page Mode DRAM Module, 5 V, 1-bank

## DESCRIPTION

The Fujitsu MB8502E064AB is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eight MB8117805A devices. The MB8502E064AB is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8502E064AB are the same as the MB8117805A which features hyper page mode (EDO) operation. For ease of memory expansion, the MB8502E064AB is offered in an 168-pin Dual In-line Memory Module package (DIMM).

## PRODUCT LINE & FEATURES

| Parameter                  |                | MB8502E064AB-60 | MB8502E064AB-70 |
|----------------------------|----------------|-----------------|-----------------|
| RAS Access Time            |                | 60 ns max.      | 70 ns max.      |
| Random Cycle Time          |                | 104 ns min.     | 124 ns min.     |
| Address Access Time        |                | 35 ns max.      | 40 ns max.      |
| CAS Access Time            |                | 20 ns max.      | 22 ns max.      |
| Hyper Page Mode Cycle Time |                | 25 ns min.      | 30 ns min.      |
| Power Dissipation          | Operating Mode | 6600 mW max.    | 6105 mW max.    |
|                            | Standby Mode   | 440 mW max.     | 440 mW max.     |

- Conformed to 8-Byte DIMM JEDEC standard
- Organization: 2,097,152 words × 64 bits
- Module Size: 1.00" (height) × 5.25" (length) × 0.350" (thick)
- Memory: MB8117805A (2 M × 8, 2 K ref.), 8 pcs
- TI's Input Buffers, 2 pcs
- TI's Input Driver for Buffered PD, 1 pc
- Parallel Presence Detect

- 5.0 V + 10% Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Hyper Page Operation (EDO)
- RAS-only Refresh / CAS-before-RAS Refresh
- Package and Ordering Information:  
168-pin DIMM, order as  
MB8502E064AB-xxDG (DG = Gold Pad)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

# MB8502E064AB-60/-70

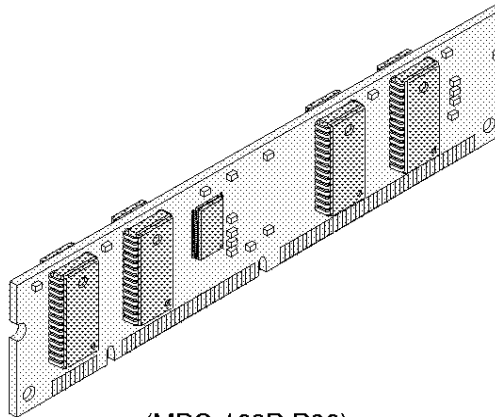
## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter                    | Symbol    | Value        | Unit |
|------------------------------|-----------|--------------|------|
| Supply Voltage               | $V_{CC}$  | -0.5 to +7.0 | V    |
| Input Voltage                | $V_{IN}$  | -0.5 to +7.0 | V    |
| Output Voltage               | $V_{OUT}$ | -0.5 to +7.0 | V    |
| Short Circuit Output Current | $I_{OUT}$ | ±50          | mA   |
| Power Dissipation            | $P_D$     | 10           | W    |
| Storage Temperature          | $T_{STG}$ | -55 to +125  | °C   |

**WARNING:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ■ PACKAGE

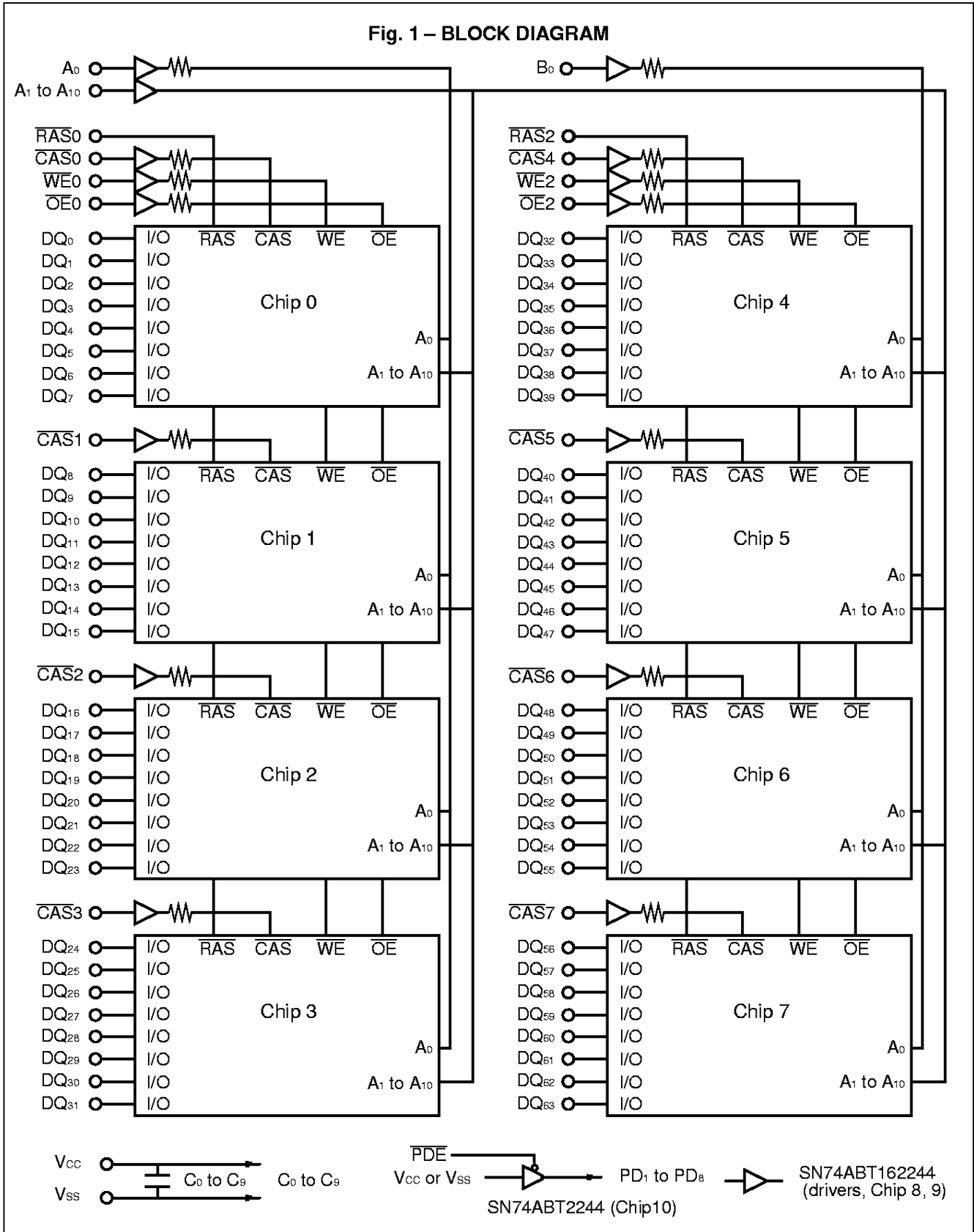
168-pin plastic DIMM (socket type)



(MDS-168P-P06)

# MB8502E064AB-60/-70

Fig. 1 – BLOCK DIAGRAM



# MB8502E064AB-60/-70

## ■ PIN ASSIGNMENTS

| Pin No. | MB8502E064AB             | Pin No. | MB8502E064AB             | Pin No. | MB8502E064AB             | Pin No. | MB8502E064AB             |
|---------|--------------------------|---------|--------------------------|---------|--------------------------|---------|--------------------------|
| 1       | V <sub>SS</sub>          | 43      | V <sub>SS</sub>          | 85      | V <sub>SS</sub>          | 127     | V <sub>SS</sub>          |
| 2       | DQ <sub>0</sub>          | 44      | $\overline{\text{OE}}2$  | 86      | DQ <sub>32</sub>         | 128     | N.C.                     |
| 3       | DQ <sub>1</sub>          | 45      | $\overline{\text{RAS}}2$ | 87      | DQ <sub>33</sub>         | 129     | N.C.                     |
| 4       | DQ <sub>2</sub>          | 46      | $\overline{\text{CAS}}4$ | 88      | DQ <sub>34</sub>         | 130     | $\overline{\text{CAS}}5$ |
| 5       | DQ <sub>3</sub>          | 47      | $\overline{\text{CAS}}6$ | 89      | DQ <sub>35</sub>         | 131     | $\overline{\text{CAS}}7$ |
| 6       | V <sub>CC</sub>          | 48      | $\overline{\text{WE}}2$  | 90      | V <sub>CC</sub>          | 132     | $\overline{\text{PDE}}$  |
| 7       | DQ <sub>4</sub>          | 49      | V <sub>CC</sub>          | 91      | DQ <sub>36</sub>         | 133     | V <sub>CC</sub>          |
| 8       | DQ <sub>5</sub>          | 50      | N.C.                     | 92      | DQ <sub>37</sub>         | 134     | N.C.                     |
| 9       | DQ <sub>6</sub>          | 51      | N.C.                     | 93      | DQ <sub>38</sub>         | 135     | N.C.                     |
| 10      | DQ <sub>7</sub>          | 52      | DQ <sub>16</sub>         | 94      | DQ <sub>39</sub>         | 136     | DQ <sub>48</sub>         |
| 11      | N.C.                     | 53      | DQ <sub>17</sub>         | 95      | N.C.                     | 137     | DQ <sub>49</sub>         |
| 12      | V <sub>SS</sub>          | 54      | V <sub>SS</sub>          | 96      | V <sub>SS</sub>          | 138     | V <sub>SS</sub>          |
| 13      | DQ <sub>8</sub>          | 55      | DQ <sub>18</sub>         | 97      | DQ <sub>40</sub>         | 139     | DQ <sub>50</sub>         |
| 14      | DQ <sub>9</sub>          | 56      | DQ <sub>19</sub>         | 98      | DQ <sub>41</sub>         | 140     | DQ <sub>51</sub>         |
| 15      | DQ <sub>10</sub>         | 57      | DQ <sub>20</sub>         | 99      | DQ <sub>42</sub>         | 141     | DQ <sub>52</sub>         |
| 16      | DQ <sub>11</sub>         | 58      | DQ <sub>21</sub>         | 100     | DQ <sub>43</sub>         | 142     | DQ <sub>53</sub>         |
| 17      | DQ <sub>12</sub>         | 59      | V <sub>CC</sub>          | 101     | DQ <sub>44</sub>         | 143     | V <sub>CC</sub>          |
| 18      | V <sub>CC</sub>          | 60      | DQ <sub>22</sub>         | 102     | V <sub>CC</sub>          | 144     | DQ <sub>54</sub>         |
| 19      | DQ <sub>13</sub>         | 61      | N.C.                     | 103     | DQ <sub>45</sub>         | 145     | N.C.                     |
| 20      | DQ <sub>14</sub>         | 62      | N.C.                     | 104     | DQ <sub>46</sub>         | 146     | N.C.                     |
| 21      | DQ <sub>15</sub>         | 63      | N.C.                     | 105     | DQ <sub>47</sub>         | 147     | N.C.                     |
| 22      | N.C.                     | 64      | N.C.                     | 106     | N.C.                     | 148     | N.C.                     |
| 23      | V <sub>SS</sub>          | 65      | DQ <sub>23</sub>         | 107     | V <sub>SS</sub>          | 149     | DQ <sub>55</sub>         |
| 24      | N.C.                     | 66      | N.C.                     | 108     | N.C.                     | 150     | N.C.                     |
| 25      | N.C.                     | 67      | DQ <sub>24</sub>         | 109     | N.C.                     | 151     | DQ <sub>56</sub>         |
| 26      | V <sub>CC</sub>          | 68      | V <sub>SS</sub>          | 110     | V <sub>CC</sub>          | 152     | V <sub>SS</sub>          |
| 27      | $\overline{\text{WE}}0$  | 69      | DQ <sub>25</sub>         | 111     | N.C.                     | 153     | DQ <sub>57</sub>         |
| 28      | $\overline{\text{CAS}}0$ | 70      | DQ <sub>26</sub>         | 112     | $\overline{\text{CAS}}1$ | 154     | DQ <sub>58</sub>         |
| 29      | $\overline{\text{CAS}}2$ | 71      | DQ <sub>27</sub>         | 113     | $\overline{\text{CAS}}3$ | 155     | DQ <sub>59</sub>         |
| 30      | $\overline{\text{RAS}}0$ | 72      | DQ <sub>28</sub>         | 114     | N.C.                     | 156     | DQ <sub>60</sub>         |
| 31      | $\overline{\text{OE}}0$  | 73      | V <sub>CC</sub>          | 115     | N.C.                     | 157     | V <sub>CC</sub>          |
| 32      | V <sub>SS</sub>          | 74      | DQ <sub>29</sub>         | 116     | V <sub>SS</sub>          | 158     | DQ <sub>61</sub>         |
| 33      | A <sub>0</sub>           | 75      | DQ <sub>30</sub>         | 117     | A <sub>1</sub>           | 159     | DQ <sub>62</sub>         |
| 34      | A <sub>2</sub>           | 76      | DQ <sub>31</sub>         | 118     | A <sub>3</sub>           | 160     | DQ <sub>63</sub>         |
| 35      | A <sub>4</sub>           | 77      | N.C.                     | 119     | A <sub>5</sub>           | 161     | N.C.                     |
| 36      | A <sub>6</sub>           | 78      | V <sub>SS</sub>          | 120     | A <sub>7</sub>           | 162     | V <sub>SS</sub>          |
| 37      | A <sub>8</sub>           | 79      | PD <sub>1</sub>          | 121     | A <sub>9</sub>           | 163     | PD <sub>2</sub>          |
| 38      | A <sub>10</sub>          | 80      | PD <sub>3</sub>          | 122     | N.C.                     | 164     | PD <sub>4</sub>          |
| 39      | N.C.                     | 81      | PD <sub>5</sub>          | 123     | N.C.                     | 165     | PD <sub>6</sub>          |
| 40      | V <sub>CC</sub>          | 82      | PD <sub>7</sub>          | 124     | V <sub>CC</sub>          | 166     | PD <sub>8</sub>          |
| 41      | N.C.                     | 83      | ID <sub>0</sub>          | 125     | N.C.                     | 167     | ID <sub>1</sub>          |
| 42      | N.C.                     | 84      | V <sub>CC</sub>          | 126     | B <sub>0</sub>           | 168     | V <sub>CC</sub>          |

# MB8502E064AB-60/-70

## ■ PIN DESCRIPTIONS

| Symbol  | Function                 | Input/Output | Pin Count |
|---|--------------------------|--------------|-----------|
| A <sub>0</sub> to A <sub>10</sub> , B <sub>0</sub>      | Address Input            | Input        | 12        |
| $\overline{\text{RAS}}_0$ and $\overline{\text{RAS}}_2$ | Row Address Strobe       | Input        | 2         |
| $\overline{\text{CAS}}_0$ to $\overline{\text{CAS}}_7$  | Column Address Strobe    | Input        | 8         |
| $\overline{\text{WE}}_0$ and $\overline{\text{WE}}_2$   | Write Enable             | Input        | 2         |
| $\overline{\text{OE}}_0$ and $\overline{\text{OE}}_2$   | Output Enable            | Input        | 2         |
| DQ <sub>0</sub> to DQ <sub>63</sub>                     | Data Input / Data Output | Input/Output | 64        |
| PD <sub>1</sub> to PD <sub>8</sub>                      | Presence Detect          | Output       | 8         |
| ID <sub>0</sub> and ID <sub>1</sub>                     | ID bit                   | Output       | 2         |
| $\overline{\text{PDE}}$                                 | Presence Detect Enable   | Input        | 1         |
| V <sub>CC</sub>   | Power Supply             | —            | 16        |
| V <sub>SS</sub>   | Ground                   | —            | 16        |
| N.C.  | No Connection            | —            | 16        |

## ■ PRESENCE DETECT (PD) / ID DEFINITION

| Symbol          | MB8502E064AB-60 | MB8502E064AB-70 | Description of PD / ID  |
|-----------------|-----------------|-----------------|---|
| PD <sub>1</sub> | H               | H               | MODULE DENSITY, DRAM ORGANIZATION AND ADDRESSING;<br>Module Density: 16 MB, Number of Bank: 1 Bank<br>Module Configuration: 2 M × 64<br>Mounted DRAM Configuration: 2 M × 8<br>DRAM Address (Row / Column): 11/10 |
| PD <sub>2</sub> | L               | L               |   |
| PD <sub>3</sub> | L               | L               |   |
| PD <sub>4</sub> | H               | H               |   |
| PD <sub>5</sub> | H               | H               | EDO DETECTION; Hyper Page Mode: PD <sub>5</sub> = H   |
| PD <sub>6</sub> | H               | L               | MODULE SPEED; 60 ns: PD <sub>6</sub> = H, PD <sub>7</sub> = H<br>70 ns: PD <sub>6</sub> = L, PD <sub>7</sub> = H  |
| PD <sub>7</sub> | H               | H               |   |
| PD <sub>8</sub> | H               | H               | ECC/PARITY DETECTION; (parity): PD <sub>8</sub> = H   |
| ID <sub>0</sub> | L               | L               | MODULE TYPE; × 64 (parity): ID <sub>0</sub> = L   |
| ID <sub>1</sub> | H               | H               | REFRESH MODE; Self Refresh: ID <sub>1</sub> = H   |

## ■ CAPACITANCE

(T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = +5.0 V)

| Parameter  | Symbol           | Max. | Unit |
|--|------------------|------|------|
| Input Capacitance, Address   | C <sub>IN1</sub> | 20   | pF   |
| Input Capacitance, $\overline{\text{RAS}}$   | C <sub>IN2</sub> | 50   | pF   |
| Input Capacitance, $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ | C <sub>IN3</sub> | 20   | pF   |
| Input/Output Capacitance, DQ <sub>0</sub> to DQ <sub>63</sub>                                | C <sub>DQ</sub>  | 20   | pF   |

# MB8502E064AB-60/-70

## RECOMMENDED OPERATING CONDITIONS

(Referenced to  $V_{SS}$ )

| Parameter                      | Symbol   | Min. | Typ. | Max. | Unit |
|--------------------------------|----------|------|------|------|------|
| Supply Voltage                 | $V_{CC}$ | 4.5  | 5.0  | 5.5  | V    |
| Ground                         | $V_{SS}$ | —    | 0    | —    | V    |
| Input High Voltage, All Inputs | $V_{IH}$ | 2.4  | —    | 6.0  | V    |
| Input Low Voltage, All Inputs* | $V_{IL}$ | -0.3 | —    | 0.8  | V    |
| Ambient Temperature            | $T_A$    | 0    | —    | 70   | °C   |

\* : Undershoots of up to -1.5 volts with a pulse width not exceeding 10 ns are acceptable.

## DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

| Parameter   | Notes            | Symbol    | Condition   | Value |      | Unit          |
|---|------------------|-----------|---|-------|------|---------------|
|   |                  |           |   | Min.  | Max. |               |
| Output High Voltage                                     | *1               | $V_{OH}$  | $I_{OH} = -5.0 \text{ mA}$  | 2.4   | —    | V             |
| Output Low Voltage                                      | *1               | $V_{OL}$  | $I_{OL} = +4.2 \text{ mA}$  | —     | 0.4  | V             |
| Input Leakage Current                                   | $\overline{RAS}$ | $I_{IL}$  | $0 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$ ,<br>$4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ ,<br>$V_{SS} = 0 \text{ V}$ , All other pins<br>not under test = 0 V | -30   | 30   | $\mu\text{A}$ |
|   | Others           |           |   | -10   | 10   |               |
| Output Leakage Current                                  |                  | $I_{OL}$  | $0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V}$ ,<br>$4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ ,<br>Data out disabled  | -10   | 10   | $\mu\text{A}$ |
| Operating Current<br>(Average Power<br>Supply Current)  | *2               | $I_{CC1}$ | $\overline{RAS}$ & $\overline{CAS}$ cycling,<br>$t_{RC} = \text{min}$   | —     | 1200 | mA            |
|   |                  |           |   | —     | 1110 |               |
| Standby Current<br>(Power Supply<br>Current)            | *2               | $I_{CC2}$ | $\overline{RAS} = \overline{CAS} = \overline{PDE} = V_{IH}$<br>$\overline{RAS} = \overline{CAS} = \overline{PDE} \geq V_{CC} - 0.2 \text{ V}$                         | —     | 80   | mA            |
|   |                  |           |   | —     | 69   |               |
| Refresh Current #1<br>(Average Power<br>Supply Current) | *2               | $I_{CC3}$ | $\overline{CAS} = V_{IH}$ , $\overline{RAS} = \text{cycling}$ ,<br>$t_{RC} = \text{min}$  | —     | 1200 | mA            |
|   |                  |           |   | —     | 1110 |               |
| Hyper Page Mode<br>Current                              | *2               | $I_{CC4}$ | $\overline{RAS} = V_{IL}$ , $\overline{CAS} = \text{cycling}$ ,<br>$t_{HPC} = \text{min}$   | —     | 1200 | mA            |
|   |                  |           |   | —     | 1110 |               |
| Refresh Current #2<br>(Average Power<br>Supply Current) | *2               | $I_{CC5}$ | $\overline{RAS} = \text{cycling}$ , $\overline{CAS}$ -before-<br>$\overline{RAS}$ , $t_{RC} = \text{min}$   | —     | 1120 | mA            |
|   |                  |           |   | —     | 1030 |               |
| Refresh Current #3<br>(Average Power Supply Current)    |                  | $I_{CC9}$ | Self Refresh;<br>$A_0$ to $A_{10}$ , $B_0$ , $\overline{WE}$ , $\overline{OE}$ , $\overline{PDE} \geq$<br>$V_{CC} - 2.1 \text{ V}$                                    | —     | 30   | mA            |

**Notes:** \*1. Referenced to  $V_{SS}$ .

\*2.  $I_{CC}$  depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

$I_{CC}$  depends on the number of address change as  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ ,  $V_{IL} > -0.3 \text{ V}$ .

$I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .

# MB8502E064AB-60/-70

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

| No. | Parameter   | Notes | Symbol            | MB8502E064AB-60 |        | MB8502E064AB-70 |        | Unit |
|-----|---|-------|-------------------|-----------------|--------|-----------------|--------|------|
|     |   |       |                   | Min.            | Max.   | Min.            | Max.   |      |
| 1   | Time Between Refresh  |       | t <sub>REF</sub>  | —               | 32.8   | —               | 32.8   | ms   |
| 2   | Random Read/Write Cycle Time                                      |       | t <sub>RC</sub>   | 104             | —      | 124             | —      | ns   |
| 3   | Read-Modify-Write Cycle Time                                      |       | t <sub>RWC</sub>  | 138             | —      | 162             | —      | ns   |
| 4   | Access Time from $\overline{\text{RAS}}$                          | *4,7  | t <sub>RAC</sub>  | —               | 60     | —               | 70     | ns   |
| 5   | Access Time from $\overline{\text{CAS}}$                          | *5,7  | t <sub>CAC</sub>  | —               | 20     | —               | 22     | ns   |
| 6   | Column Address Access Time  | *6,7  | t <sub>AA</sub>   | —               | 35     | —               | 40     | ns   |
| 7   | Output Hold Time  |       | t <sub>OH</sub>   | 5               | —      | 5               | —      | ns   |
| 8   | Output Hold Time from $\overline{\text{CAS}}$                     |       | t <sub>OHc</sub>  | 7               | —      | 7               | —      | ns   |
| 9   | Output Buffer Turn on Delay Time                                  |       | t <sub>ON</sub>   | 2               | —      | 2               | —      | ns   |
| 10  | Output Buffer Turn off Delay Time                                 | *8    | t <sub>OFF</sub>  | —               | 20     | —               | 22     | ns   |
| 11  | Output Buffer Turn off Delay Time from $\overline{\text{RAS}}$    | *8    | t <sub>OFFR</sub> | —               | 15     | —               | 17     | ns   |
| 12  | Output Buffer Turn off Delay Time from $\overline{\text{WE}}$     | *8    | t <sub>WEZ</sub>  | —               | 20     | —               | 22     | ns   |
| 13  | Transition Time   |       | t <sub>T</sub>    | 1               | 16     | 1               | 16     | ns   |
| 14  | $\overline{\text{RAS}}$ Precharge Time                            |       | t <sub>RP</sub>   | 40              | —      | 50              | —      | ns   |
| 15  | $\overline{\text{RAS}}$ Pulse Width                               |       | t <sub>RAS</sub>  | 60              | 100000 | 70              | 100000 | ns   |
| 16  | $\overline{\text{RAS}}$ Hold Time                                 |       | t <sub>RSH</sub>  | 20              | —      | 22              | —      | ns   |
| 17  | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time |       | t <sub>CRP</sub>  | 5               | —      | 5               | —      | ns   |
| 18  | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time     | *9,10 | t <sub>RCD</sub>  | 12              | 45     | 12              | 53     | ns   |
| 19  | $\overline{\text{CAS}}$ Pulse Width                               |       | t <sub>CAS</sub>  | 10              | —      | 13              | —      | ns   |
| 20  | $\overline{\text{CAS}}$ Hold Time                                 |       | t <sub>CSH</sub>  | 38              | —      | 48              | —      | ns   |
| 21  | $\overline{\text{CAS}}$ Precharge Time (Normal)                   | *17   | t <sub>CPN</sub>  | 10              | —      | 10              | —      | ns   |
| 22  | Row Address Set Up Time   |       | t <sub>ASR</sub>  | 5               | —      | 5               | —      | ns   |
| 23  | Row Address Hold Time   |       | t <sub>RAH</sub>  | 8               | —      | 8               | —      | ns   |
| 24  | Column Address Set Up Time  |       | t <sub>ASC</sub>  | 0               | —      | 0               | —      | ns   |
| 25  | Column Address Hold Time  |       | t <sub>CAH</sub>  | 10              | —      | 10              | —      | ns   |
| 26  | Column Address Hold Time from $\overline{\text{RAS}}$             |       | t <sub>AR</sub>   | 22              | —      | 22              | —      | ns   |
| 27  | $\overline{\text{RAS}}$ to Column Address Delay Time              | *11   | t <sub>RAD</sub>  | 10              | 35     | 10              | 40     | ns   |
| 28  | Column Address to $\overline{\text{RAS}}$ Lead Time               |       | t <sub>RAL</sub>  | 35              | —      | 40              | —      | ns   |
| 29  | Column Address to $\overline{\text{CAS}}$ Lead Time               |       | t <sub>CAL</sub>  | 23              | —      | 28              | —      | ns   |
| 30  | Read Command Set Up Time  |       | t <sub>RCS</sub>  | 5               | —      | 5               | —      | ns   |

# MB8502E064AB-60/-70

(Continued)

| No. | Parameter  | Notes  | Symbol            | MB8502E064AB-60 |      | MB8502E064AB-70 |      | Unit |
|-----|--|--------|-------------------|-----------------|------|-----------------|------|------|
|     |  |        |                   | Min.            | Max. | Min.            | Max. |      |
| 31  | Read Command Hold Time Referenced to $\overline{\text{RAS}}$                                   | *12    | $t_{\text{RRH}}$  | -2              | —    | -2              | —    | ns   |
| 32  | Read Command Hold Time Referenced to $\overline{\text{CAS}}$                                   | *12    | $t_{\text{RCH}}$  | 0               | —    | 0               | —    | ns   |
| 33  | Write Command Set Up Time  | *13,18 | $t_{\text{WCS}}$  | 0               | —    | 0               | —    | ns   |
| 34  | Write Command Hold Time  |        | $t_{\text{WCH}}$  | 10              | —    | 10              | —    | ns   |
| 35  | Write Command Hold Time from $\overline{\text{RAS}}$   |        | $t_{\text{WCR}}$  | 22              | —    | 22              | —    | ns   |
| 36  | $\overline{\text{WE}}$ Pulse Width   |        | $t_{\text{WP}}$   | 8               | —    | 8               | —    | ns   |
| 37  | Write Command to $\overline{\text{RAS}}$ Lead Time   |        | $t_{\text{RWL}}$  | 20              | —    | 22              | —    | ns   |
| 38  | Write Command to $\overline{\text{CAS}}$ Lead Time   |        | $t_{\text{CWL}}$  | 10              | —    | 13              | —    | ns   |
| 39  | DIN Set Up Time  |        | $t_{\text{DS}}$   | -2              | —    | -2              | —    | ns   |
| 40  | DIN Hold Time  |        | $t_{\text{DH}}$   | 15              | —    | 15              | —    | ns   |
| 41  | Data Hold Time from $\overline{\text{RAS}}$  |        | $t_{\text{DHR}}$  | 24              | —    | 24              | —    | ns   |
| 42  | $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time                                   | *18    | $t_{\text{RWD}}$  | 75              | —    | 87              | —    | ns   |
| 43  | $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time                                   | *18    | $t_{\text{CWD}}$  | 32              | —    | 36              | —    | ns   |
| 44  | Column Address to $\overline{\text{WE}}$ Delay Time  | *18    | $t_{\text{AWD}}$  | 47              | —    | 54              | —    | ns   |
| 45  | $\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh Cycles) |        | $t_{\text{RPC}}$  | 3               | —    | 3               | —    | ns   |
| 46  | $\overline{\text{CAS}}$ Set Up Time (C-B-R Refresh)  |        | $t_{\text{CSR}}$  | 5               | —    | 5               | —    | ns   |
| 47  | $\overline{\text{CAS}}$ Hold Time (C-B-R Refresh)  |        | $t_{\text{CHR}}$  | 12              | —    | 14              | —    | ns   |
| 48  | Access Time from $\overline{\text{OE}}$  | *7     | $t_{\text{OEA}}$  | —               | 20   | —               | 22   | ns   |
| 49  | Output Buffer Turn off Delay from $\overline{\text{OE}}$                                       | *8     | $t_{\text{WCZ}}$  | —               | 20   | —               | 22   | ns   |
| 50  | $\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data                     |        | $t_{\text{WCL}}$  | 15              | —    | 15              | —    | ns   |
| 51  | $\overline{\text{OE}}$ to $\overline{\text{CAS}}$ Lead Time                                    |        | $t_{\text{COL}}$  | 5               | —    | 5               | —    | ns   |
| 52  | $\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$                          | *14    | $t_{\text{OEH}}$  | 5               | —    | 5               | —    | ns   |
| 53  | $\overline{\text{OE}}$ to Data in Delay Time   |        | $t_{\text{OED}}$  | 20              | —    | 22              | —    | ns   |
| 54  | $\overline{\text{RAS}}$ to Data in Delay Time  |        | $t_{\text{RDD}}$  | 15              | —    | 15              | —    | ns   |
| 55  | $\overline{\text{CAS}}$ to Data in Delay Time  |        | $t_{\text{CDD}}$  | 20              | —    | 22              | —    | ns   |
| 56  | DIN to $\overline{\text{CAS}}$ Delay Time  | *15    | $t_{\text{DZC}}$  | -2              | —    | -2              | —    | ns   |
| 57  | DIN to $\overline{\text{OE}}$ Delay Time   | *15    | $t_{\text{DZO}}$  | -2              | —    | -2              | —    | ns   |
| 58  | $\overline{\text{OE}}$ Precharge Time  |        | $t_{\text{OEP}}$  | 8               | —    | 8               | —    | ns   |
| 59  | $\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$                         |        | $t_{\text{OECH}}$ | 10              | —    | 10              | —    | ns   |
| 60  | $\overline{\text{WE}}$ Precharge Time  |        | $t_{\text{WPZ}}$  | 8               | —    | 8               | —    | ns   |

# MB8502E064AB-60/-70

(Continued)

| No. | Parameter  | Notes | Symbol      | MB8502E064AB-60 |        | MB8502E064AB-70 |        | Unit    |
|-----|--|-------|-------------|-----------------|--------|-----------------|--------|---------|
|     |  |       |             | Min.            | Max.   | Min.            | Max.   |         |
| 61  | $\overline{WE}$ to Data in Delay Time                                      |       | $t_{WED}$   | 20              | —      | 22              | —      | ns      |
| 62  | Hyper Page Mode $\overline{RAS}$ Pulse Width                               |       | $t_{RASP}$  | —               | 100000 | —               | 200000 | ns      |
| 63  | Hyper Page Mode Read/Write Cycle Time                                      |       | $t_{HPC}$   | 25              | —      | 30              | —      | ns      |
| 64  | Hyper Page Mode Read-Modify-Write Cycle Time                               |       | $t_{HPRWC}$ | 69              | —      | 79              | —      | ns      |
| 65  | Access Time from $\overline{CAS}$ Precharge                                | *7,16 | $t_{CPA}$   | —               | 40     | —               | 45     | ns      |
| 66  | Hyper Page Mode $\overline{CAS}$ Precharge Time                            |       | $t_{CP}$    | 10              | —      | 10              | —      | ns      |
| 67  | Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge |       | $t_{RHCP}$  | 40              | —      | 45              | —      | ns      |
| 68  | Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time   | *18   | $t_{CPWD}$  | 52              | —      | 59              | —      | ns      |
| 69  | $\overline{RAS}$ Pulse Width (Self Refresh)                                | *19   | $t_{RASS}$  | 100             | —      | 100             | —      | $\mu s$ |
| 70  | $\overline{RAS}$ Precharge Time (Self Refresh)                             | *19   | $t_{RPS}$   | 104             | —      | 124             | —      | ns      |
| 71  | $\overline{CAS}$ Hold Time (Self Refresh)                                  | *19   | $t_{CHS}$   | -52             | —      | -52             | —      | ns      |

# MB8502E064AB-60/-70

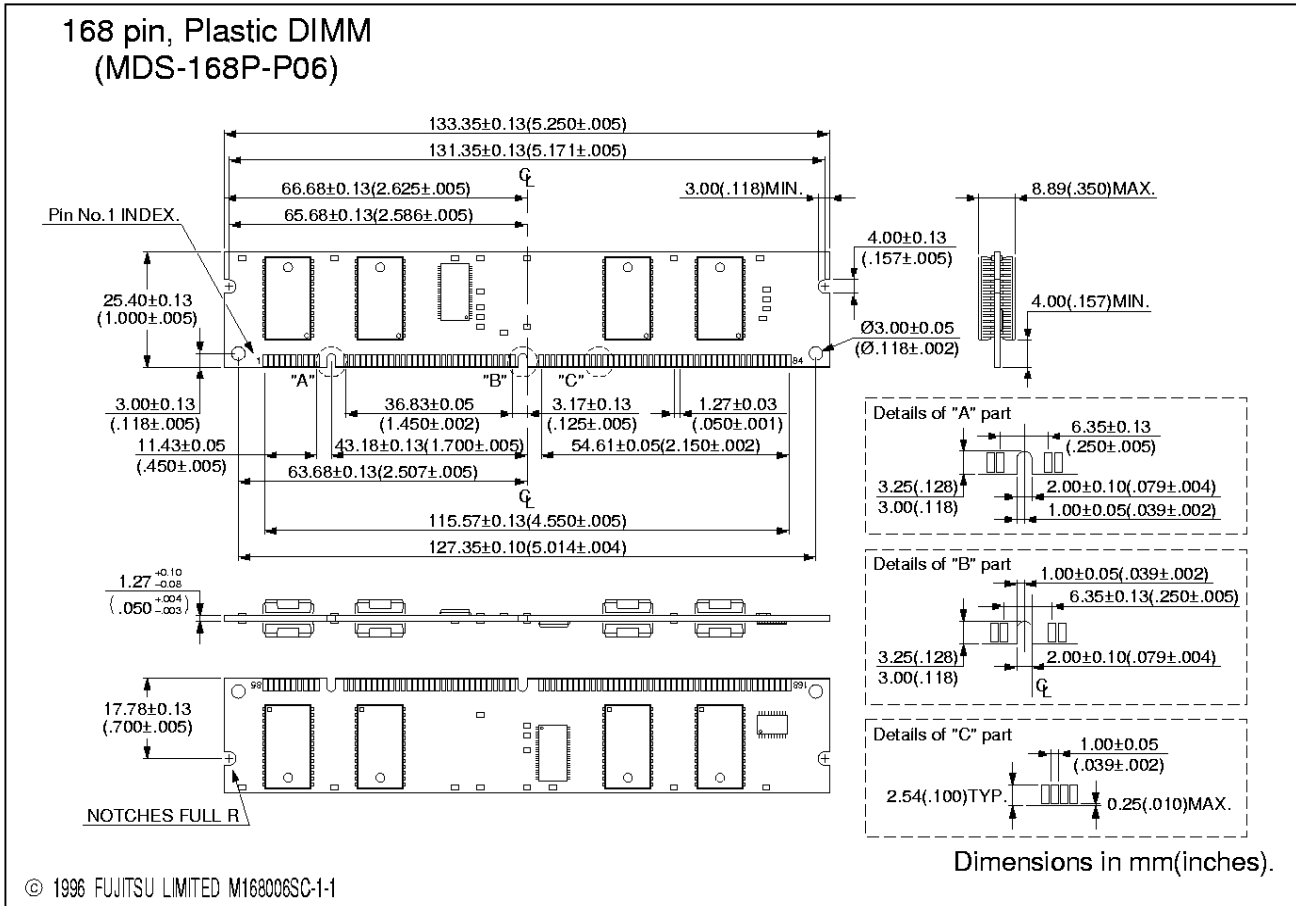
- Notes:**
- \*1. An initial pause ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{IH}}$ ) of 200  $\mu\text{s}$  is required after power-up followed by any eight  $\overline{\text{RAS}}$ -only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles are required instead of eight  $\overline{\text{RAS}}$  cycles.
  - \*2. AC characteristics assume  $t_{\text{r}} = 5 \text{ ns}$ .
  - \*3.  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are reference levels for measuring the timing of input signals. Transition times are measured between  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max).
  - \*4. Assumes that  $t_{\text{rCD}} \leq t_{\text{rCD}} (\text{max})$ ,  $t_{\text{rAD}} \leq t_{\text{rAD}} (\text{max})$ . If  $t_{\text{rCD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{rAC}}$  will be increased by the amount that  $t_{\text{rCD}}$  exceeds the value shown.
  - \*5. If  $t_{\text{rCD}} \geq t_{\text{rCD}} (\text{max})$ ,  $t_{\text{rAD}} \geq t_{\text{rAD}} (\text{max})$ , and  $t_{\text{ASC}} \geq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{r}}$ , access time is  $t_{\text{CAC}}$ .
  - \*6. If  $t_{\text{rAD}} \geq t_{\text{rAD}} (\text{max})$  and  $t_{\text{ASC}} \leq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{r}}$ , access time is  $t_{\text{AA}}$ .
  - \*7. Measured with a load equivalent to two TTL loads and 100 pF.
  - \*8.  $t_{\text{OFF}}$ ,  $t_{\text{OEZ}}$ ,  $t_{\text{OFR}}$  and  $t_{\text{WEZ}}$  is specified that output buffer change to high-impedance state.
  - \*9. Operation within the  $t_{\text{rCD}} (\text{max})$  limit ensures that  $t_{\text{rAC}} (\text{max})$  can be met.  $t_{\text{rCD}} (\text{max})$  is specified as a reference point only; if  $t_{\text{rCD}}$  is greater than the specified  $t_{\text{rCD}} (\text{max})$  limit, access time is controlled exclusively by  $t_{\text{CAC}}$  or  $t_{\text{AA}}$ .
  - \*10.  $t_{\text{rCD}} (\text{min}) = t_{\text{RAH}} (\text{min}) + 2 t_{\text{r}} + t_{\text{ASC}} (\text{min})$ .
  - \*11. Operation within the  $t_{\text{rAD}} (\text{max})$  limit ensures that  $t_{\text{rAC}} (\text{max})$  can be met.  $t_{\text{rAD}} (\text{max})$  is specified as a reference point only; if  $t_{\text{rAD}}$  is greater than the specified  $t_{\text{rAD}} (\text{max})$  limit, access time is controlled exclusively by  $t_{\text{CAC}}$  or  $t_{\text{AA}}$ .
  - \*12. Either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be satisfied for a read cycle.
  - \*13.  $t_{\text{WCS}}$  is specified as a reference point only. If  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$  the data output pin will remain High-Z state through entire cycle.
  - \*14. Assumes that  $t_{\text{WCS}} < t_{\text{WCS}} (\text{min})$ .
  - \*15. Either  $t_{\text{DZC}}$  or  $t_{\text{DZO}}$  must be satisfied.
  - \*16.  $t_{\text{CPA}}$  is access time from the selection of a new column address (caused by changing  $\overline{\text{CAS}}$  from "L" to "H"). Therefore, if  $t_{\text{CP}}$  become long,  $t_{\text{CPA}}$  also become longer than  $t_{\text{CPA}} (\text{max})$ .
  - \*17. Assumes that  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh.
  - \*18.  $t_{\text{WCS}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$ , and  $t_{\text{CPWD}}$  are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$ , the cycle is an early write cycle and  $\text{D}_{\text{OUT}}$  pin will maintain high-impedance state throughout the entire cycle. If  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ , and  $t_{\text{CPWD}} \geq t_{\text{CPWD}} (\text{min})$ , the cycle is a read-modify-write cycle and data from the selected cell will appear at the  $\text{D}_{\text{OUT}}$  pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the  $\text{D}_{\text{OUT}}$  pin, and write operation can be executed by satisfying  $t_{\text{RWL}}$ ,  $t_{\text{CWL}}$ ,  $t_{\text{RAL}}$  and  $t_{\text{CAL}}$  specifications.
  - \*19. Assumes that self refresh.

\*Source: See MB8117805A Data Sheet for details on the electricals.

# MB8502E064AB-60/-70

## ■ PACKAGE DIMENSIONS

(Suffix: DG)



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