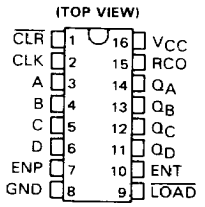
TYPES SN54ALS160 THRU SN54ALS163
SN74ALS160 THRU SN74ALS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**



J Suffix—Case 620-08 (Ceramic)
N Suffix—Case 648-05 (Plastic)

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'ALS160 and 'ALS162 are decade counters, and the 'ALS161 and 'ALS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'ALS160 and 'ALS161 is asynchronous and a low level at the clear input sets both of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'ALS162 and 'ALS163 is synchronous and a low level at the clear input sets both of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS160 through SN54ALS163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS160 through SN74ALS163 are characterized for operation from 0°C to 70°C.

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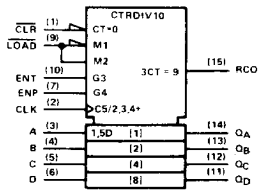
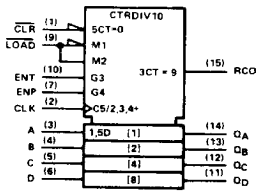
logic symbols

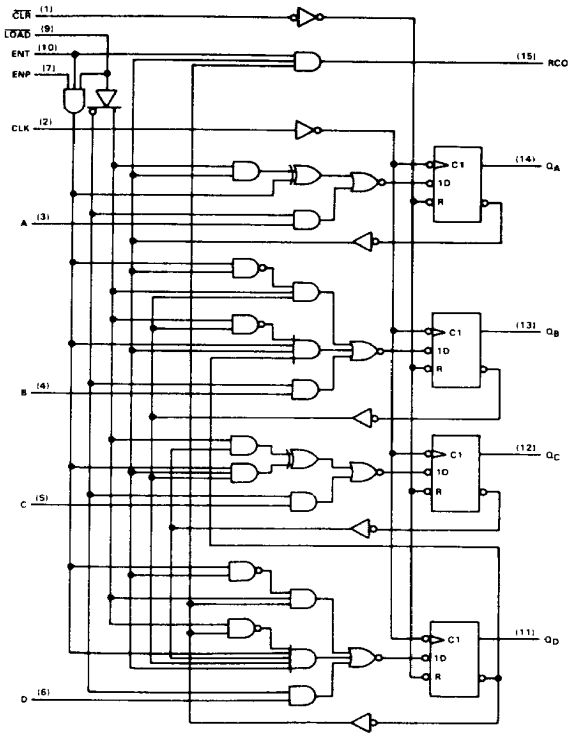
'ALS160 DECADE
COUNTER WITH DIRECT CLEAR



'ALS162 DECADE
COUNTER WITH SYNCHRONOUS CLEAR



'ALS160 logic diagram (positive logic)

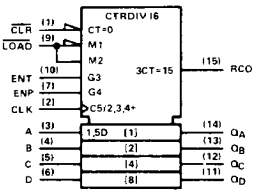


'ALS162 decade counter is similar; however the clear is synchronous as shown for the 'ALS163 binary counter on the following page.

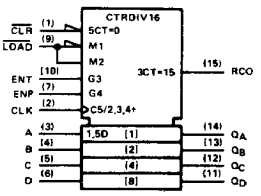
Pin numbers shown are for J and N packages.

logic symbols

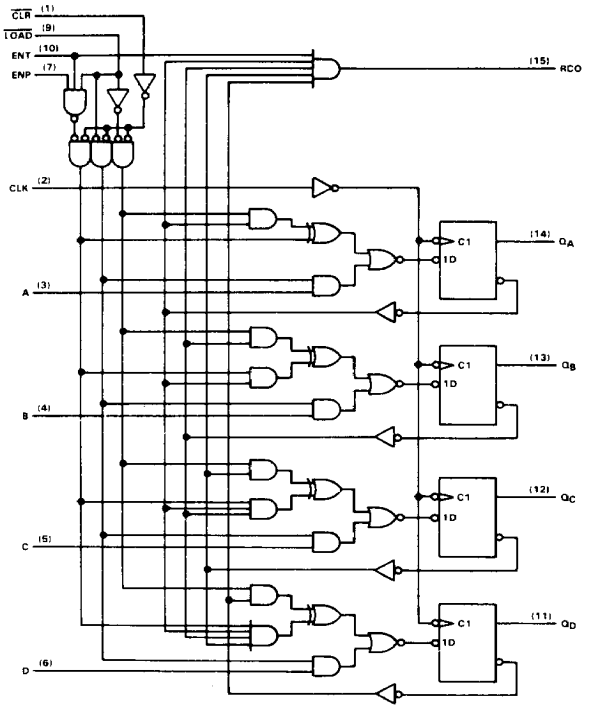
'ALS161 BINARY COUNTER WITH DIRECT CLEAR



'ALS163 BINARY COUNTER WITH SYNCHRONOUS CLEAR



'ALS163 logic diagram (positive logic)



'ALS161 synchronous binary counter is similar; however the clear is asynchronous as shown for the 'ALS160 decade counter on the preceding page.

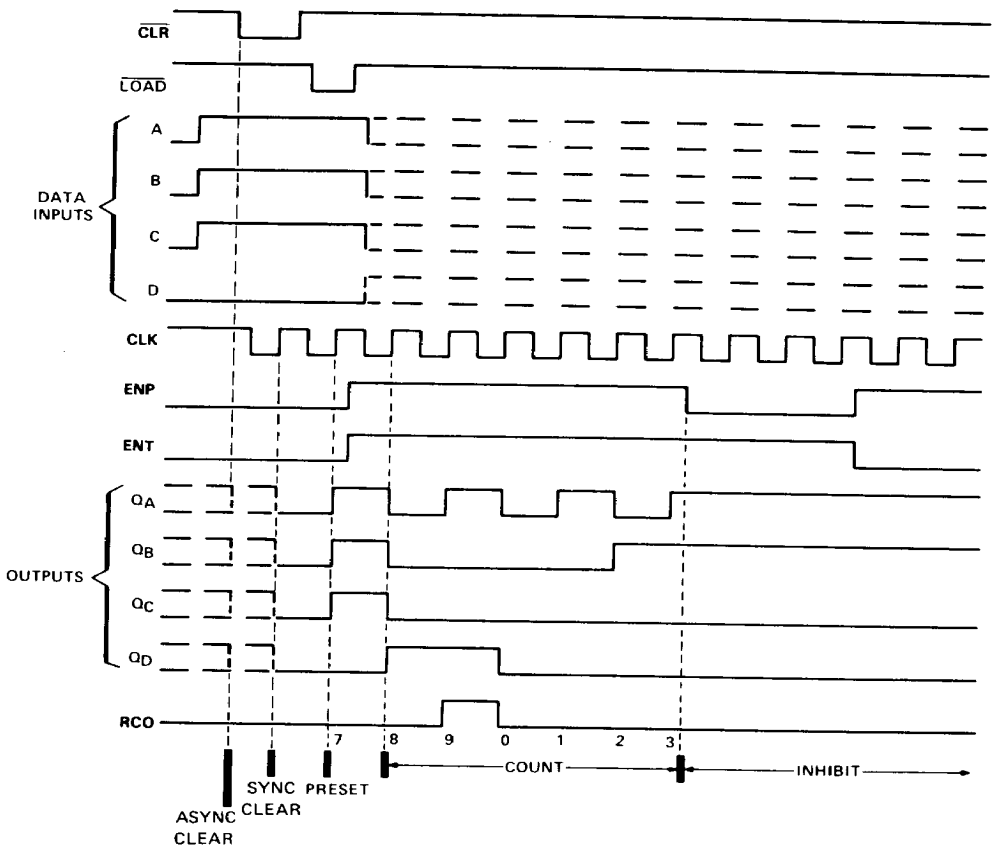
Pin numbers shown are for J and N packages.

typical clear, preset, count, and inhibit sequences

'ALS160, 'ALS162

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS160 is asynchronous, 'ALS162 is synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

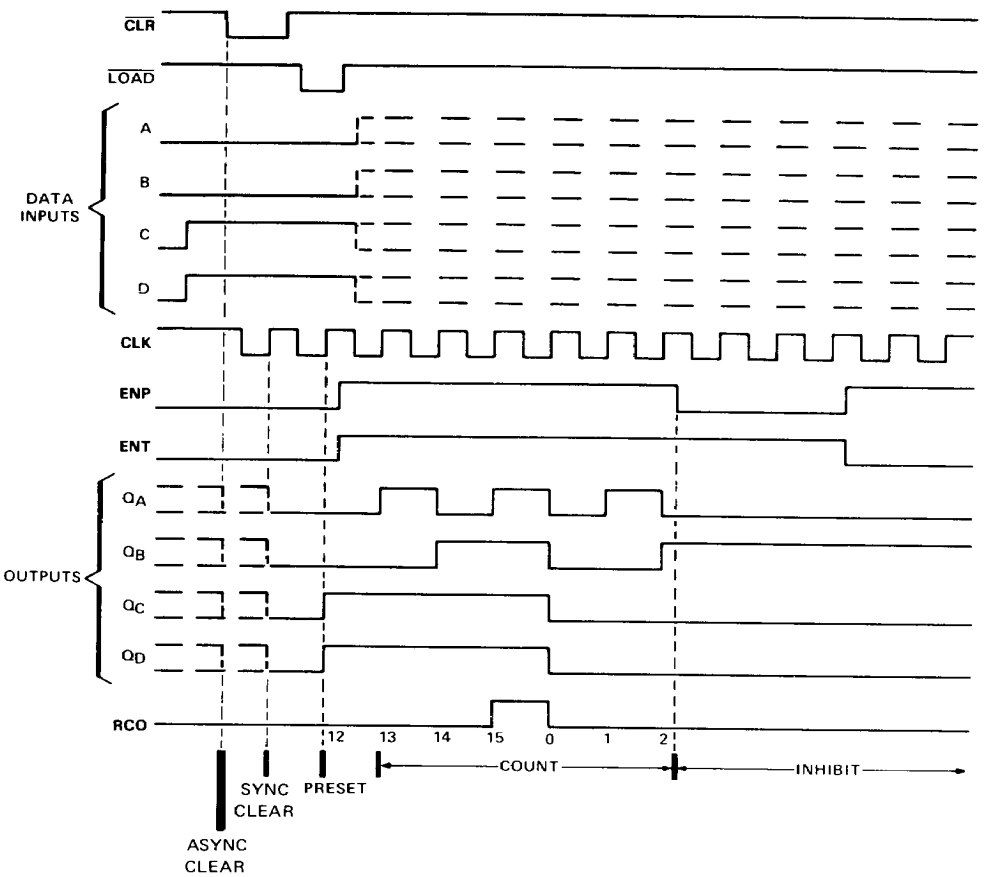


typical clear, preset, count, and inhibit sequences

'ALS161, 'ALS163

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS161 is asynchronous, 'ALS163 is synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS160 thru SN54ALS163 . . . . . −55 °C to 125 °C
SN74ALS160 thru SN74ALS163 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

				SN54ALS160 THRU SN54ALS163			SN74ALS160 THRU SN74ALS163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output voltage					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency	'ALS160, 'ALS162		0		30	0		30	MHz
		'ALS161, 'ALS163		0		30	0		30	
t_w	Pulse duration	CLK High		18			15			ns
		CLK Low		15			15			
		'ALS160, 'ALS161 $\overline{CLR}$ low		18			16			
t_{su}	Setup time before CLK↑	A, B, C, D		15			15			ns
		ENP, ENT	'ALS160, 'ALS161	20			20			
			'ALS162, 'ALS163	20			20			
		'ALS160, 'ALS161 $\overline{CLR}$ inactive		15			15			
		'ALS162, 'ALS163	$\overline{CLR}$ Low	25			25			
			$\overline{CLR}$ high (inactive)	15			15			
t_h	Hold time, all synchronous inputs after CLK↑			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS160 THRU SN54ALS163			SN74ALS160 THRU SN74ALS163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}			I_{OH} = −0.4 mA	V_{CC}−2						V
			I_{OH} = −0.4 mA				V_{CC}−2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	$\overline{LOAD}$, CLK or ENT	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All other					0.1			0.1	
I_{IH}	$\overline{LOAD}$, CLK or ENT	V_{CC} = 5.5 V,	V_I = 0.4 V			40			40	μA
	All other					20			20	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O*		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCL}		V_{CC} = 5.5 V				16			16	mA
I_{CCH}		V_{CC} = 5.5 V				15.5			15.5	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.
*The current produced by grounding the outputs is approximately twice that produced with 2.25 V on the outputs.

'ALS160 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS160 SN54ALS161		SN74ALS160 SN74ALS161		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS160		30		30		MHz
	'ALS161		30		30		
t_{PLH}	CLK	RCO	8	25	8	23	ns
t_{PHL}			7	20	7	20	
t_{PLH}	CLK	Any Q	4	22	4	22	ns
t_{PHL}			6	28	6	28	
t_{PLH}	ENT	RCO	5	20	5	20	ns
t_{PHL}			4	16	4	16	
t_{PHL}	$\overline{CLR}$	Any Q	8	28	8	28	ns
t_{PHL}	$\overline{CLR}$	RCO	11	35	11	30	ns

'ALS162 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS162 SN54ALS163		SN74ALS162 SN74ALS163		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS162		30		30		MHz
	'ALS163		30		30		
t_{PLH}	CLK	RCO	8	25	8	23	ns
t_{PHL}			7	20	7	20	
t_{PLH}	CLK	Any Q	4	22	4	22	ns
t_{PHL}			6	28	6	28	
t_{PLH}	ENT	RCO	5	20	5	20	ns
t_{PHL}			4	16	4	16	

See next page for 161 and 163.

'ALS161 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS160 SN54ALS161		SN74ALS160 SN74ALS161		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS160		30		30		MHz
	'ALS161		30		30		
t_{PLH}	CLK	RCO	8	25	8	23	ns
t_{PHL}			7	20	7	20	
t_{PLH}	CLK	Any Q	4	22	4	22	ns
t_{PHL}			6	26	6	26	
t_{PLH}	ENT	RCO	5	20	5	20	ns
t_{PHL}			4	16	4	16	
t_{PHL}	$\overline{CLR}$	Any Q	8	28	8	28	ns
t_{PHL}	$\overline{CLR}$	RCO	11	31	11	28	ns

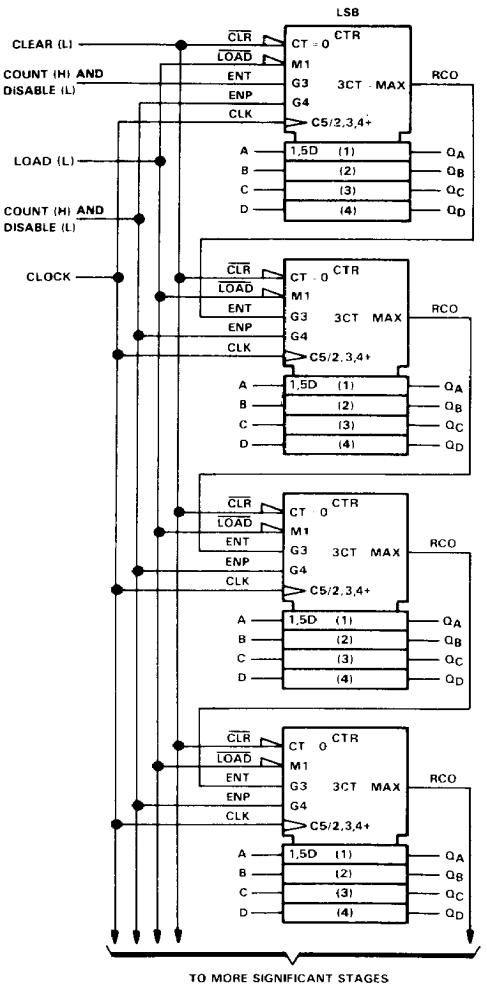
'ALS163 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS162 SN54ALS163		SN74ALS162 SN74ALS163		
			MIN	MAX	MIN	MAX	
f_{max}	'ALS162		30		30		MHz
	'ALS163		30		30		
t_{PLH}	CLK	RCO	8	25	8	23	ns
t_{PHL}			7	20	7	20	
t_{PLH}	CLK	Any Q	4	22	4	22	ns
t_{PHL}			6	28	6	28	
t_{PLH}	ENT	RCO	5	20	5	20	ns
t_{PHL}			4	16	4	16	

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'ALS160 and 'ALS162 will count in BCD and the 'ALS161 and 'ALS163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



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