

# MH2M08ATNA-85L,-10L,-12L,-15L / MH2M08ATNA-85H,-10H,-12H,-15H

16777216-BIT (2097152-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The MH2M08ATNA is a 16777216-bits CMOS static RAM module organized as 2097152-words by 8-bits. It consists of sixteen industry standard 128K × 8 static RAMs and two decoders.

The stand-by current is low enough for a battery back-up application. It is mounted a TSOP package on a 36-pin dual in line package.

## FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH2M08ATNA-85L	85ns	138mA	800 μA (V <sub>cc</sub> = 3.0V)
MH2M08ATNA-10L	100ns		
MH2M08ATNA-12L	120ns		
MH2M08ATNA-15L	150ns		
MH2M08ATNA-85H	85ns	160 μA (V <sub>cc</sub> = 3.0V)	
MH2M08ATNA-10H	100ns		
MH2M08ATNA-12H	120ns		
MH2M08ATNA-15H	150ns		

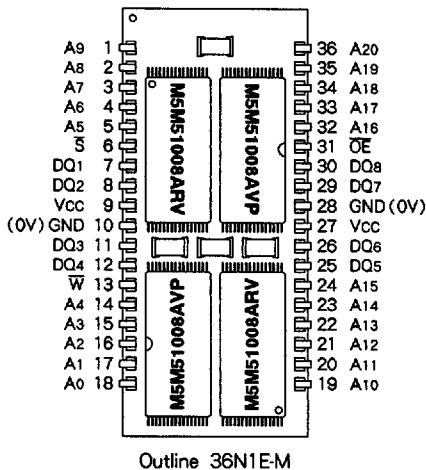
- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Three-state outputs : OR-tie capability
- Simple memory expansion by  $\bar{S}$
- $\bar{OE}$  prevents data contention in the I/O bus
- Common data I/O
- 36-pin 600mil dual in-line package
- Solder dipping lead

## APPLICATION

Small capacity memory units

## PIN CONFIGURATION (TOP VIEW)

(Both side, 2-layer)



# MH2M08ATNA

16777216-BIT  
(2097152-WORD BY 8-BIT) CMOS STATIC RAM

## FUNCTION

The operation mode of the MH2M08ATNA is determined by a combination of the device control inputs  $\bar{S}$ ,  $\bar{W}$  and  $\bar{OE}$ . Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level  $\bar{W}$  overlaps with the low level  $\bar{S}$ . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of  $\bar{W}$ ,  $\bar{S}$ , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable  $\bar{OE}$  directly controls the output stage. Setting the  $\bar{OE}$  at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

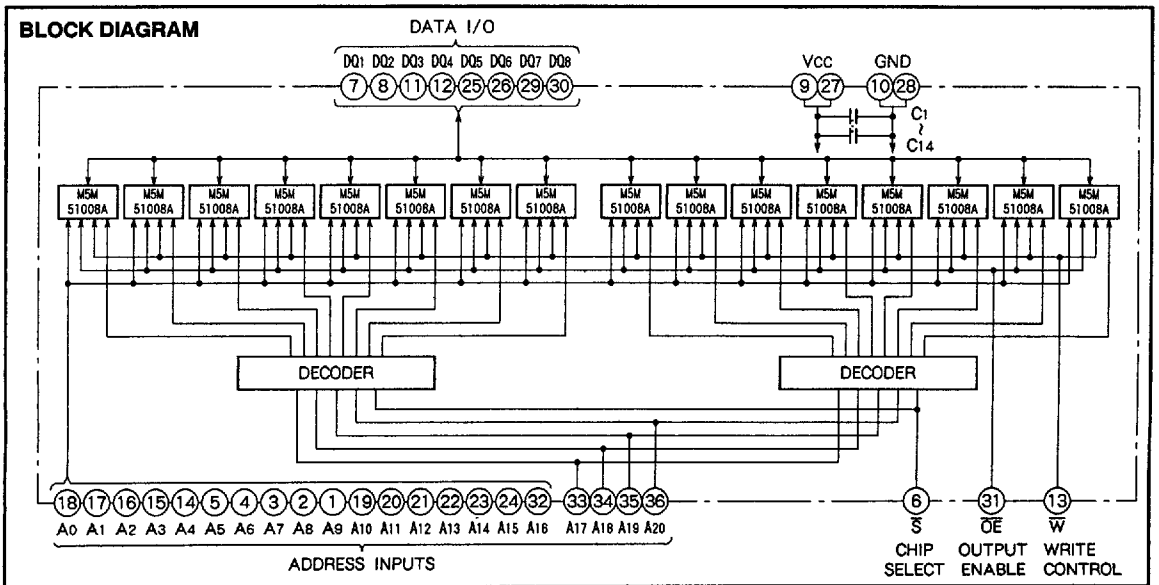
A read cycle is executed by setting  $\bar{W}$  at a high level and  $\bar{OE}$  at a low level while  $\bar{S}$  are in an active state.

When setting  $\bar{S}$  at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by  $\bar{S}$ . The power supply current is reduced as low as the stand-by current which is specified as  $I_{cc3}$  or  $I_{cc4}$ , and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

## FUNCTION TABLE

$\bar{S}$	$\bar{W}$	$\bar{OE}$	Mode	DQ	$I_{cc}$
H	X	X	Non-selection	High-impedance	Stand-by
L	L	X	Write	DIN	Active
L	H	L	Read	DOUT	Active
L	H	H		High-impedance	Active

## BLOCK DIAGRAM



**MH2M08ATNA**

16777216-BIT

(2097152-WORD BY 8-BIT) CMOS STATIC RAM

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage	With respect to GND	- 0.3~7	V
V <sub>i</sub>	Input voltage		- 0.3*~V <sub>cc</sub> + 0.3	V
V <sub>o</sub>	Output voltage		0~V <sub>cc</sub>	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	700	mW
T <sub>opr</sub>	Operating temperature		0~70	°C
T <sub>stg</sub>	Storage temperature		- 40~125	°C

\* - 3.0V in case of AC (Pulse width ≤ 50ns)

**ELECTRICAL CHARACTERISTICS** (T<sub>a</sub> = 0~70°C, V<sub>cc</sub> = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High input voltage		3.2		V <sub>cc</sub> +0.3	V
V <sub>IL</sub>	Low input voltage		- 0.3*		0.8	V
V <sub>OH</sub>	High output voltage	I <sub>OH</sub> = - 1mA	2.4			V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 2mA			0.4	V
I <sub>i</sub>	Input leakage current	V <sub>i</sub> = 0~V <sub>cc</sub>			± 16	μA
I <sub>o</sub>	Output current in off-state	$\bar{S} = V_{IH}$ or $\overline{OE} = V_{IH}$ , V <sub>I/O</sub> = 0~V <sub>cc</sub>			± 16	μA
I <sub>cc1</sub>	Active supply current (AC. MOS level)	$\bar{S} \leq 0.2V$ , output open other input ≤ 0.2V or ≥ V <sub>cc</sub> - 0.2V Min. cycle		95	133	mA
I <sub>cc2</sub>	Active supply current (AC. TTL level)	$\bar{S} = V_{IL}$ , output open other input = V <sub>IL</sub> or V <sub>IH</sub> Min. cycle		98	138	mA
I <sub>cc3</sub>	Stand-by supply current	$\bar{S} \geq V_{cc} - 0.2V$ , A <sub>17</sub> ~A <sub>20</sub> ≤ 0.2V or ≥ V <sub>cc</sub> - 0.2V other inputs = 0~V <sub>cc</sub>	-L		1600	μA
			-H		21	
I <sub>cc4</sub>	Stand-by supply current	$\bar{S} = V_{IH}$ , other inputs = 0~V <sub>cc</sub>			48	mA
C <sub>i</sub>	Input capacitance	V <sub>i</sub> = GND, V <sub>i</sub> = 25mVrms, f = 1MHz			140	pF
C <sub>o</sub>	Output capacitance	V <sub>o</sub> = GND, V <sub>o</sub> = 25mVrms, f = 1MHz			160	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark).

2. Typical value is V<sub>cc</sub> = 5V, T<sub>a</sub> = 25°C.

\* - 3.0V in case of AC (Pulse width ≤ 50ns)

# MH2M08ATNA

16777216-BIT  
(2097152-WORD BY 8-BIT) CMOS STATIC RAM

**AC ELECTRICAL CHARACTERISTICS** (Ta = 0~70 °C, Vcc = 5 ± 10 %, unless otherwise noted)

**MEASUREMENT CONDITIONS**

Input pulse levels.....VIH = 3.2V, VIL = 0.6V

Input rise and fall time.....5ns

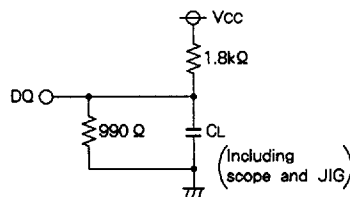
Reference levels.....VOH = VOL = 1.5V

Transition is measured ± 500mV from steady state voltage.(for ten, tdis)

Output loads..... CL = 100pF (-10L, -12L, -15L, -10H, -12H, -15H)

CL = 30pF (-85L, -85H)

CL = 5pF (for ten, tdis)



**Fig. 1 Output load**

**Read cycle**

Symbol	Parameter	Limits								Unit
		MH2M08ATNA-85L		MH2M08ATNA-10L		MH2M08ATNA-12L		MH2M08ATNA-15L		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCR	Read cycle time	85		100		120		150		ns
ta(A)	Address access time		85		100		120		150	ns
ta(S)	Chip select access time		85		100		120		150	ns
ta(OE)	Output enable access time		35		45		50		60	ns
tdis(S)	Output disable time after S high		40		45		50		55	ns
tdis(OE)	Output disable time after OE high		25		30		35		40	ns
ten(S)	Output enable time after S low	10		10		10		10		ns
ten(OE)	Output enable time after OE low	5		5		5		5		ns
tv(A)	Data valid time after address change	10		10		10		10		ns

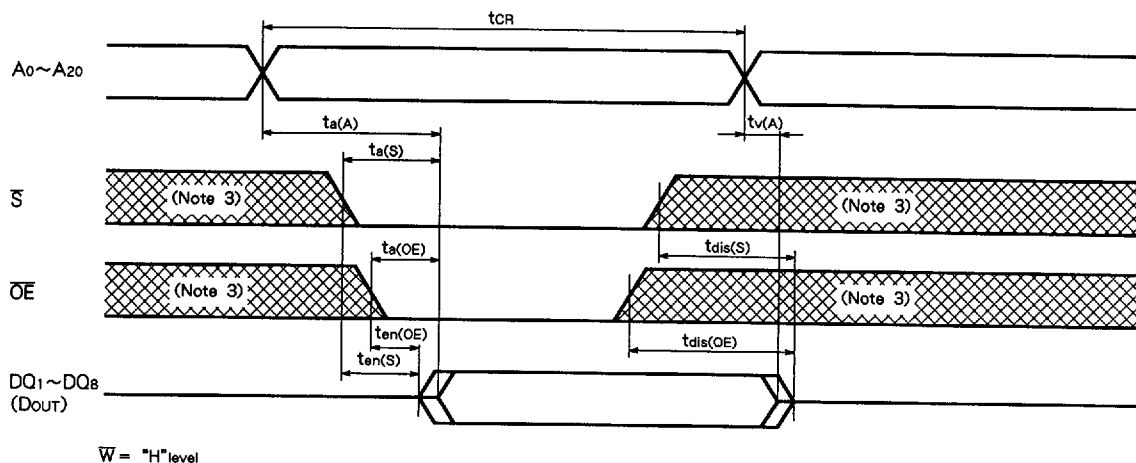
**Write cycle**

Symbol	Parameter	Limits								Unit
		MH2M08ATNA-85L		MH2M08ATNA-85L		MH2M08ATNA-85L		MH2M08ATNA-85L		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCW	Write cycle time	85		100		120		150		ns
tw(W)	Write pulse width	55		65		75		85		ns
tsu(A)	Address set up time	0		0		0		0		ns
tsu(A-WH)	Address set up time with respect to W high	65		75		85		100		ns
tsu(S)	Chip select set up time	80		90		100		115		ns
tsu(D)	Data set up time	30		35		40		45		ns
th(D)	Data hold time	0		0		0		0		ns
trec(W)	Write recovery time	0		0		0		0		ns
tdis(W)	Output disable time after W low		25		30		35		40	ns
tdis(OE)	Output disable time after OE high		25		30		35		40	ns
ten(W)	Output enable time after W high	5		5		5		5		ns
ten(OE)	Output enable time after OE low	5		5		5		5		ns

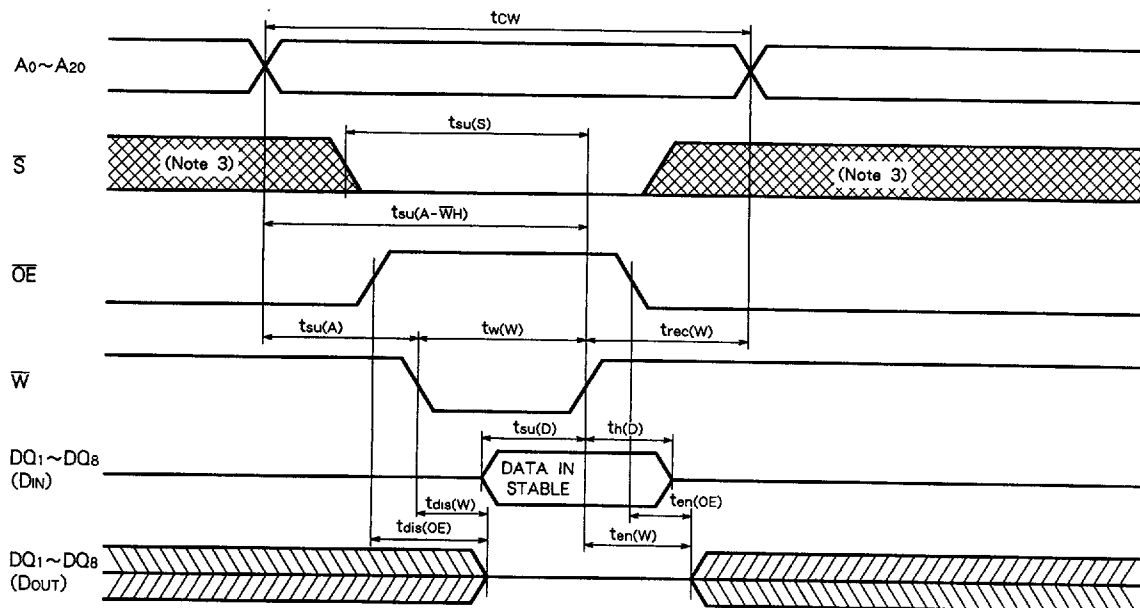
**MH2M08ATNA**

1677216-BIT  
(2097152-WORD BY 8-BIT) CMOS STATIC RAM

**TIMING DIAGRAM**  
Read cycle



**Write cycle ( $\bar{W}$  control)**

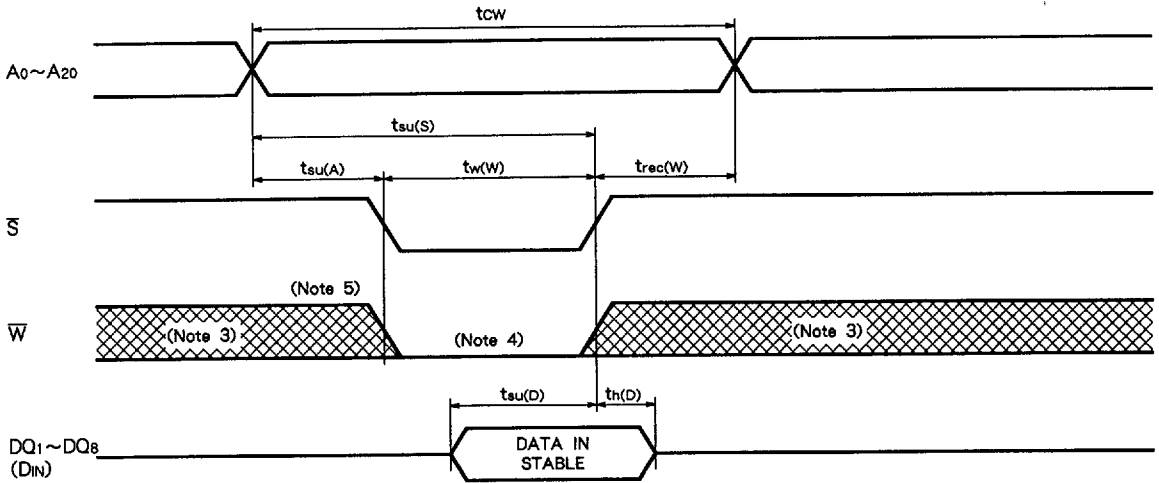


# MH2M08ATNA

16777216-BIT

(2097152-WORD BY 8-BIT) CMOS STATIC RAM

### Write cycle ( $\bar{S}$ control)



- Note 3. Hatching indicates the state is don't care.
- 4. Writing is executed in overlap of  $\bar{S}$  and  $\bar{W}$  low.
- 5. If  $\bar{W}$  goes low simultaneously with or prior to  $\bar{S}$ , the output remains in the high, impedance state.
- 6. Don't active inverted phase signal externally when DQ pin is in output mode.

### POWER DOWN CHARACTERISTICS

#### ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V <sub>CC(PD)</sub>	Power down supply voltage		2			V	
V <sub>I(S)</sub>	Chip select input $\bar{S}$	2.2V ≤ V <sub>CC(PD)</sub>	2.2			V	
		2V ≤ V <sub>CC(PD)</sub> ≤ 2.2V			V <sub>CC(PD)</sub>		
I <sub>CC(PD)</sub>	Power down supply current	V <sub>CC</sub> =3V, $\bar{S} \geq V_{CC}-0.2V$ , A <sub>17</sub> ~A <sub>20</sub> ≤ 0.2V or ≥ V <sub>CC</sub> -0.2V other inputs=0~V <sub>CC</sub>	-L			800	μA
			-H			160 (Note 8)	

- Note 7. When  $\bar{S}$  is at 2.2V(V<sub>IH</sub> min) and supply voltage is at any level between 4.5V and 2.4V, supply current is defined as I<sub>CC4</sub>.
- 8. I<sub>CC(PD)</sub> = 21 μA in case of Ta = 25°C.

### TIMING REQUIREMENTS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>su(PD)</sub>	Power down set up time		0			ns
t <sub>rec(PD)</sub>	Power down recovery time		5			ms

### POWER DOWN CHARACTERISTICS

