PRELIMINARY

256Kx4 Dynamic RAM CMOS, Monolithic

The EDI44256C is a high performance, low power CMOS Dynamic RAM organized as 256Kx4. The use of triple-layer polysilicon process, combined with silicide technology and a single transistor dynamic storage cell, provide high circuit density with high performance.

The use of dynamic circuitry, including sense amplifiers, assures low power dissipation.

Multiplexed address inputs permit a low pin count for maximum system density.

In addition to the RAS\-only refresh mode, the hidden refresh mode and CAS\ before RAS\ refresh mode are available.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Military product compliant to MIL-STD-883, paragraph 1.2.1, is available.

Features

256Kx4 bit CMOS Dynamic Random Access Memory

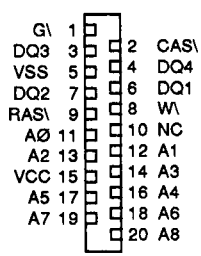
- Access Times 70, 80, 100, 120, and 150ns
- Low Operating Power Dissipation
- Low Standby Power
- Common I/O
- All Inputs/Outputs TTL Compatible

Package Styles

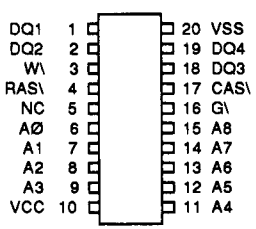
- 20 Pin DIP, No. 4
- 20(26) Lead Ceramic SOJ, No. 16
- 20 pin Ceramic ZIP, No.18

Single +5V (±10%) Supply Operation

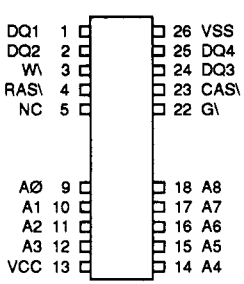
Pin Configurations and Block Diagram



ZIP



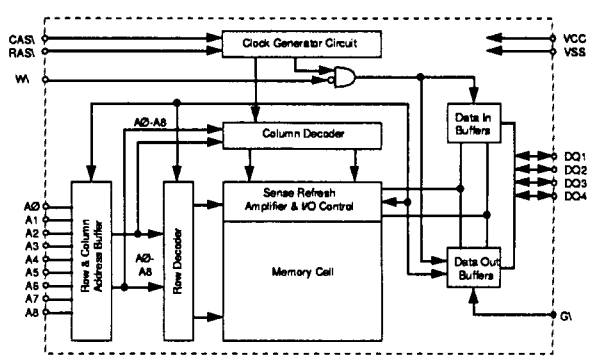
DIP



CSOJ

Pin Names

AØ-A8	Address Inputs
CAS\	Column Address Strobe
RAS\	Row Address Strobe
W\	Write Control Input
G\	Output Enable
DQ1-DQ4	Data Inputs/Outputs
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -1.0V to 7.0V
Operating Temperature TA (Ambient)
Military..... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation..... 1 Watt
Output Current..... 50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

(Note 1)

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.4	--	6.5	V
Input Low Voltage	VIL	-1.0	--	0.8	V

Notes: 1. All voltage values are with respect to VSS.

Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%) Note 2.

Parameter	Sym	Conditions	ns	Min	Typ	Max	Units
Average Supply Current from VCC Operating (Notes 3, 4)	ICC1	RAS\, CAS\ Cycling TRC = TWC = Min, Output Open	70			80	mA
			80			70	mA
			100			60	mA
			120			60	mA
			150			55	mA
Supply Current from VCC Standby	ICC2	RAS\ = CAS\ = VIH, Outputs Open				2	mA
		RAS\ = CAS\ ≥ VCC-0.5, Outputs Open				0.5	mA
Average Supply Current from VCC Refreshing (Note 3)	ICC3	RAS\ Cycling, CAS\ = VIH TRC = Min, Outputs Open	70			80	mA
			80			70	mA
			100			60	mA
			120			60	mA
			150			55	mA
Average Supply Current from VCC Fast Page Mode (Notes 3, 4)	ICC4	RAS\ = VIL, CAS\ = Cycling TPC = Min, Outputs Open	70			70	mA
			80			60	mA
			100			50	mA
			120			45	mA
			150			35	mA
Average Supply Current from VCC CAS\ before RAS\ Refresh Mode (Note 3)	ICC6	CAS\ before RAS\ Refresh Cycling TRC = Min Outputs Open	70			80	mA
			80			70	mA
			100			60	mA
			120			60	mA
			150			55	mA
Input Current	II	0V ≤ VIN ≤ 6.5V All Other Input Pins = 0V		-10		10	µA
Off-State Output Current	IOZ	Q Floating 0V≤ V OUT ≤ 5.5V		-10		10	µA
Output High Voltage	VOH	IOH = -5mA		2.4	—	VCC	V
Output Low Voltage	VOL	IOL= 4.2mA		0	—	0.4	V

Notes: 2. Current flowing into an IC is positive, out is negative.
3. ICC1(av), ICC3(av), ICC4(av), and ICC6 are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. ICC1(av), and ICC4(av) are dependent on output loading. Specified values are obtained with the output open.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Test Conditions	Min	Typ	Max	Unit
Address Input Capacitance	CA	VI = VSS			6	pF
Input Capacitance (D)	CD	f = 1MHz			6	pF
Input Capacitance (CAS\,W\, RAS\)	CC, CW, CR	Vi = 25mVrms			7	pF
Output Capacitance (Q)	CQ	VO = VSS, f = 1MHz, Vi = 25mVrms			7	pF

Input Conditions for Each Mode

The EDI44256C provides, in addition to normal Read, Write, and Read-modify-Write operations, a number of other functions, e.g. Fast Page Mode, RAS\-only Refresh, and Delayed Write. The input conditions for each are shown below.

ACT = Active
NAC= Non-active
DNC= Don't care
VLD = Valid
APD = Applied
OPN = Open

Operation	Inputs						Input/Output		Refresh
	RAS\	CAS\	W\	G\	Row Address	Column Address	D	Q	
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	Yes*
Early Write	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	Yes*
Read-Modify-Write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	Yes*
RAS\-only Refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	Yes
Hidden Refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	Yes
CAS\ before RAS\ Refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	Yes
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	No

* Fast Page Mode Identical.

Switching Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%) Note 5.

Parameter	Sym	70ns		80ns		100ns		120ns		150ns		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from CAS\	TCAC		20		20		25		30		40	ns	6, 7
Access Time From RAS\	TRAC		70		80		100		120		150	ns	6, 8
Column Address Access Time	TCAA		35		40		50		55		70	ns	6, 9
Access Time from CAS\ Precharge	TCPA		40		45		55		60		75	ns	6, 10
Access Time from G\	TOEA		20		20		25		30		40	ns	6
Output Low Impedance Time from CAS\ low	TCLZ	5		5		5		5		5		ns	6
Output Disable Time after CAS\ High	TOFF	0	20	0	20	0	25	0	30	0	35	ns	11
Output Disable Time after G\ High	TDISOE	0	20	0	20	0	25	0	30	0	35	ns	11

Notes: 5. An initial pause of 500µs is required after power-up, followed by any 8 RAS\ or RAS\-CAS\ cycles before proper device operation is achieved. Note that RAS\ may be cycled during the initial pause. Any 8 RAS\ or RAS\-CAS\ cycles are required after prolonged periods of RAS\ inactivity before proper device operation.

6. Measured with a load circuit equivalent to 2TTL loads and 100pF.
7. Assume that TRCD(max) ≤ TRAD and TRAD(max) ≥ TRAD.
8. Assume that TRCD ≤ TRCD(max) and TRAD ≤ TRAD(max).
9. Assume that TRCD - TRAD ≤ TCAA(max) and TRCD ≥ TRCD(max).
10. Assume that TCP ≤ TCP(max) and TASC ≥ TASC(max).
11. TOFF(max) defines the time at which the output achieves the high impedance state (IOUT ≤ |±10µA|) and is not reference to VOH(min) or VOL(max).

Timing Requirements
Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%) Notes 12, 13

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Refresh Cycle	TREF		8		8		8	ms	
RAS\ Precharge Time	TRP	60		70		80		ns	
RAS\ to CAS\ Delay Time	TRCD	20	50	25	60	25	75	ns	14
Delay CAS\ High to RAS\ Low	TCRP	10		10		10		ns	15
CAS\ Precharge Time (Non Page Mode)	TCPN	30		35		35		ns	16
Column Address Delay from RAS\ Low	TRAD	15	35	20	40	20	50	ns	17
Row Address Set Up Time	TASR	0		0		0		ns	
Column Address Set Up Time	TASC	0	10	0	15	0	20	ns	18
Row Address Hold Time	TRAH	10		15		15		ns	
Column Address Hold Time	TCAH	15		20		20		ns	
Transition Time	TT	3	50	3	50	3	50	ns	19

Timing Requirements
Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%) Notes 12, 13

		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Refresh Cycle	TREF		8		8	ms	
RAS\ Precharge Time	TRP	90		100		ns	
RAS\ to CAS\ Delay Time	TRCD	25	95	30	115	ns	14
Delay CAS\ High to RAS\ Low	TCRP	10		10		ns	15
CAS\ Precharge Time (Non Page Mode)	TCPN	35		35		ns	16
Column Address Delay from RAS\ Low	TRAD	20	65	25	80	ns	17
Row Address Set Up Time	TASR	0		0		ns	
Column Address Set Up Time	TASC	0	25	0	30	ns	18
Row Address Hold Time	TRAH	15		20		ns	
Column Address Hold Time	TCAH	20		25		ns	
Transition Time	TT	3	50	3	50	ns	19

Notes: 12. The timing requirements are assumed TT = 5ns.
13. VIH(min) and VIL (max) are reference levels for measuring timing of input signals.
14. TRCD(max) is specified as a reference point only. If TRCD is less than TRCD(max), access time is TRAC. If TRCD is greater than TRCD(max), access time is defined as TCAC and TCAA as shown in notes 7, 9.
15. TCRP requirement is applicable for all RAS\-CAS\ cycles.
16. TCPN(min) is specified as TCPN(min) =TRCD(min) +TCRP(min) except for TCP of fast page mode cycle.
17. TRAD(max) is specified as a reference point only. If TRAD ≥ TRAD(max), access time is assumed byTCAA for read cycle.
18. TASC(max) is specified as a reference point only of address acess time.
19. TT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Cycle Time	TRC	140		160		190		ns	
RAS\ Low Pulse Width	TRAS	70	10,000	80	10,000	100	10,000	ns	
CAS\ Low Pulse Width	TCAS	20	10,000	20	10,000	25	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns	
Read Set Up Time before CAS\ Low	TRCS	0		0		0		ns	
Read Hold Time after CAS\ High	TRCH	0		0		0		ns	20
Read Hold Time after RAS\ High	TRRH	10		10		10		ns	20
Column Address to RAS\ Setup	TRAL	35		40		50		ns	
Precharge to CAS\ Active	TRPC	0		0		0		ns	
G\ Hold Time after CAS\ Low	THCLOE	20		20		25		ns	
G\ Hold Time after RAS\ Low	THRLOE	70		80		100		ns	
Delay Time, Data to G\ Low	TDOEL	0		0		0		ns	
Delay Time, G\ High to Data	TOEHD	15		15		20		ns	
CAS\ Hold Time after G\ Low	THOECH	20		20		25		ns	
RAS\ Hold Time after G\ Low	THOERH	20		20		25		ns	

Notes: 20. Either TRCH or TRRH must be satisfied for a read cycle.

Read and Refresh Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Cycle Time	TRC	220		260		ns	
RAS\ Low Pulse Width	TRAS	120	10,000	150	10,000	ns	
CAS\ Low Pulse Width	TCAS	30	10,000	40	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	120		150		ns	
RAS\ Hold Time after CAS\ Low	TRSH	30		40		ns	
Read Set Up Time before CAS\ Low	TRCS	0		0		ns	
Read Hold Time after CAS\ High	TRCH	0		0		ns	20
Read Hold Time after RAS\ High	TRRH	10		10		ns	20
Column Address to RAS\ Setup	TRAL	55		70		ns	
Precharge to CAS\ Active	TRPC	0		0		ns	
G\ Hold Time after CAS\ Low	THCLOE	30		35		ns	
G\ Hold Time after RAS\ Low	THRLOE	120		150		ns	
Delay Time, Data to G\ Low	TDOEL	0		0		ns	
Delay Time, G\ High to Data	TOEHD	25		30		ns	
CAS\ Hold Time after G\ Low	THOECH	30		35		ns	
RAS\ Hold Time after G\ Low	THOERH	25		35		ns	

Notes: 20. Either TRCH or TRRH must be satisfied for a read cycle.

Write Cycle, Early and Delayed Write

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write Cycle Time	TWC	140		160		190		ns	
RAS\ Low Pulse Width	TRAS	70	10,000	80	10,000	100	10,000	ns	
CAS\ Low Pulse Width	TCAS	20	10,000	20	10,000	25	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns	
Write Setup Time before CAS\ Low	TWCS	0		0		0		ns	22
Write Hold Time after CAS\ Low	TWCH	15		15		20		ns	
CAS\ Hold Time after Write Low	TCWL	20		20		25		ns	
RAS\ Hold Time after Write Low	TRWL	20		20		25		ns	
Write Pulse Width	TWP	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	
Data Hold Time after CAS\ Low	TDH	15		15		20		ns	
Delay Time, G\ High to Data	TDEHD	15		15		20		ns	
G\ Hold Time after Write Low	THWOE	15		15		20		ns	

Write Cycle, Early and Delayed Write

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write Cycle Time	TWC	220		260		ns	
RAS\ Low Pulse Width	TRAS	120	10,000	150	10,000	ns	
CAS\ Low Pulse Width	TCAS	30	10,000	40	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	120		150		ns	
RAS\ Hold Time after CAS\ Low	TRSH	30		40		ns	
Write Setup Time before CAS\ Low	TWCS	0		0		ns	22
Write Hold Time after CAS\ Low	TWCH	25		30		ns	
CAS\ Hold Time after Write Low	TCWL	30		40		ns	
RAS\ Hold Time after Write Low	TRWL	30		40		ns	
Write Pulse Width	TWP	20		25		ns	
Data Set up Time	TDS	0		0		ns	
Data Hold Time after CAS\ Low	TDH	25		30		ns	
Delay Time, G\ High to Data	TDEHD	25		30		ns	
G\ Hold Time after Write Low	THWOE	25		30		ns	

Read-Write and Read-Modify-Write Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-Modify-Write CycleTime	TRWC	185		205		245		ns	21
RAS\ Low Pulse Width	TRASRW	115	10,000	125	10,000	155	10,000	ns	
CAS\ Low Pulse Width	TCASRW	65	10,000	65	10,000	85	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSHRW	115		125		155		ns	
RAS\ Hold Time after CAS\ Low	TRSHRW	65		65		80		ns	
Read Setup time before CAS\ Low	TRCS	0		0		0		ns	
CAS\ Low to W\ Low Delay	TCWD	40		40		50		ns	22
RAS\ Low to W\ Low Delay	TRWD	90		100		125		ns	22
CAS\ Hold after W\ Low	TCWL	20		20		25		ns	
RAS\ Hold after W\ Low	TRWL	20		20		25		ns	
Write Pulse Width	TWP	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	
Data Hold Time after W\ Low	TDH	15		15		20		ns	
Address to W\ Low Delay	TAWD	55		60		75		ns	22
G\ Hold Time after CAS\ Low	THCLOE	20		20		25		ns	
G\ Hold Time after RAS\ Low	THRLOE	70		80		100		ns	
Delay Time, Data to G\ Low	TDOEL	0		0		0		ns	
Delay Time, G\ High to Data	TOEHD	15		15		20		ns	
G\ Hold Time after Write Low	THRWOE	15		15		20		ns	

Notes: 21. TRWC is specified as TRWC(min) = TRCD(max) + TCWD (min) +TRWL(min) + TRP(min) +4TT.

22. TWCS, TRWD, TCWD, and TAWD do not define the limits of operation, but are included as electrical characteristics only. When TWCS ≥ TWCS(min), an early write cycle is performed, and the data output keeps the high-impedance state. When TRWD ≥ TRWD(min), TCWD ≥ TCWD(min) and TAWD ≥ TAWD(min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of Q (at the access time and until CAS\ goes back to VIH) is indeterminate.

Read-Write and Read-Modify-Write Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-Modify-Write CycleTime	TRWC	290		330		ns	21
RAS\ Low Pulse Width	TRASRW	165	10,000	215	10,000	ns	
CAS\ Low Pulse Width	TCASRW	85	10,000	105	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSHRW	175		190		ns	
RAS\ Hold Time after CAS\ Low	TRSHRW	85		80		ns	
Read Setup time before CAS\ Low	TRCS	0		0		ns	
CAS\ Low to W\ Low Delay	TCWD	55		65		ns	22
RAS\ Low to W\ Low Delay	TRWD	145		175		ns	22
CAS\ Hold after W\ Low	TCWL	30		40		ns	
RAS\ Hold after W\ Low	TRWL	30		40		ns	
Write Pulse Width	TWP	20		25		ns	
Data Set up Time	TDS	0		0		ns	
Data Hold Time after W\ Low	TDH	20		25		ns	
Address to W\ Low Delay	TAWD	85		95		ns	22
G\ Hold Time after CAS\ Low	THCLOE	30		35		ns	
G\ Hold Time after RAS\ Low	THRLOE	120		150		ns	
Delay Time, Data to G\ Low	TDOEL	0		0		ns	
Delay Time, G\ High to Data	TOEHD	25		30		ns	
G\ Hold Time after Write Low	THRWOE	25		30		ns	

Notes: 21. TRWC is specified as TRWC(min) = TRCD(max) + TCWD (min) +TRWL(min) + TRP(min) +4TT.

22. TWCS, TRWD, TCWD, and TAWD do not define the limits of operation, but are included as electrical characteristics only. When TWCS ≥ TWCS(min), an early write cycle is performed, and the data output keeps the high-impedance state. When TRWD ≥ TRWD(min), TCWD ≥ TCWD(min) and TAWD ≥ TAWD(min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of Q (at the access time and until CAS\ goes back to VIH) is indeterminate.

Fast Page Mode Cycle

Read, Early Write, Read-Write, Read-Modify-Write Cycles

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast Page Mode Cycle Time	TPC	45		50		60		65		80		ns	
Fast Page Mode for R/W, R/M/W Cycle Time	TRWPC	95		100		115		135		165		ns	
RAS\ Low Pulse Width for Read, Write Cycle	TRASP	115	50,000	130	50,000	160	50,000	185	50,000	230	50,000	ns	
CAS\ Low Pulse Width for Read Cycle	TCAS	20	10,000	20	10,000	25	10,000	30	10,000	40	10,000	ns	
CAS\ Pulse Width (Page Mode)	TCP	10	25	10	25	10	25	10	25	10	25	ns	23
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		30		40		ns	

Note: 23. TCP (Max) is specified as a reference point only. If TCP (Max) ≤ TCP, access time is assumed by TCAC.

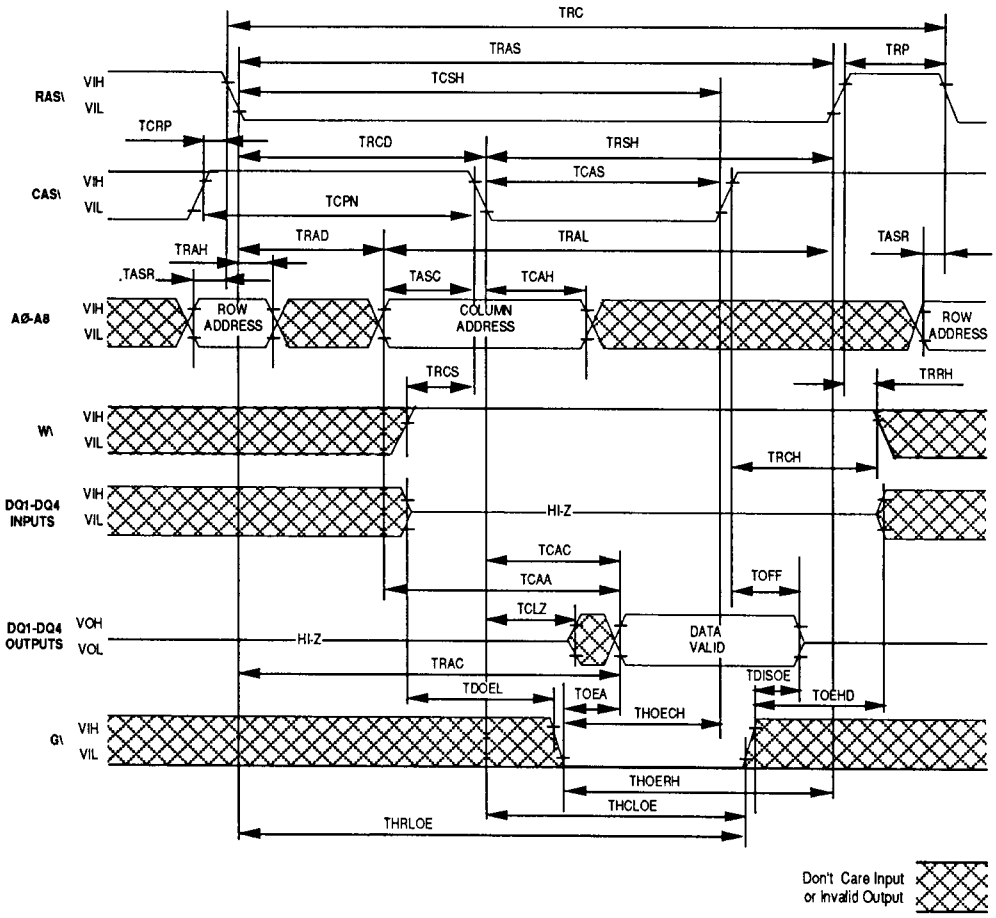
CAS\ before RAS\ Refresh Cycle

(TA = -55°C to +125°C; VCC = 5.0V±10%)

		70ns		80ns		100ns		120ns		150ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
CAS\ Setup for CAS\ before RAS\ Refresh	TCSR	10		10		10		10		10		ns	24
CAS\ Hold for CAS\ before RAS\ Refresh	TCHR	15		15		20		25		30		ns	24
Precharge to CAS\ Active	TRPC	0		0		0		0		0		ns	24

Note: 24. Eight or more CAS\ before RAS\ cycles are necessary for proper operation of CAS\ before RAS\ refresh mode.

Read Cycle


TRC
TRAS
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COLUMN ADDRESS
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DQ1-DQ4 INPUTS
HI-Z
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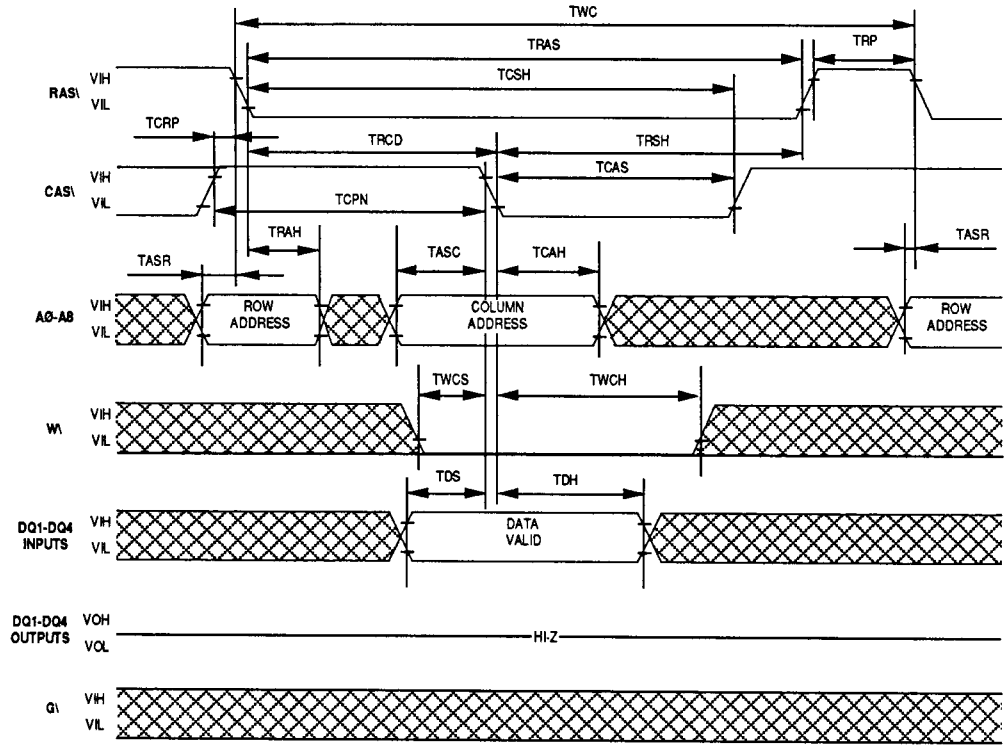
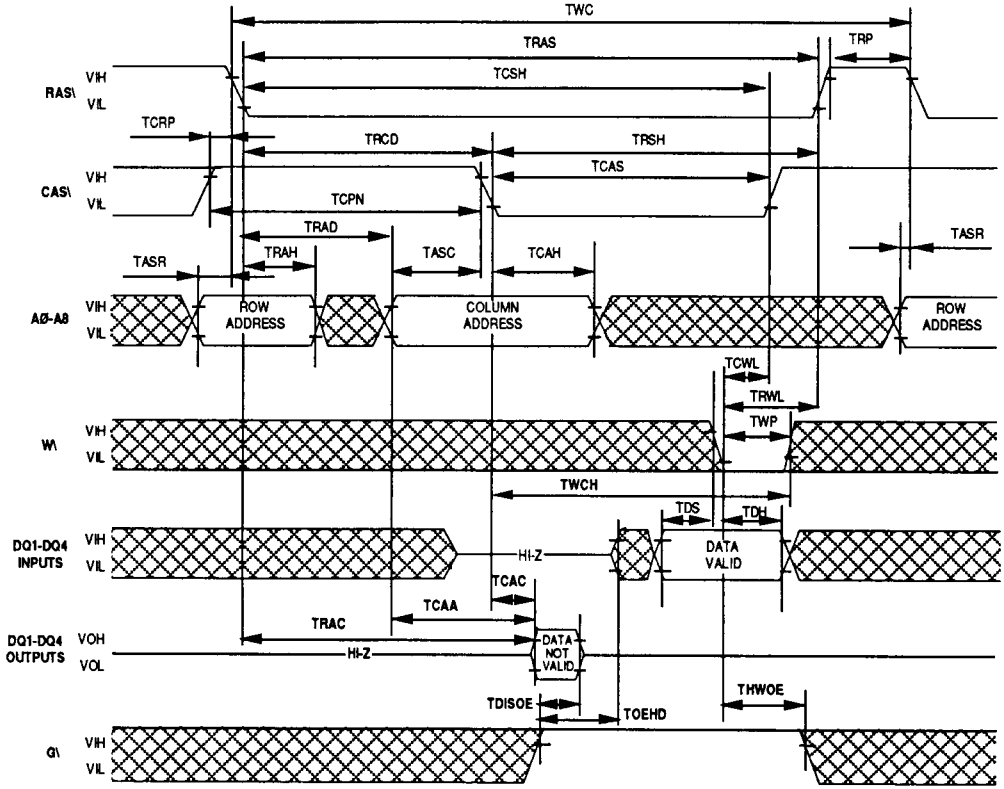
TCAA
TOFF
TCLZ
DQ1-DQ4 OUTPUTS
VOH
VOL
HI-Z
DATA VALID
TRAC
TDISOE
TDOEL
TOEA
TOEHD
THOECH
G\
THOERH
THCLOE
THRLOE
Don't Care Input or Invalid Output

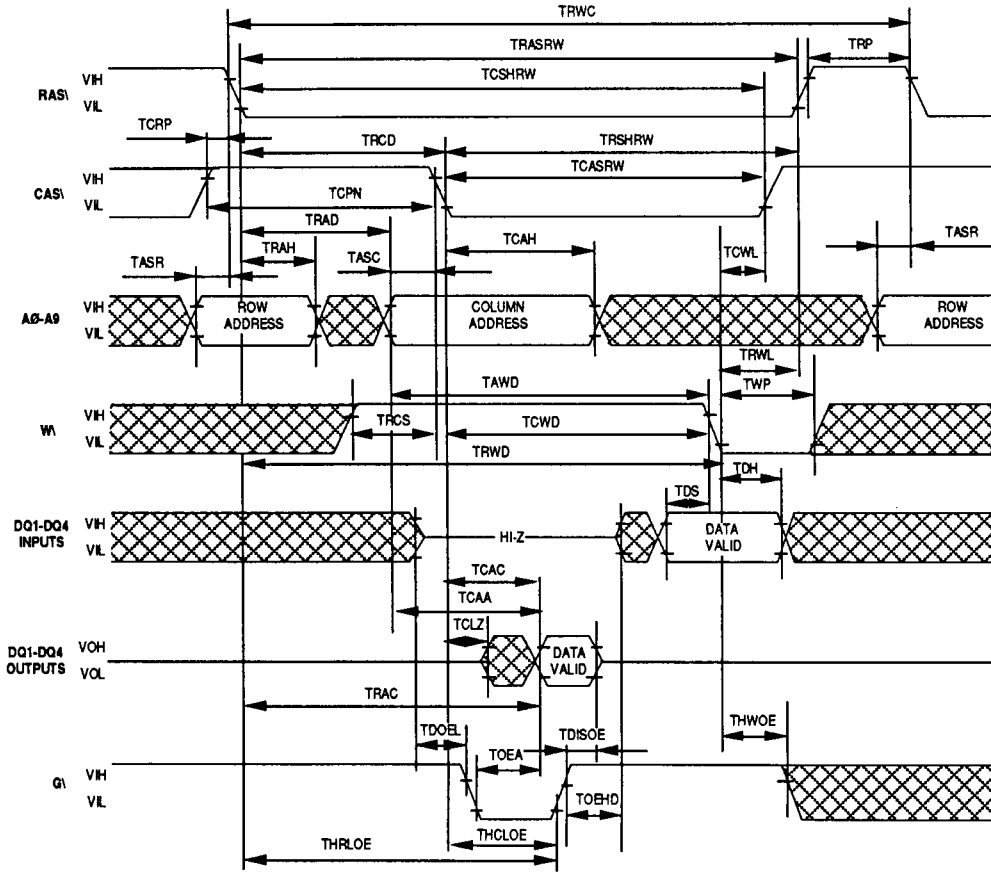
Write Cycle, Early Write



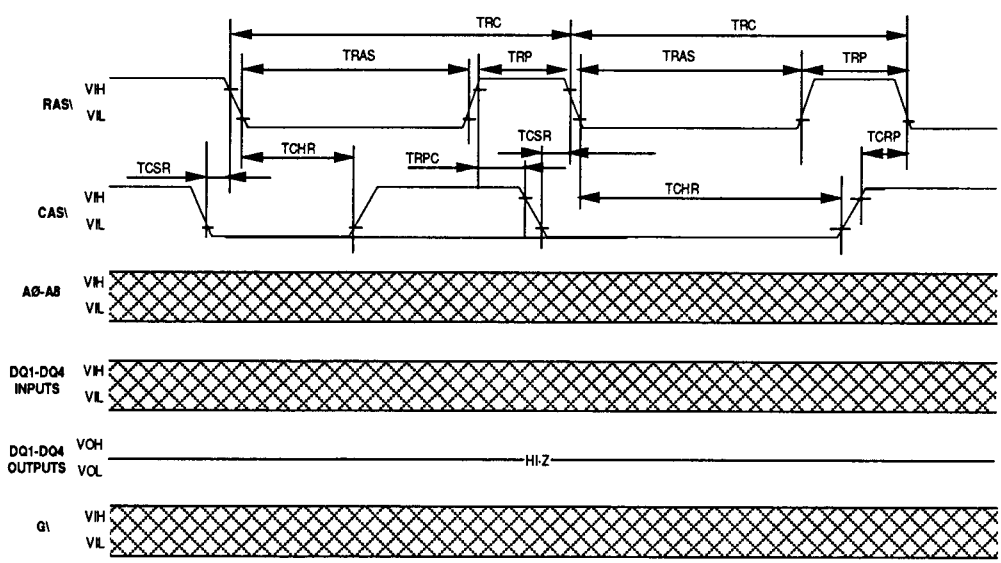
Write Cycle, Delayed Write



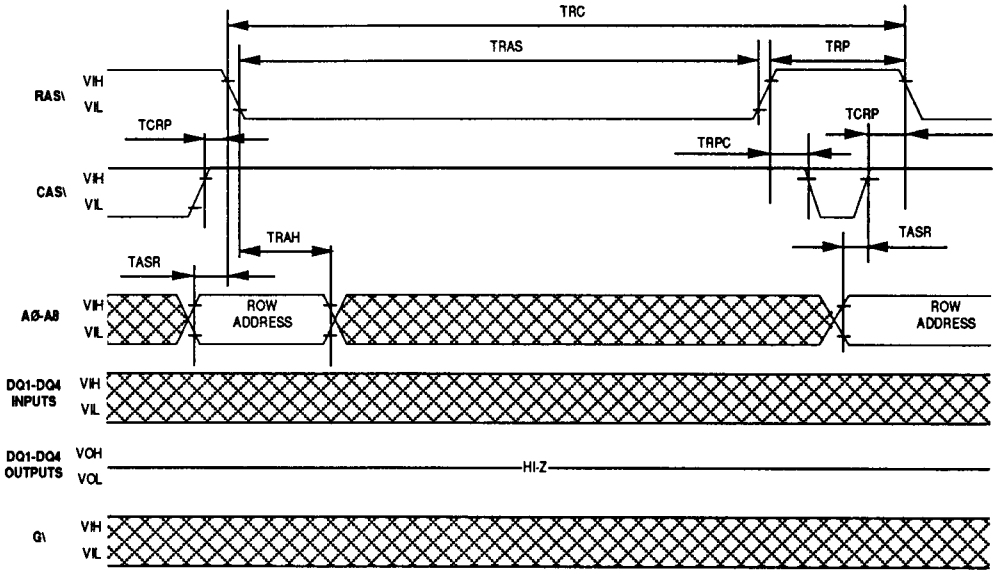
Read-Write, Read-Modify-Write Cycle



CAS\ before RAS\ Refresh Cycle *Note 25*

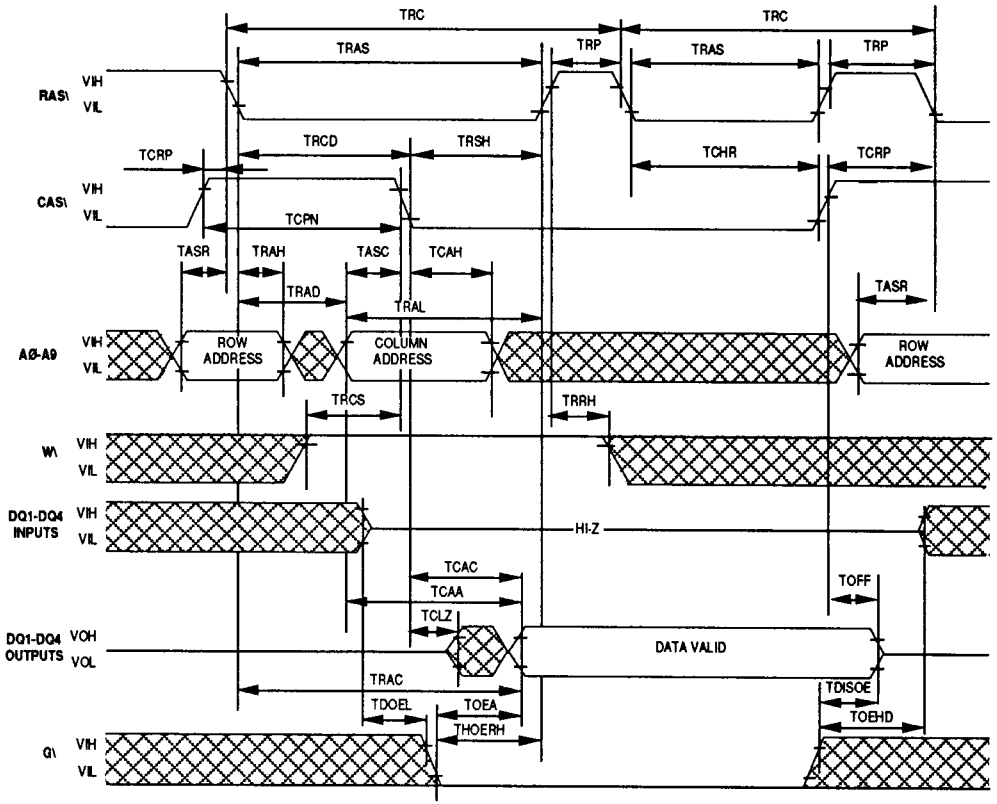


RAS\-only Refresh Cycle *Note 25*

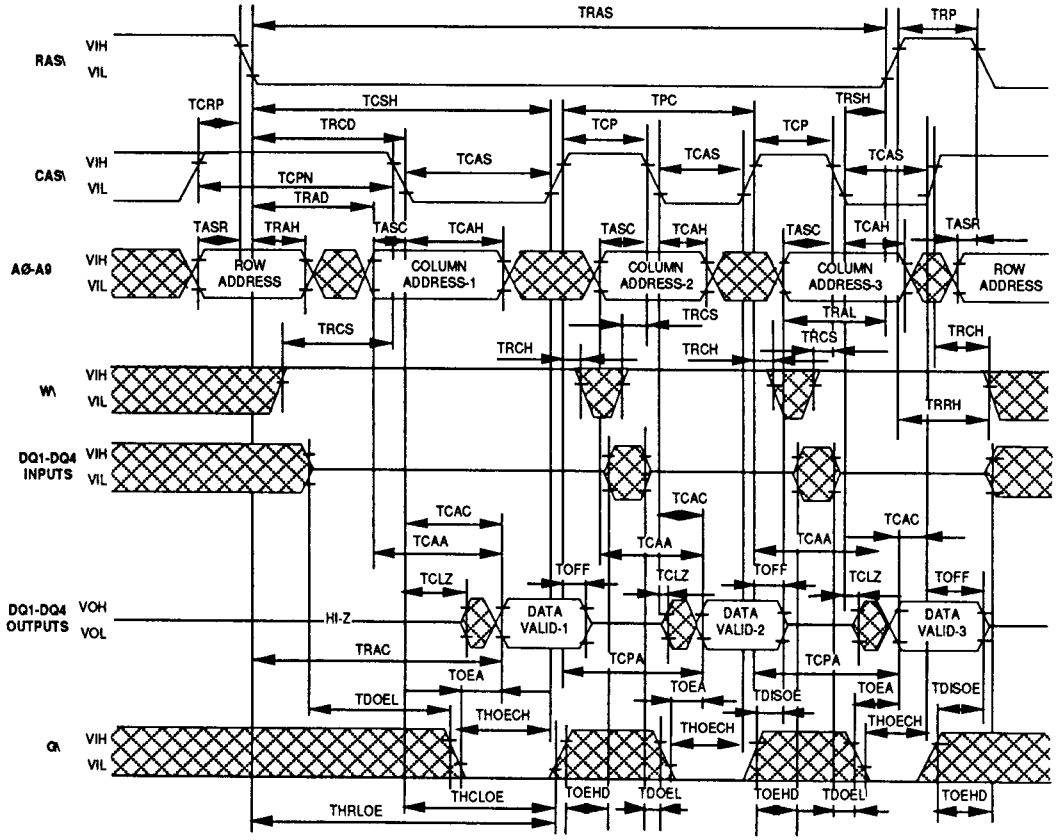


Note: 25. W\ Don't care

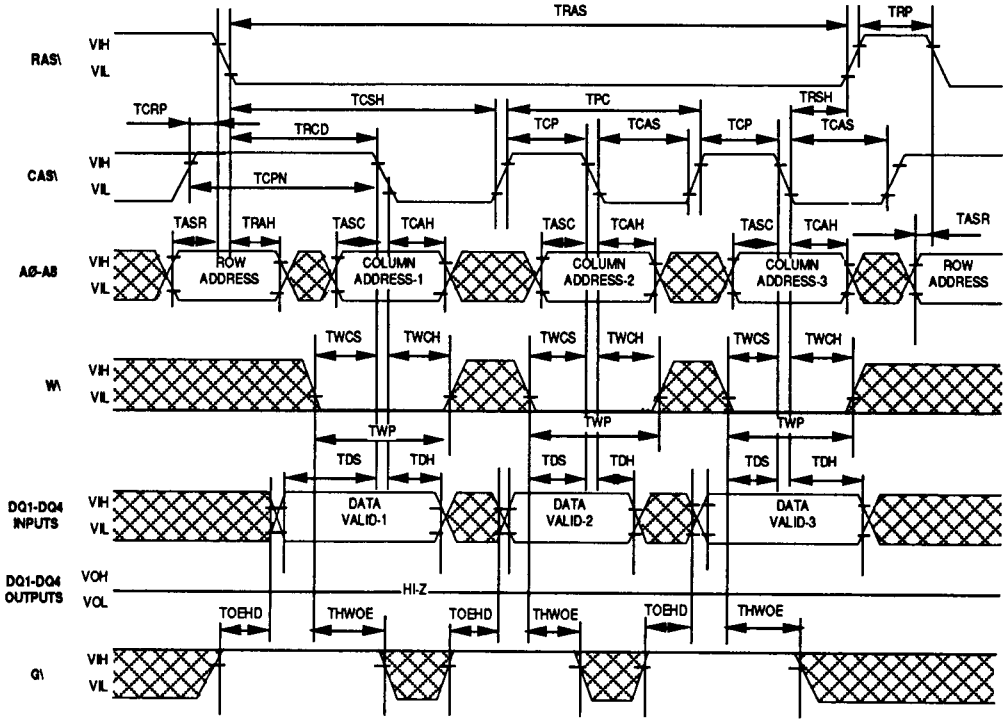
Hidden Refresh Cycle



Fast-Page-Mode, Read Cycle



Fast-Page-Mode, Early Write Cycle



Fast-Page-Mode Read-Write, Read-Modify-Write Cycle