Ordering number : EN※4541A

CMOS LSI

No. ※4541A

SANYO

LC331632M-70/80/10/12, ML-70/80/10

512 K (32768 words × 16 bits) Pseudo-SRAM

Preliminary

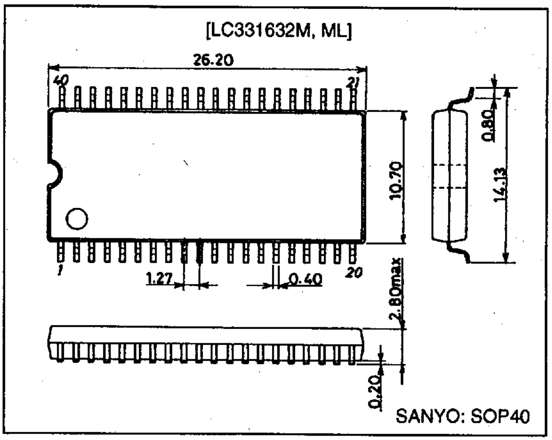
Overview

The LC331632 series is composed of pseudo static RAM that operate on a single 5 V power supply and are organized as 32768 words × 16 bits. By using memory cells each composed of a single transistor and capacitor, together with peripheral CMOS circuitry, this series achieves ease of use with high density, high speed, and low power dissipation. The LC331632 series can easily accomplish auto-refresh by means of $\overline{\text{LOE}}/\overline{\text{RFSH}}$ input. The available package is the 40-pin SOP with a width of 525 mil.

Package Dimensions

unit: mm

3195-SOP40



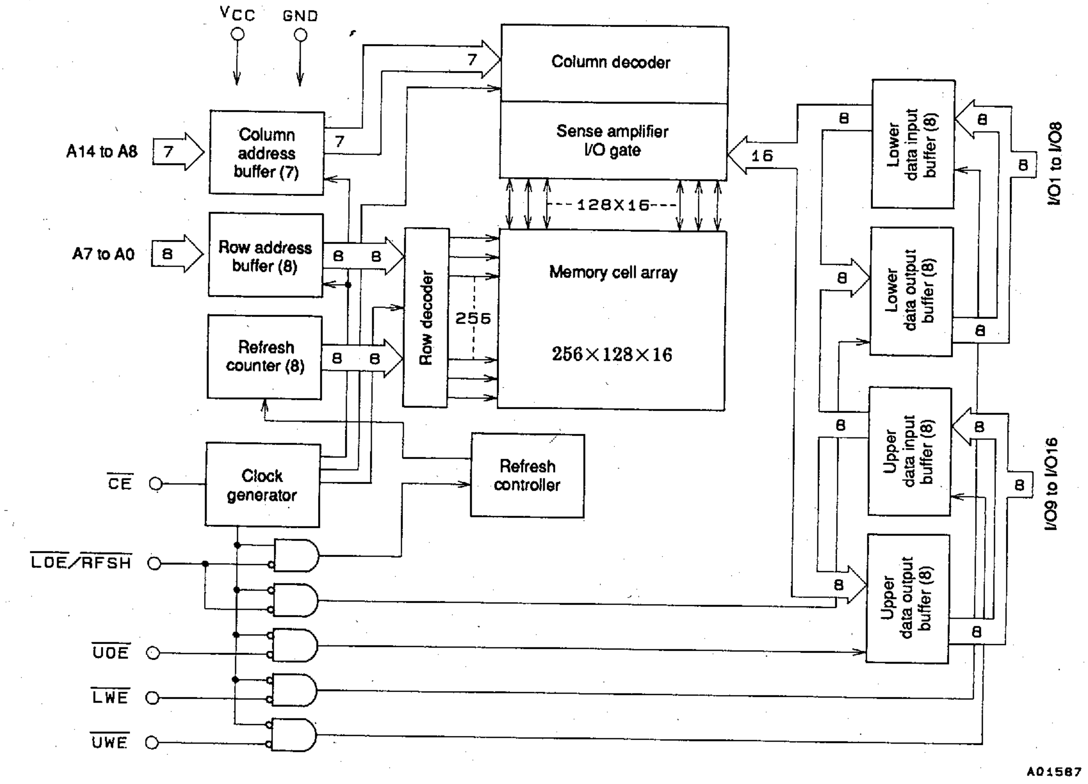
Features

- 32768 words × 16 bits configuration
- $\overline{\text{CE}}$ access time, $\overline{\text{OE}}$ access time, cycle time and current dissipation

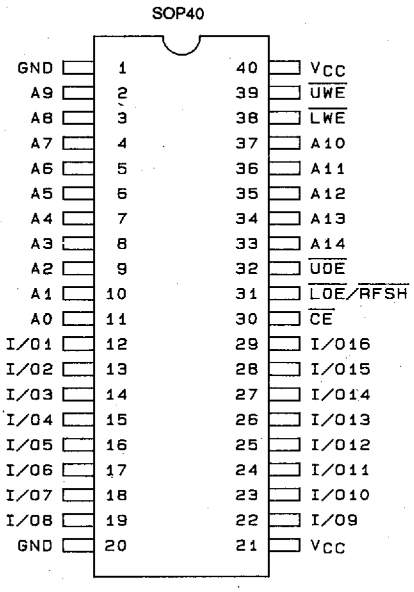
Parameter		LC331632M, ML			
		-70	-80	-10	-12
$\overline{\text{CE}}$ access time		70 ns	80 ns	100 ns	120 ns
$\overline{\text{OE}}$ access time		35 ns	40 ns	50 ns	75 ns
Cycle time		115 ns	130 ns	160 ns	210 ns
Current dissipation	Operating	100 mA	90 mA	75 mA	65 mA
	Standby	2 mA/100 µA (L version)			

- Single 5 V ±10% power supply
- All input and output (I/O) TTL compatible
- Fast access time and low power dissipation
- 4 ms refresh using 256 refresh cycles
- Supports $\overline{\text{CE}}$-only refresh and auto-refresh
- Supports byte unit read and write operations using the $\overline{\text{LOE}}/\overline{\text{RFSH}}$ and $\overline{\text{UOE}}$ inputs or the $\overline{\text{LWE}}$ and $\overline{\text{UWE}}$ inputs.
- Low-power version: 100 µA standby current
- 40-pin SOP plastic package

Block Diagram



Pin Assignment



Top View

Pin Functions

A0 to A14	Address input
$\overline{LWE}$	Lower byte write enable input
$\overline{UWE}$	Upper byte write enable input
$\overline{LOE}/\overline{RFSH}$	Lower byte output enable input/refresh input
$\overline{UOE}$	Upper byte output enable input
$\overline{CE}$	Chip enable input
I/O1 to I/O8	Lower byte data input/output
I/O9 to I/O16	Upper byte data input/output
V_{CC}	Power supply
GND	Ground

Functional Logic

$\overline{CE}$	$\overline{LOE}$ /RFSH	$\overline{UOE}$	$\overline{LWE}$	$\overline{UWE}$	A0 to 7	A8 to 14	I/O1 to 8	I/O9 to 16	State
H	H	X	X	X	X	X	HZ	HZ	Standby
L	L	L	H	H	VX	VX	OUT	OUT	Read (word)
L	L	H	H	H	VX	VX	OUT	HZ	Read (lower byte)
L	H	L	H	H	VX	VX	HZ	OUT	Read (upper byte)
L	H	H	L	L	VX	VX	IN	IN	Write (word)
L	H	H	L	H	VX	VX	IN	HZ	Write (lower byte)
L	H	H	H	L	VX	VX	HZ	IN	Write (upper byte)
L	H	H	H	H	VX	X	HZ	HZ	$\overline{CE}$-only refresh
H	NP	X	X	X	X	X	HZ	HZ	Auto-refresh

H: High-level input of V_{IN} = 6.5 V to V_{IH} (min)
L: Low-level input of V_{IN} = V_{IL} (max) to –1.0 V
X: High- or low-level input
NP: Negative-polarity pulse input
VX: "IN" when $\overline{CE}$ = L is confirmed, then "X"
HZ: High impedance
IN: Input state
OUT: Output state

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	V_{CC} max	–1.0 to +7.0	V	1
Input voltage	V_{IN}	–1.0 to +7.0	V	1
Output voltage	V_{OUT}	–1.0 to +7.0	V	1
Allowable power dissipation	Pd max	600	mW	1
Output short current	I_{OUT}	50	mA	1
Operating temperature range	Topr	0 to +70	°C	1
Storage temperature range	Tstg	–55 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage	V_{IL}	–1.0		+0.8	V	2

Note: 2. All voltages are referenced to GND.

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5V±10%

Parameter	Symbol	Conditions			min	max	Unit	Note
Operating current (Average current during operation)	I_{CCA}		Cycle time	115 ns		100	mA	3, 4
				130 ns		90		
				160 ns		75		
				210 ns		65		
Standby current 1	I_{CCS1}	$\overline{CE}$ = $\overline{LOE}$/RFSH = V_{IH}	LC331632M			3	mA	
			LC331632ML			1	mA	
Standby current 2	I_{CCS2}	$\overline{CE}$ = $\overline{LOE}$/RFSH = V_{CC} – 0.2 V	LC331632M			2	mA	
			LC331632ML			100	µA	
Input leakage current	I_{IL}	0 V ≤ V_{IN} ≤ V_{CC}, pins other than measuring pin = 0 V			–10	+10	µA	
Output leakage current	I_{OL}	Output disable, 0 V ≤ V_{OUT} ≤ V_{CC}			–10	+10	µA	
Output high level voltage	V_{OH}	I_{OUT} = –1 mA			2.4		V	
Output low level voltage	V_{OL}	I_{OUT} = 4.2 mA				0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller. A bypass capacitor of 0.01 µF or larger should be inserted between V_{CC} and GND for each memory chip to suppress power supply noise (voltage drops) due to transient currents.
4. Dependent on output load. Maximum value is value during free state.

Capacitance Characteristics at Ta = 25°C, f = 1 MHz, V_{CC} = 5 V ± 10%

Parameter	Symbol	Measuring Conditions	min	max	Unit
Input capacitance (A0 to A14)	C_{IN1}	$V_{IN1} = 0$ V		5	pF
Input capacitance ($\overline{\text{CE}}$, $\overline{\text{LOE}}$/$\overline{\text{RFSH}}$, $\overline{\text{UOE}}$, $\overline{\text{LWE}}$, $\overline{\text{UWE}}$)	C_{IN2}	$V_{IN2} = 0$ V		7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0$ V		10	pF

Sampling inspections, and not full-lot inspections, are carried out for these parameters.

AC Recommended Operating Ranges at Ta = 0 to +70°C, V_{CC} = 5 V ± 10% (Notes 5, 6, 7, 8, 9)

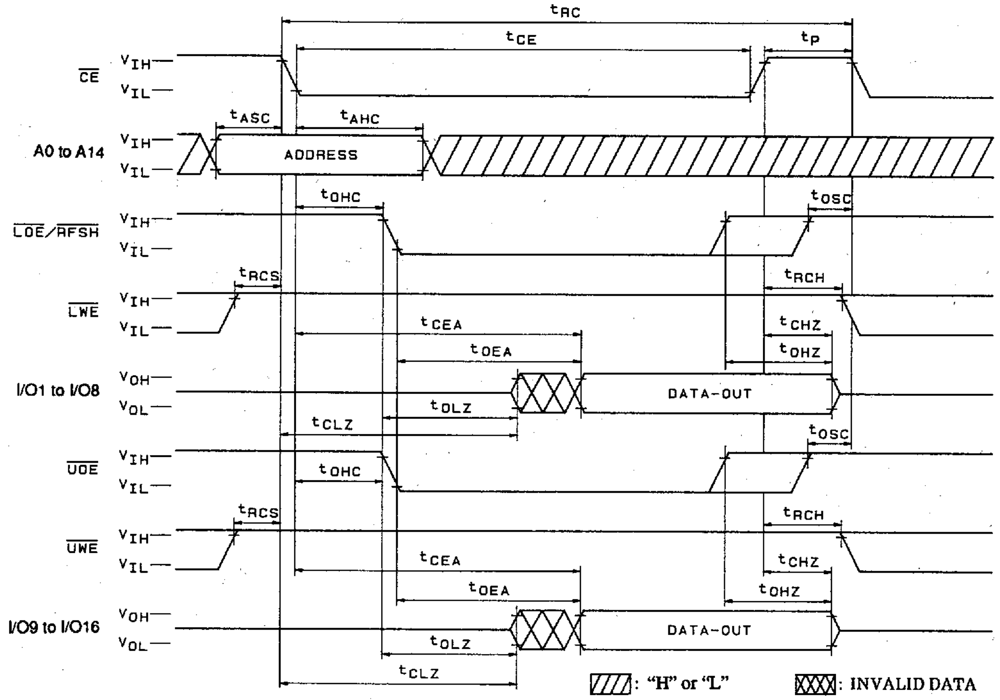
Parameter	Symbol	-70		-80		-10		-12		Unit	Note
		min	max	min	max	min	max	min	max		
Random read or write cycle time	t_{RC}	115		130		160		210		ns	
$\overline{\text{CE}}$ pulse width	t_{CE}	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{\text{CE}}$ precharge time	t_P	35		40		50		80		ns	
$\overline{\text{CE}}$ access time	t_{CEA}		70		80		100		120	ns	
$\overline{\text{LOE}}$, $\overline{\text{UOE}}$ access time	t_{OEA}		35		40		50		75	ns	
$\overline{\text{CE}}$ output enable time	t_{CLZ}	10		10		10		10		ns	
$\overline{\text{LOE}}$, $\overline{\text{UOE}}$ output enable time	t_{OLZ}	0		0		0		0		ns	
$\overline{\text{CE}}$ output disable time	t_{CHZ}	0	20	0	25	0	30	0	35	ns	10
$\overline{\text{LOE}}$, $\overline{\text{UOE}}$ output disable time	t_{OHZ}	0	20	0	25	0	30	0	35	ns	10
$\overline{\text{LOE}}$, $\overline{\text{UOE}}$ hold time for $\overline{\text{CE}}$	t_{OHC}	0		0		0		0		ns	
$\overline{\text{LOE}}$, $\overline{\text{UOE}}$ setup time for $\overline{\text{CE}}$	t_{OSC}	10		10		10		10		ns	
Read command setup time	t_{RCS}	0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		ns	
Write pulse width	t_{WP}	25		30		35		85		ns	
Write command hold time	t_{WCH}	55		60		65		85		ns	
Write command lead time	t_{CWL}	40		45		50		85		ns	
Input data setup time for $\overline{\text{LWE}}$, $\overline{\text{UWE}}$	t_{DSW}	25		30		35		50		ns	11
Input data setup time for $\overline{\text{CE}}$	t_{DSC}	25		30		35		50		ns	11
Input data hold time for $\overline{\text{LWE}}$, $\overline{\text{UWE}}$	t_{DHW}	0		0		0		0		ns	11
Input data hold time for $\overline{\text{CE}}$	t_{DHC}	0		0		0		0		ns	11
Address setup time for $\overline{\text{CE}}$	t_{ASC}	0		0		0		0		ns	12
Address hold time for $\overline{\text{CE}}$	t_{AHC}	15		20		25		30		ns	12
Auto-refresh cycle time	t_{FC}	115		130		160		210		ns	
$\overline{\text{RFSH}}$ delay time for $\overline{\text{CE}}$	t_{RFD}	35		40		50		60		ns	
$\overline{\text{RFSH}}$ pulse width (Auto-refresh)	t_{FAP}	75	8000	80	8000	80	8000	80	8000	ns	13
$\overline{\text{RFSH}}$ precharge time (Auto-refresh)	t_{FP}	30		30		30		30		ns	13
$\overline{\text{RFSH}}$ active $\overline{\text{CE}}$ delay time (Auto-Refresh)	t_{FCE}	135		160		190		225		ns	13
Refresh time	t_{REF}		4		4		4		4	ms	
Rise or fall time	t_T	3	50	3	50	3	50	3	50	ns	

Note: 5. To accomplish internal initialization, $\overline{\text{CE}}$ and $\overline{\text{LOE}}$/$\overline{\text{RFSH}}$ are fixed at V_{IH} for an interval of 1 ms when V_{CC} reaches the specified voltage after power is switched on. At least eight dummy cycles must be executed following that period.

6. Measured at $t_T = 5$ ns.
7. When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are refrence levels.
8. Measured using an equivalent of 100 pF and two standard TTL loads.
9. $\overline{\text{LOE}}$/$\overline{\text{RFSH}}$ input functions as lower byte output enable input ($\overline{\text{LOE}}$) when $\overline{\text{CE}} = V_{IL}$, and as refresh input ($\overline{\text{RFSH}}$) when $\overline{\text{CE}} = V_{IH}$.
10. t_{CHZ} and t_{OHZ} are defined as the time until output enters the open circuit state and the output voltage level becomes immeasurable.
11. As with ordinary static RAM, write data is incorporated at the rise of $\overline{\text{LWE}}$, $\overline{\text{UWE}}$ input or $\overline{\text{CE}}$ input, whichever is earlier, and write data is therefore held during t_{DSW}, t_{DSC}, t_{DHW}, or t_{DHC}.
12. Because address input is incorporated at the fall of $\overline{\text{CE}}$, the address is maintained during t_{ASC} or t_{AHC}.
13. After auto-refresh has completed, $\overline{\text{CE}}$ must not be made active until the t_{FCE} period has elapsed.

Timing Chart

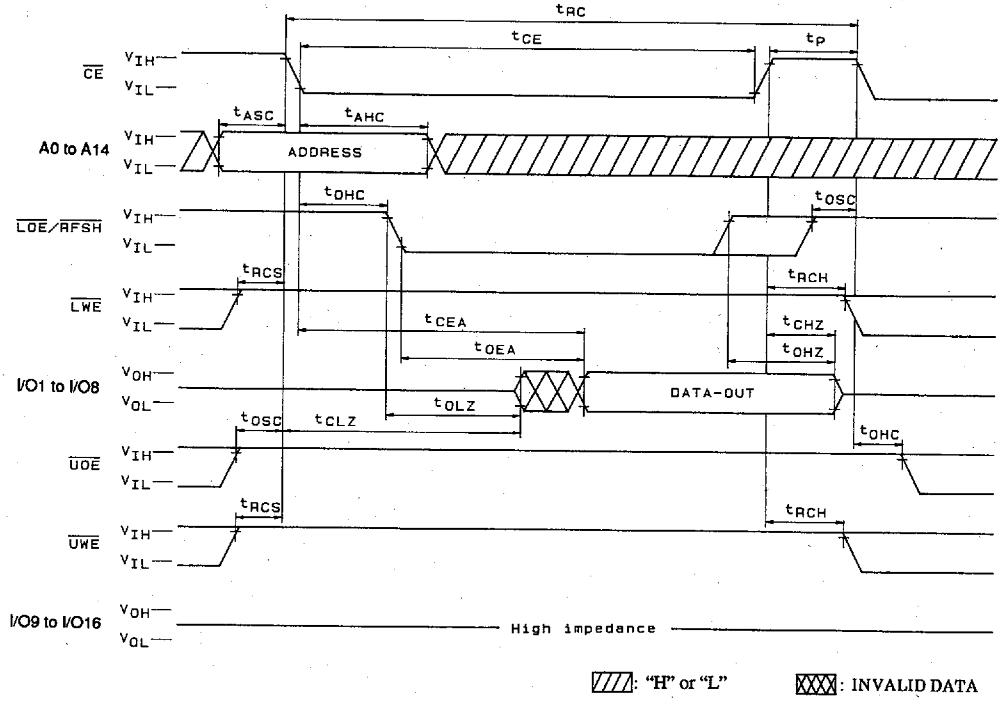
Read Cycle (word)



▨: "H" or "L" ⊠: INVALID DATA

A01589

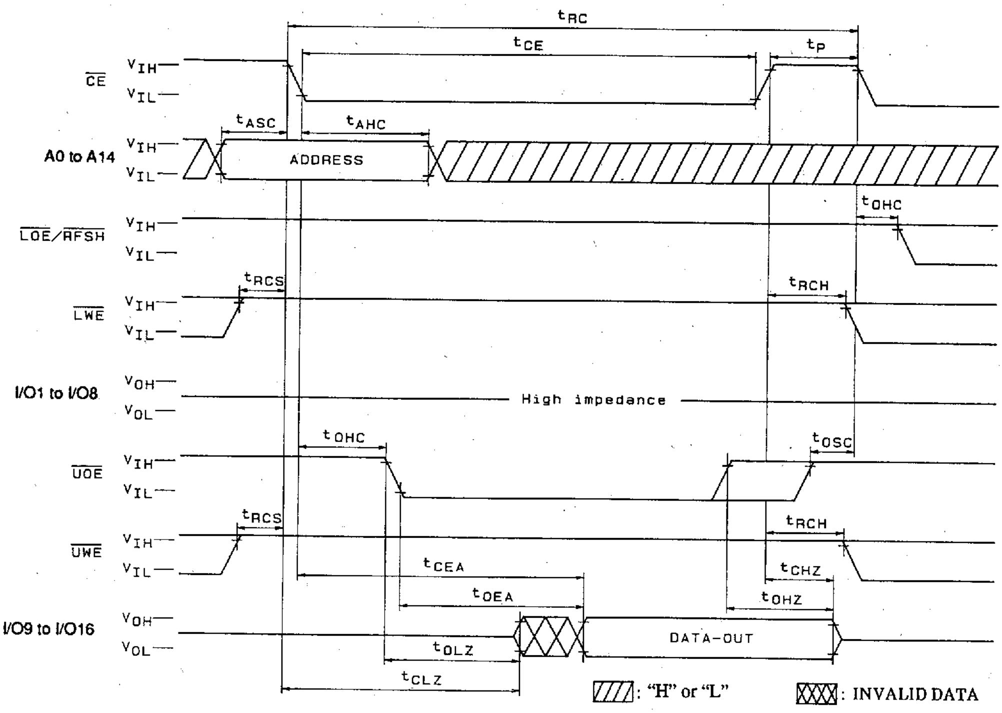
Read Cycle (lower byte)



▨: "H" or "L" ⊠: INVALID DATA

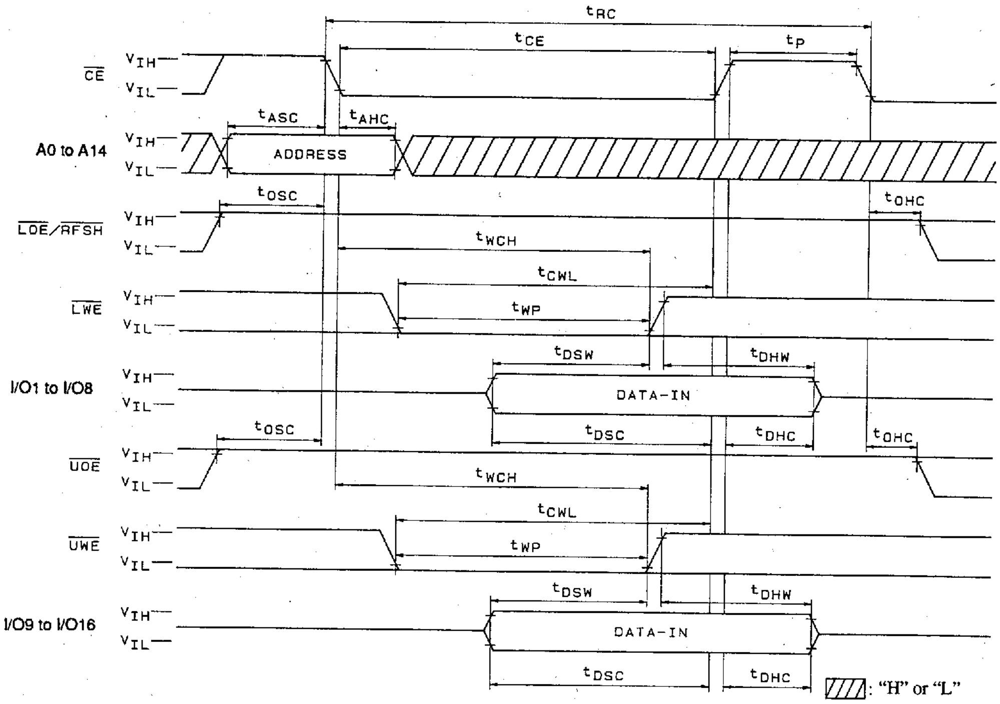
A01590

Read Cycle (upper byte)



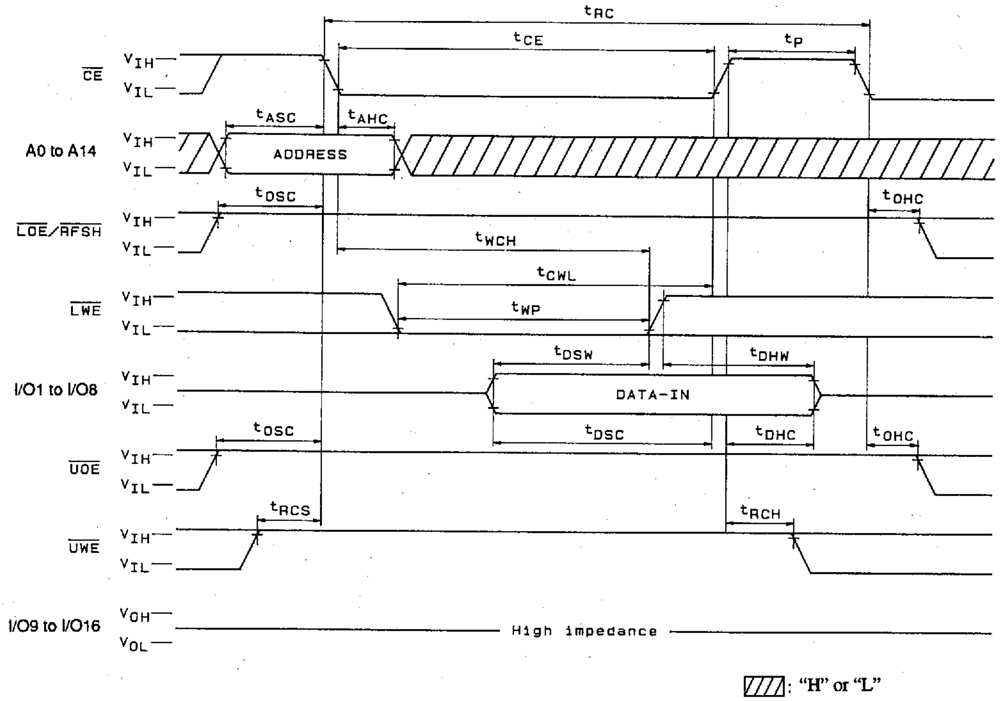
A01591

Write Cycle (word)



A01592

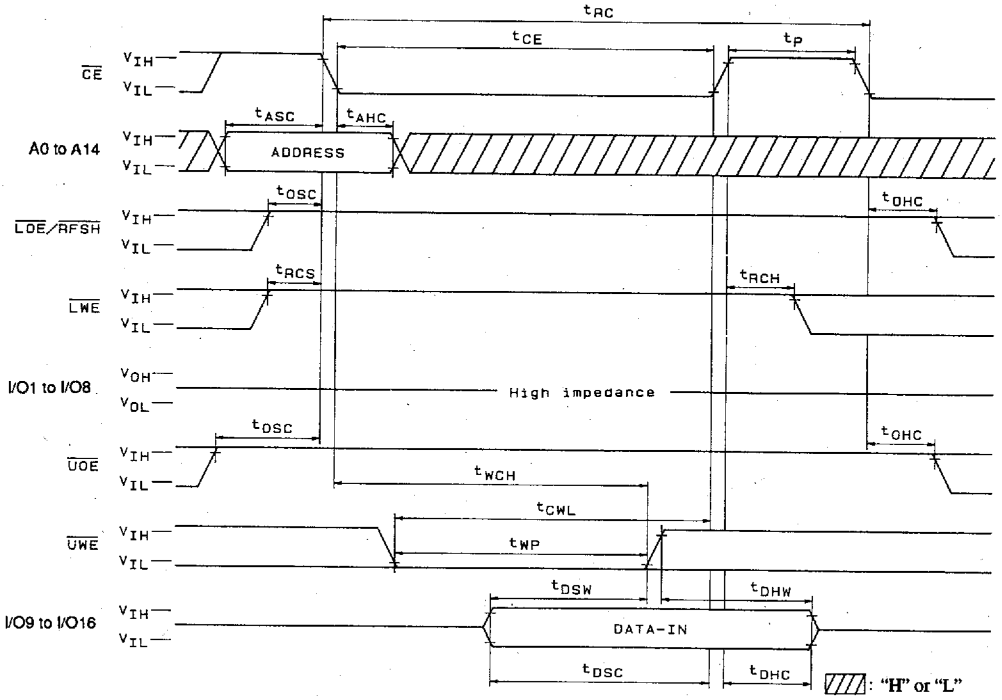
Write Cycle (lower byte)



▨: "H" or "L"

A01593

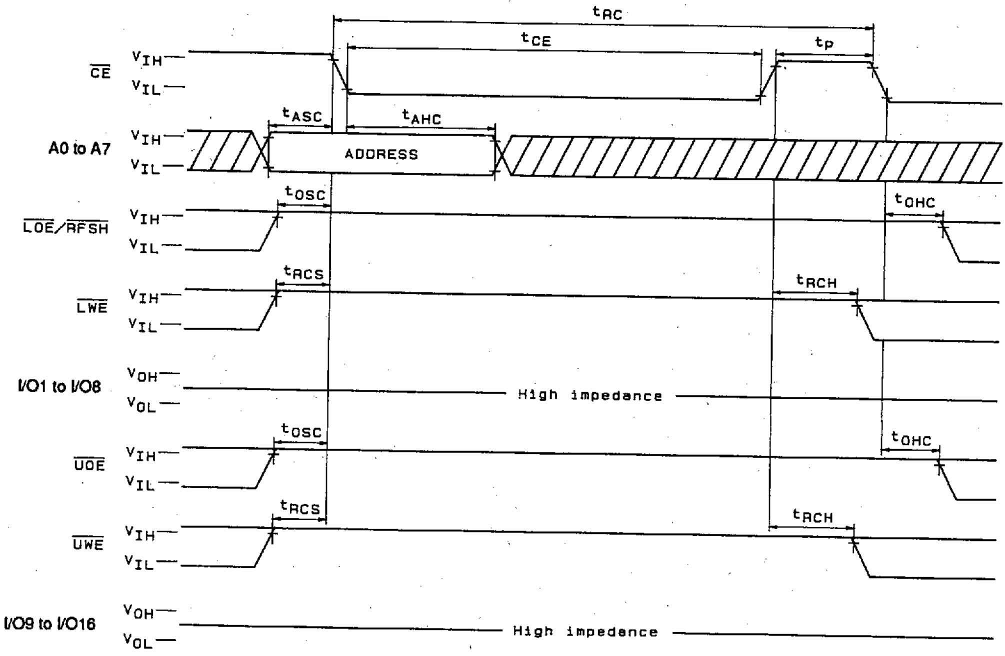
Write Cycle (upper byte)



▨: "H" or "L"

A01594

$\overline{CE}$-Only Refresh Cycle

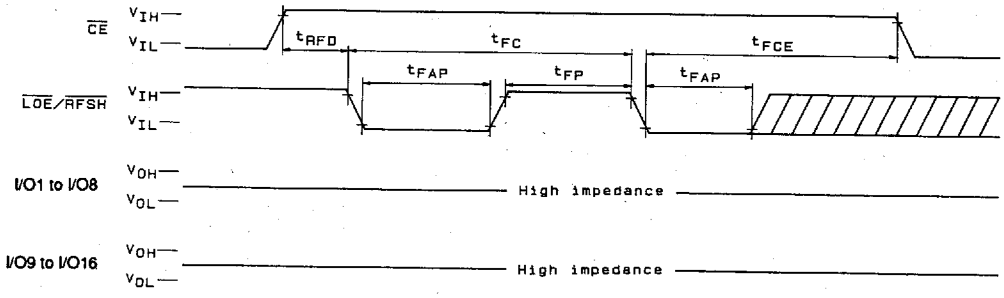


Note: A8 to A14 = "H" or "L"

▨: "H" or "L"

A01595

Auto-Refresh Cycle



Note: A0 to A14, $\overline{UOE}$, $\overline{LWE}$, $\overline{UWE}$ = "H" or "L"

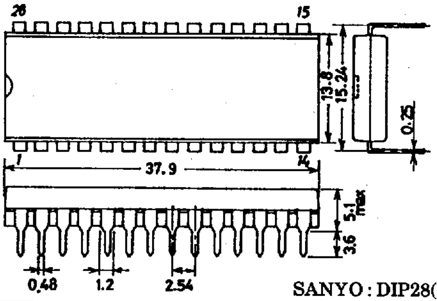
▨: "H" or "L"

A01596

MEMORY PACKAGE DIMENSIONS

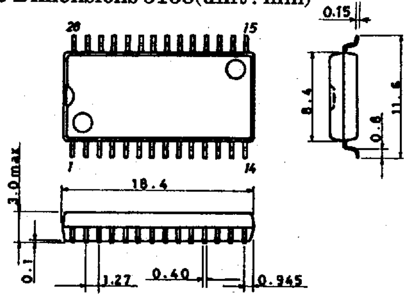
- All of Sanyo Memory package dimensions are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

Package Dimensions 3012A(unit: mm)



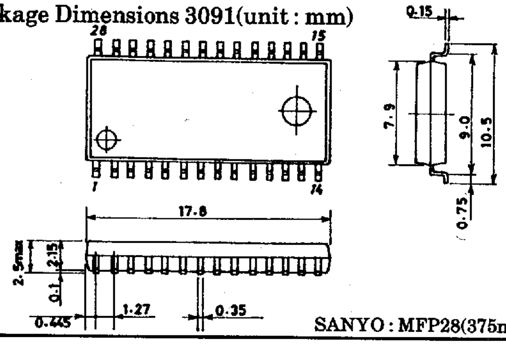
SANYO : DIP28(600mil)

Package Dimensions 3158(unit: mm)



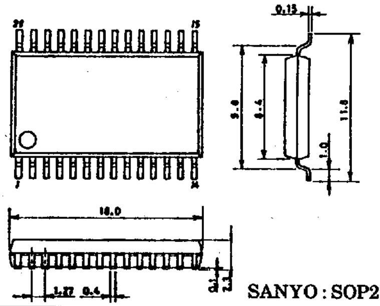
SANYO : SOP28(450mil)

Package Dimensions 3091(unit: mm)



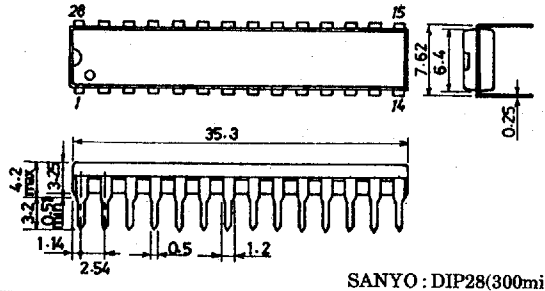
SANYO : MFP28(375mil)

Package Dimensions 3187(unit: mm)



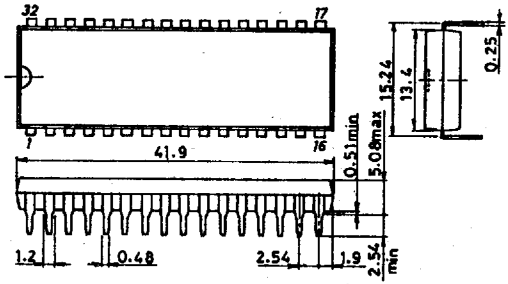
SANYO : SOP28D(450mil)

Package Dimensions 3123(unit: mm)



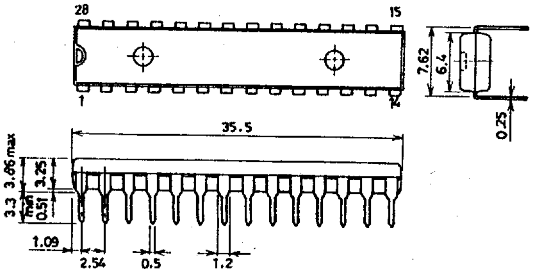
SANYO : DIP28(300mil)

Package Dimensions 3192(unit: mm)



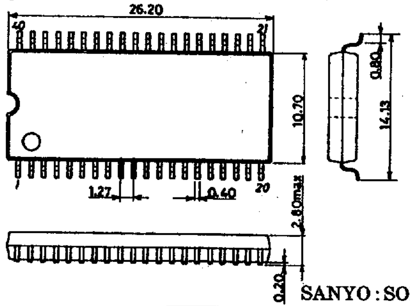
SANYO : DIP32(600mil)

Package Dimensions 3133 (unit: mm)



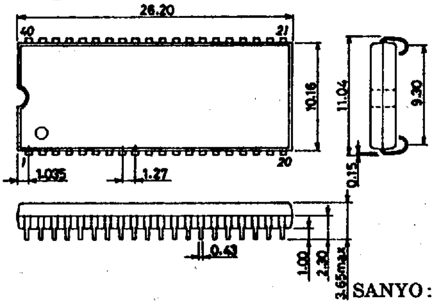
SANYO : DIP28(300mil)

Package Dimensions 3195(unit: mm)



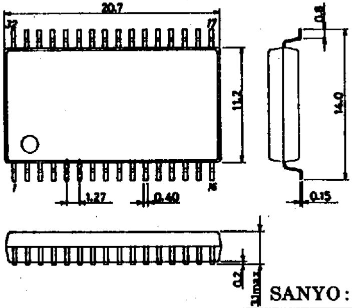
SANYO : SOP40(525mil)

Package Dimensions 3200(unit : mm)



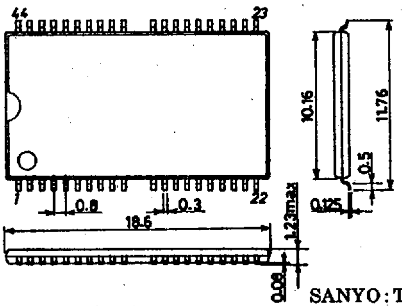
SANYO : SOJ40(400mil)

Package Dimensions 3205(unit : mm)



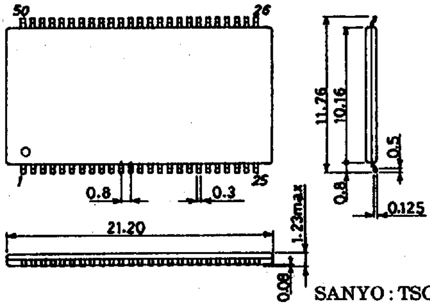
SANYO : SOP32(525mil)

Package Dimensions 3207(unit : mm)



SANYO : TSOP44 II

Package Dimensions 3211(unit : mm)



SANYO : TSOP50 II