HEWLETT PACKARD

Low Input Current, High Gain, Hermetically Sealed Optocoupler

Technical Data

8-pin Dual In-Line Package
HCPL-5700
HCPL-5701 (883B)
5962-8981001PC
HCPL-5730
HCPL-5731 (883B)
5962-8978501PC
20 Terminal Leadless Chip Carrier
HCPL-6730
HCPL-6731 (883B)
5962-89785022A

Features

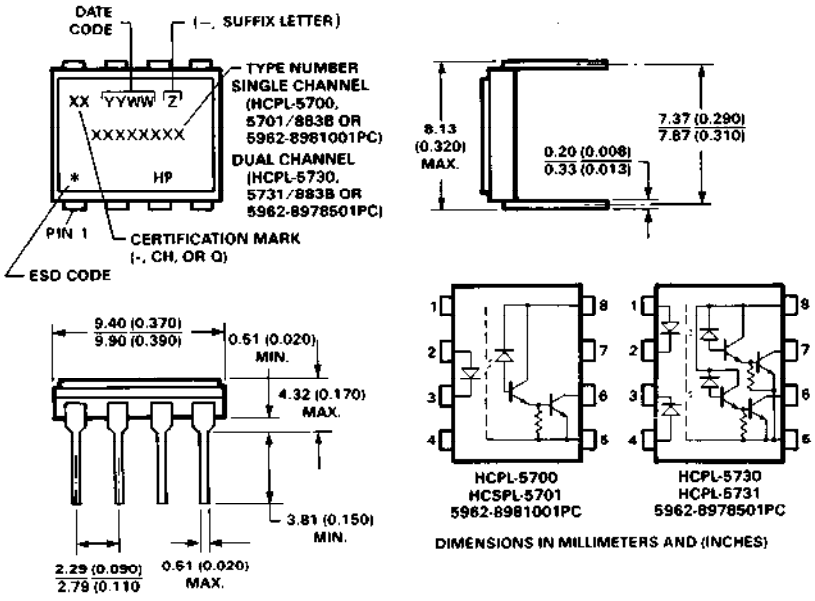
- DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534
- Hermetically Sealed Packages
- Performance Guaranteed Over -55°C to +125°C Ambient Temperature Range
- MIL-STD-883 Class B Testing
- Low Input Current Requirement: 0.5 mA
- High Current Transfer Ratio: 1500% Typical
- Low Output Saturation Voltage: 0.11 V Typical
- 1500 Vdc Withstand Test Voltage
- Low Power Consumption
- High Radiation Immunity
- Function Compatibility with 6N138/9, HCPL-2730/31, and 6N140A
- 2-18 Volt V_{CC} Range

Applications

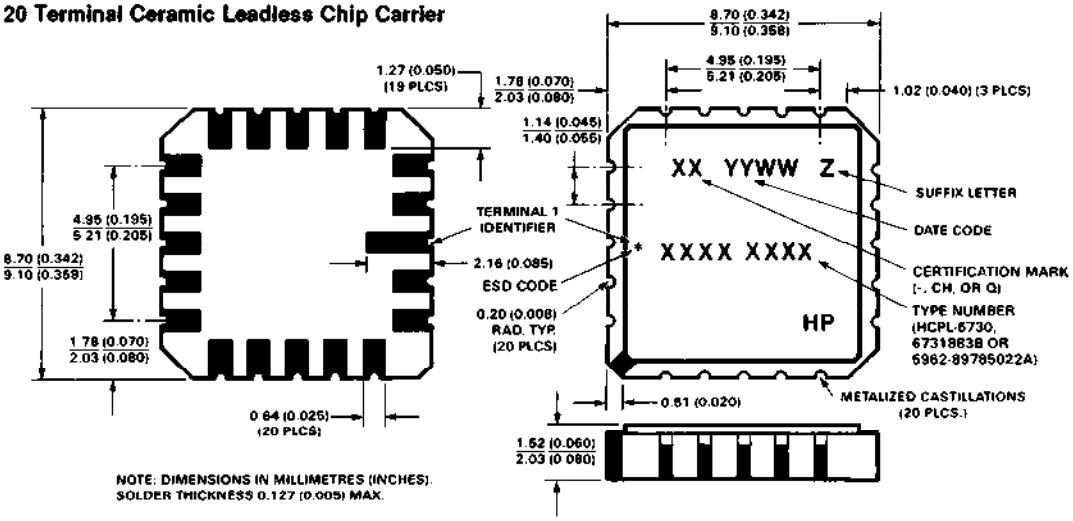
- Military/High Reliability Systems
- Telephone Ring Detection
- Microprocessor System Interface
- EIA RS-232-C Line Receiver
- Level Shifting
- Digital Logic Ground Isolation
- Current Loop Receiver
- Isolated Input Line Receiver
- System Test Equipment Isolation
- Process Control Input/Output Isolation

Outline Drawings

8-PIN CERAMIC DUAL IN-LINE PACKAGE

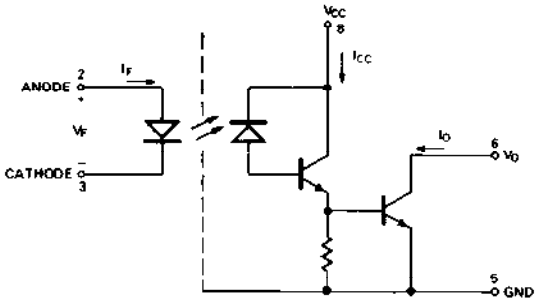


20 Terminal Ceramic Leadless Chip Carrier

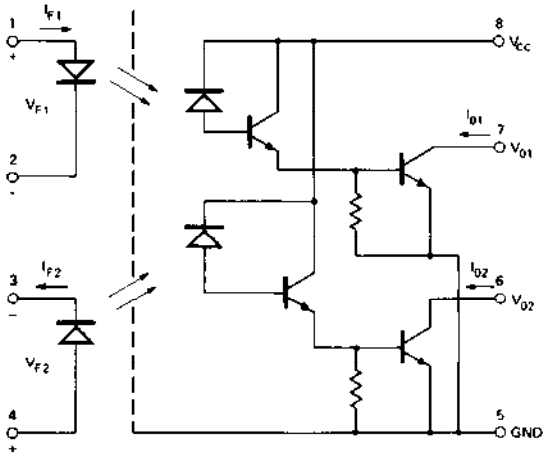


Description

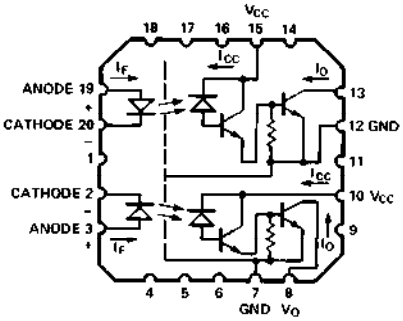
The HCPL-5700, HCPL-5701, and 5962-8981001PC are single channel, low input current, high gain optocouplers. The HCPL-5730, HCPL-5731 and 5962-8978501PC are dual channel units made from the same chip sets. All six products are in eight pin hermetic dual in-line packages. These units are capable of operation and storage over the full military temperature ranges and can be purchased as either single or dual channel standard product (HCPL-5700 and HCPL-5730 respectively), with full MIL-STD-883 Class Level B testing (HCPL-5701 and HCPL-5731 respectively), or from the DESC Standard Military Drawings (SMDs) 5962-89810 and 5962-89785 as (5962-8981001PC or 5962-8978501PC respectively). All parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the SMD part number, or by adding Option 200 to the part number for non-SMD parts.



8 PIN CERAMIC DIP SINGLE CHANNEL SCHEMATIC



8 PIN CERAMIC DIP DUAL CHANNEL SCHEMATIC



20 TERMINAL CERAMIC LEADLESS CHIP CARRIER SCHEMATIC

The HCPL-6730, HCPL-6731, and 8962-89785022A are dual channel parts in twenty terminal hermetic, ceramic, leadless chip carriers. The standard part is HCPL-6730. The product with full MIL-STD-883 Class Level B testing is HCPL-6731. The DESC SMD part is 5962-89785022A. All three products are configured and function as two independent single channels. Devices are delivered with solder dipped terminals as a standard feature. Units may also be purchased with gold plated terminals.

All devices are manufactured and tested on a MIL-STD-1772 certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Each channel contains a GaAsP light emitting diode optically coupled to an integrated high gain photon detector. The high gain output stage features an open collector output providing both lower saturation voltage and higher signaling speed than possible with conventional photo-Darlington optocouplers.

The supply voltage can be operated as low as 2.0 V without adversely affecting the parametric performance.

These devices have a 300% minimum CTR at an input current of only 0.5 mA making them ideal for use in low input current applications such as MOS, CMOS, low power logic interfaces or line receivers.

Compatibility with high voltage CMOS logic systems is assured by the 18V VCC, VOH current and the guaranteed maximum output leakage current at 18 V. The shallow depth and small junctions offered by the IC process provides better radiation immunity than conventional phototransistor optocouplers.

Upon special request, the following device selections can be made: CTR minimum of up to 600% at 0.5 mA, lower drive currents to 0.1 mA, and lower output leakage current levels to 100 µA.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	$V_{F,OFF}$		0.8	V
Input Current, High Level (Each Channel)	$I_{F,ON}$	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
Output Current, I_O (each channel) ..... 40 mA
Output Voltage, V_O (each channel) ..... -0.5 to 20 V[1]
Supply Voltage ,V_{CC} ..... -0.5 to 20 V[1]
Output Power Dissipation (each channel) ..... 50 mW[2]
Peak Input Current (each channel, ≤ 1 ms duration) ..... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (each channel) ..... 5 V

Electrical Characteristics T_A = -55°C to +125°C, unless otherwise specified

Parameter		Sym.	Test Conditions	Group A[11,14] Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
Current Transfer Ratio		CTR	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1, 2, 3	300	1500		%	3	4, 5
			I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		300	1000				
			I_F = 5 mA, V_O = 0.4 V, V_{CC} = 4.5 V		200	500				
Logic Low Output Voltage		V_{OL}	I_F = 0.5 mA, I_O = 1.5 mA, V_{CC} = 4.5 V	1, 2, 3		0.11	0.4	V	2	4
			I_F = 1.6 mA, I_O = 4.8 mA, V_{CC} = 4.5 V			0.13	0.4			
			I_F = 5.0 mA, I_O = 10 mA, V_{CC} = 4.5 V			0.16	0.4			
Logic High Output Current		I_{OHX} / I_{OH}	I_F = 2 µA (Channel Under Test) I_F = 10 mA (Other Channel) V_O = V_{CC} = 18 V	1, 2, 3		0.001	250	µA		6
Logic Low Supply Current	Single Channel	I_{CCL}	I_F = 1.6 mA, V_{CC} = 18 V	1, 2, 3		1.0	2	mA		
	Dual Channel		I_{F1} = I_{F2} = 1.6 mA, V_{CC} = 18 V				4		4	16
Logic High Supply Current	Single Channel	I_{CCH}	I_F = 0, V_{CC} = 18 V	1, 2, 3		0.001	20	µA		
	Dual Channel		I_{F1} = I_{F2} = 0, V_{CC} = 18 V				40			16
Input Forward Voltage	8 Pin DIP Devices	V_F	I_F = 1.6 mA	1	1.0	1.44	1.7	V	1	4
				2			1.7			
				3			1.8			
	20 Terminal Devices			1, 2, 3	1.0		1.8			
Input Reverse Breakdown Voltage		BV_R	I_R = 10 µA	1, 2, 3	5			V		4
Input-Output Insulation Leakage Current		I_{I-O}	45% Relative Humidity, t = 5 s, V_{I-O} = 1500 Vdc	1			1.0	µA		7, 13

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Electrical Characteristics (continued)

Parameter	Sym.	Test Conditions	Group A[14] Subgroups	Min.	Typ.*	Max.	Units	Fig.	Notes
Propagation Delay Time to Logic High at Output	t_{PLH}	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5 V	9, 10, 11		17	60	µs	7, 8	4
		I_F = 1.6 mA, R_L = 1.5 kΩ, V_{CC} = 5 V			14	50			
		I_F = 5.0 mA, R_L = 680 Ω, V_{CC} = 5 V			8	30			
Propagation Delay Time to Logic Low at Output	t_{PHL}	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5 V	9, 10, 11		10	100	µs	7, 8	4
		I_F = 1.6 mA, R_L = 1.5 kΩ, V_{CC} = 5 V			5	30			
		I_F = 5.0 mA, R_L = 680 Ω, V_{CC} = 5 V			2	10			
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	I_F = 0, R_L = 1.5 kΩ $\|V_{CM}\|$ = 50 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	≥2000		V/µs	9	4, 10, 12, 15
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	I_F = 1.6 mA, R_L = 1.5 kΩ $\|V_{CM}\|$ = 50 V_{P-P}, V_{CC} = 5.0 V	9, 10, 11	500	≥1000		V/µs	9	4, 11, 12, 15

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics

T_A = 25°C, V_{CC} = 5 V

Parameter	Symbol	Typical	Units	Test Conditions	Figure	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		4, 8
Capacitance (Input-Input)	C_{I-O}	2.0	pF	f = 1 MHz		4, 8
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.8	mV/°C	I_F = 1.6 mA		4
Input Capacitance	C_{IN}	60	pF	f = 1 MHz, V_F = 0		4

Dual Channel Product Only

Input-Output Insulation Leakage Current	I_{I-I}	0.5	nA	45% Relative Humidity, V_{I-I} = 500 Vdc T_A = 25°C, t = 5 s		9
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 Vdc		9
Capacitance (Input-Input)	C_{I-I}	1.0	pF	f = 1 MHz		9

Notes:

1. GND Pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 V, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus total supply power for the single channel device. For the dual channel device, output power is collector output power plus one half the total supply power. Derate at 1.66 mW/°C above 110°C.
3. Derate I_F at 0.33 mA/°C above 110°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. I_F = 2 μA for channel under test. For all other channels, I_F = 10 mA.
7. Device considered a two-terminal device: For 8 pin DIP, pins 1 through 4 are shorted together, and pins 5 through 8 are shorted together; for LCC, terminals 19, 20, 1, 2, 3 are shorted together, and terminals 7 through 15 are shorted together.
8. Measured between each input pair shorted together, and all outputs for that channel shorted together.
9. Measured between adjacent input pairs shorted together; i.e., for 8 pin DIP, between pins 1 and 2 shorted together and pins 3 and 4 shorted together; for LCC, between terminals 19 and 20 shorted together, and terminals 2 and 3 shorted together.
10. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
11. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
12. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is

$$R_{CC} \approx \frac{1\ V}{0.15\ I_F\ (mA)}\ k\Omega$$

for single channel;

$$R_{CC} \approx \frac{1\ V}{0.3\ I_F\ (mA)}\ k\Omega$$

for dual channel.

13. This is a momentary withstand test, not an operating condition.
14. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
15. Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in Table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.
16. The HCPL-6730 and HCPL-6731 dual channel parts function as two independent single channel units. Use the single channel parameter limits.

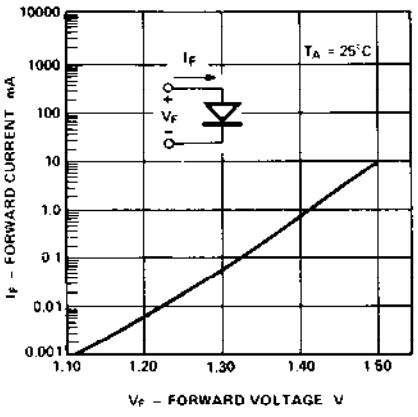


Figure 1. Input Diode Forward Current vs. Forward Voltage.

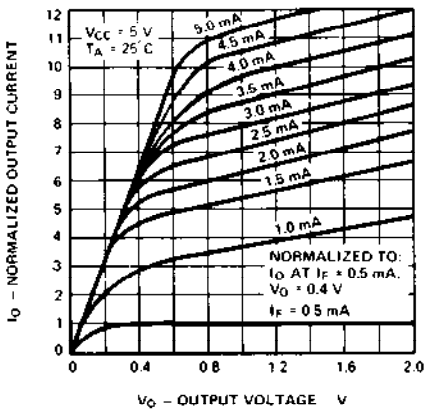


Figure 2. Normalized DC Transfer Characteristics.

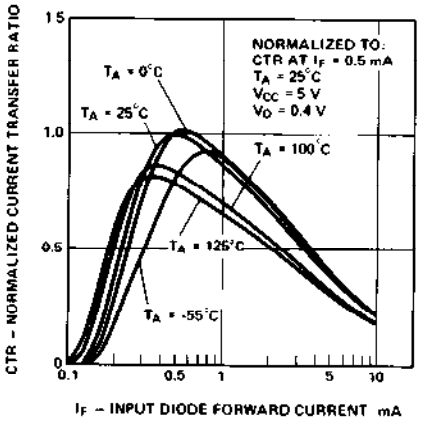


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

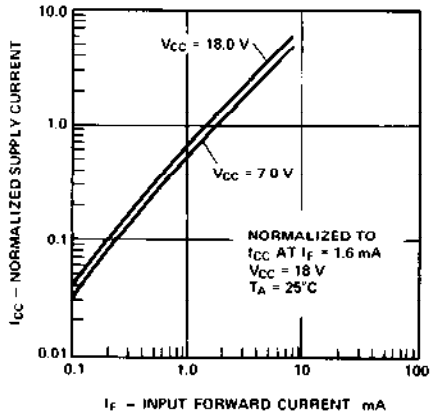


Figure 4. Normalized Supply Current vs. Input Diode Forward Current.

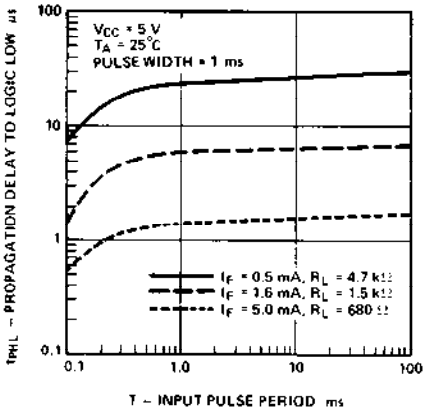


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

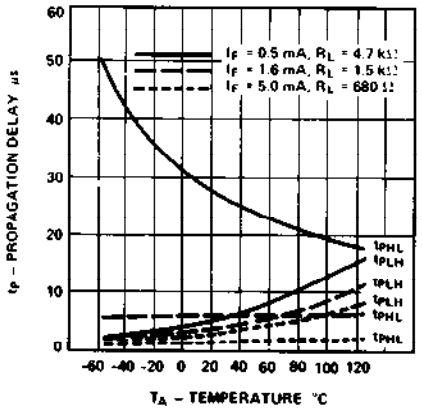


Figure 6. Propagation Delay vs. Temperature.

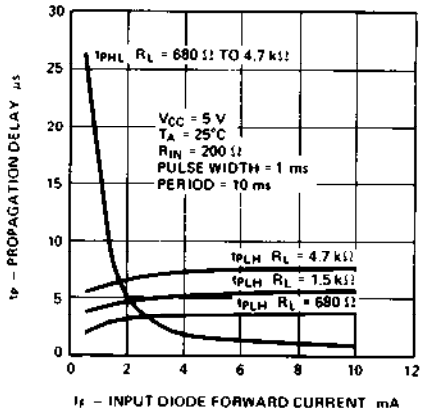
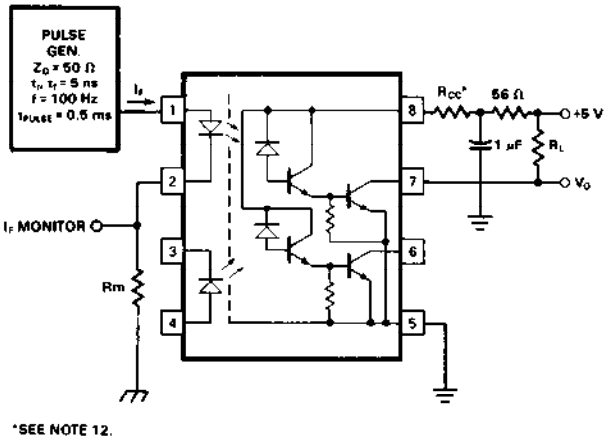
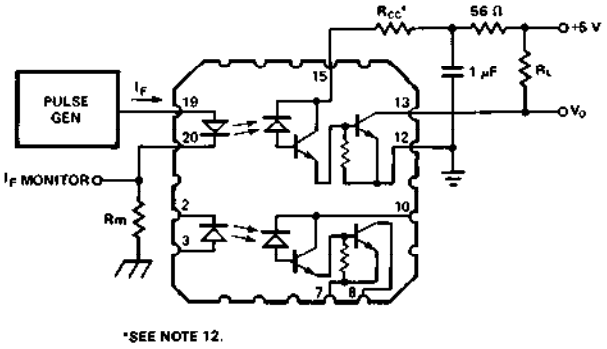


Figure 7. Propagation Delay vs. Input Diode Forward Current.





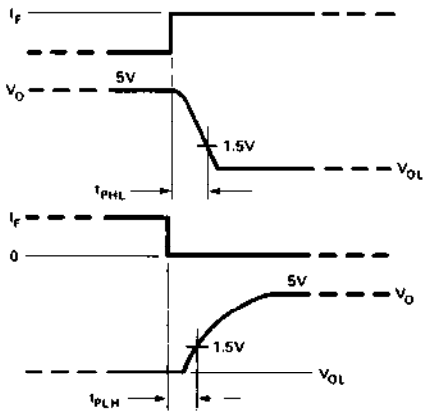
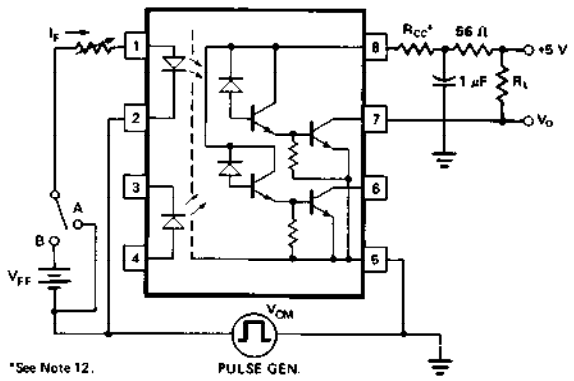
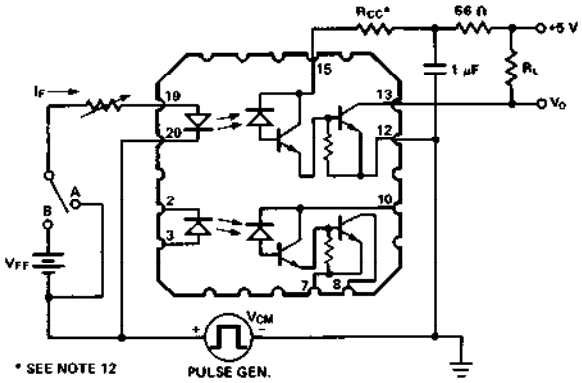
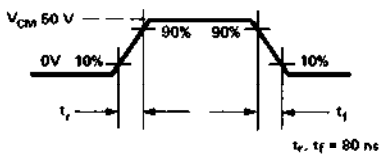
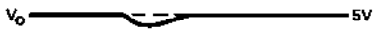


Figure 8. Switching Test Circuit.









SWITCH AT A: I_F = 0mA

SWITCH AT B: I_F = 1.6mA

Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

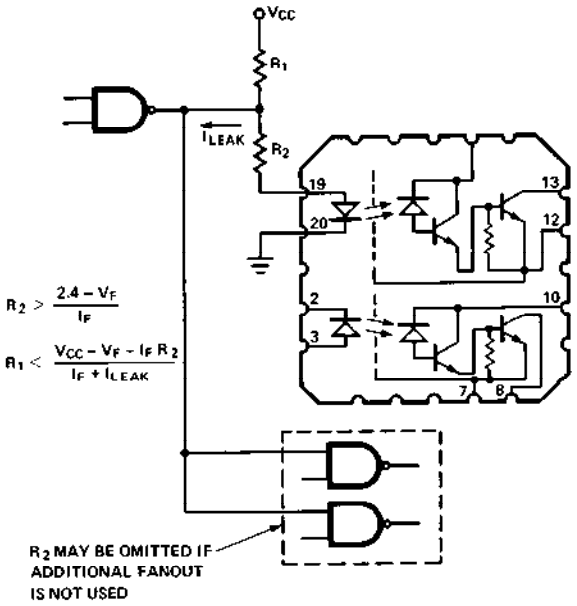


Figure 10. Recommended Drive Circuitry Using TTL Open-Collector Logic.

Condition A not E.

II. Quality Conformance Inspection per MIL-STD-883, Method 5005, Group A, B, C, and D.

Group A–See Electrical Characteristics Table.

Group B–No change.

Group C–No change.

Group D–Constant Acceleration–Condition A not E.

SMD 5962-8981001PC SMD 5962-8978501PC SMD 5962-89785022A and MIL-STD-883 Class B Test Programs

Hewlett-Packard's 883B Optocouplers are in compliance with MIL-STD-883, Revision C. Deviations listed below are specifically allowed in DESC SMDs 5962-89810 and 5962-89785 for Hewlett-Packard Optocouplers from the same generic families using the same manufacturing processes, design rules and elements of the same microcircuit groups.

Testing consists of 100% screening to Method 5004 and quality conformance inspection to Method 5005 of MIL-STD-883.

Clarifications:

I. 100% screening per MIL-STD-883, Method 5004 constant acceleration–

Part Numbering System

Commercial Product	Class B Product	SMD Product
HCPL-5700	HCPL-5701	5962-8981001PC
HCPL-5730	HCPL-5731	5962-8978501PC
HCPL-6730	HCPL-6731	5962-89785022A

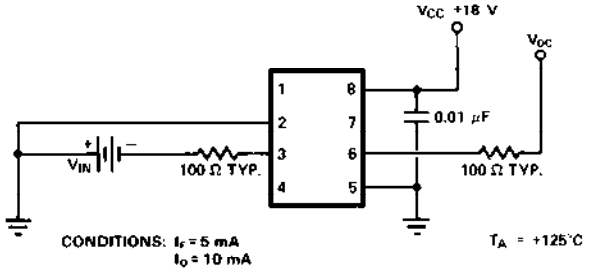


Figure 11. Single Channel Operating Circuit for Burn-In and Steady State Life Tests.

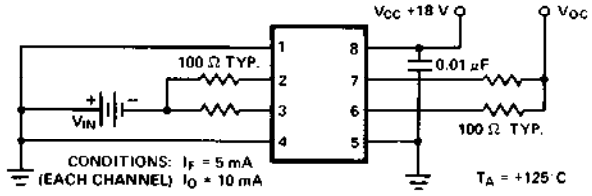


Figure 12. Dual Channel Operating Circuit for Burn-in and Steady State Life Tests.

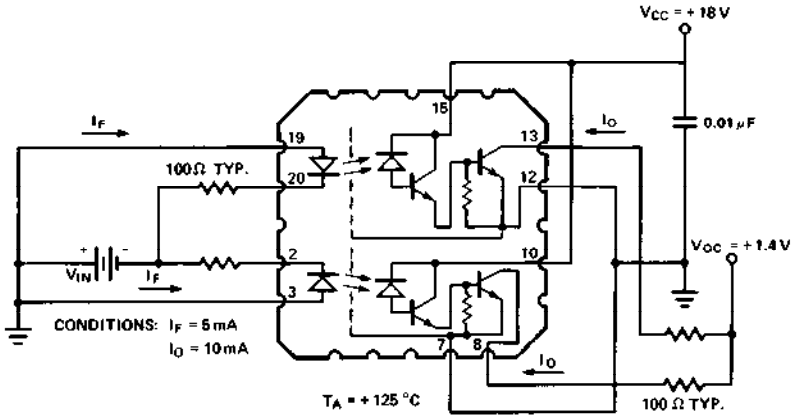


Figure 13. Operating Circuit for Burn-in and Steady State Life Tests.

For more information call:

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*Or call your local HP sales office listed in your telephone directory. Ask for a Components representative.

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