Video Generator Chip

FEATURES

- Direct interfacing with the TELEVIEW busses
- Provides master timing signals for the other TELEVIEW chips to indicate the status of the display scan
- Can address up to eight Page Stores
- Provides the address information to scan the allocated Page Store
- Provides composite synchronizing signals for the receiver for 'Off-Hours' working
- Provides various display facilities

DESCRIPTION

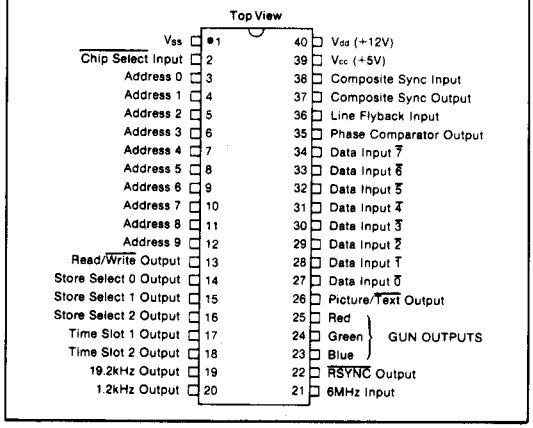
The Video Generator chip is one of a set of LSI chips used in the General Instrument TELEVIEW Teletext/Viewdata system. It reads the contents of a Page Store and generates outputs suitable for driving a normal color television receiver to display the contents of the Page Store.

The chip also monitors the composite synchronizing signals within the receiver and locks the total TELEVIEW system onto the incoming signals. When no transmission is taking place the chip develops a composite sync signal which is used to synchronize the receiver.

The device is fabricated in General Instrument's N-channel metal gate MOS process providing direct TTL interfacing, high speed and good reliability.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE



OPERATION

The Video Generator Chip contains the logic and control functions to interrogate a selected TELEVIEW Page Store and display the contained information at the correct period within the raster scan on a normal TV receiver. The chip also generates the master timing signals TS1 and TS2 which indicate the raster status to the Control processor and Data Acquisition chips.

The basic block diagram of the chip is shown in Fig. 1 and major functional blocks are described below.

Line Synchronizing Detector and Generator— The prime function of this block is to detect negative going sync. signals from the incoming mixed sync and to synchronize the TELEVIEW system with the transmitted signal. This is necessary for News flashes and subtitling functions. When the incoming transmission is turned off, (i.e. goes "off-hours"), this is recognized by the detector after three frames of missing sync. pulses. The internal link between Comp. Sync In and Comp. Sync Out is removed and an internally generated "Comp Sync" is switched to the Comp. Sync Out pin. Thus the receiver will continue in lock but synchronized to the Video Generator. Similarly if the normal transmission resumes the fact that external sync pulses are being received is recognized by the Video Generator and the chip will re-synchronize itself with the incoming transmission. Because the Video Generator is aware of the status of the mixed sync at all times the chip can detect frame sync, line sync and even or odd frames. Thus with this information the chip can continuously monitor the current line number. The relevant sections of the line scan are decoded and are indicated externally by the TS1, TS2 time slot outputs. These signals are fully described in Fig. 3, but there are four periods i.e.

a) Writing to RAM.
This occurs during Teletext lines during the frame fly-back period, under control of the D.A. chip.

b) Reading from RAM.
This occurs under control of the Video Generator chip between lines 48 and 288, and is when the display is active.

c) Data Interchange Periods.
The Interchange of information between D.A. and Control Processor and Video Generator occurs during these periods (23-47 and 289-6). Total flexibility is available to the Control Processor at these times as it becomes 'bus master', the peripherals being serviced under the control of the processor.

As the chip is aware of the raster status the chip also starts and stops the Address counter/latch combination which is used to scan the relevant Page Memory. The form of the generated sync pulses are shown in Fig. 2.

Address Counter/Latch— The address counter is a binary counter which is incremented at the character display rate (1MHz). It can also be loaded from a latch which contains the start address of each character row. Since each character consists of 10 vertical lines of raster scan, the counter is incremented 40 times from a start address and then is reloaded with the same start address ready for the next raster scan of the same forty characters. This occurs nine times. On the last line the counter is incremented an extra count and this new address is stored in the latch. This address being the start address of the next row of forty characters. The above sequence is then repeated.

If one is displaying only one half of a page with all characters in double height, the Video Generator scans the same forty addresses nineteen times and stores the new address on the twentieth raster scan. If one is in the bottom half of the page, the address counter must be initialized to 480.

BLOCK DIAGRAM

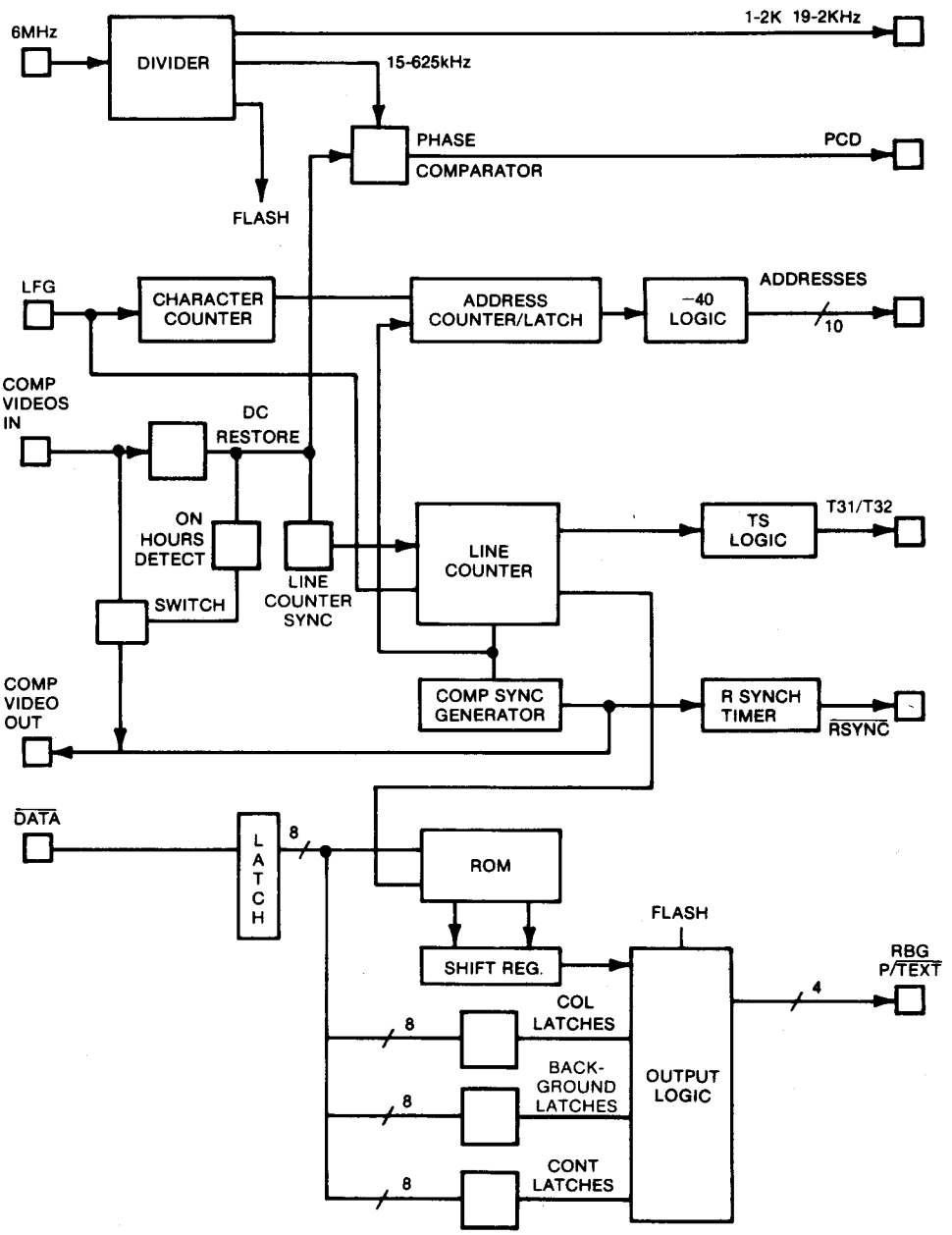


Fig. 1

AY-3-9725 VIDEO GENERATOR CHIP

The display format of 40 characters, each 1μs wide, occurs on a line of 64μs duration thus leaving a border of 12μs on each end of the character row. This address counter is actually started some 4μs before the start of the proper character display thus allowing time for address generation, RAM access time, ROM access time and display processing, these actions being pipelined. Facilities are also provided such that the output address can be reduced by 40 thus allowing accessing of the character in the row above. This is a necessary operation for a 'Double Height' display option which will be discussed later. This facility is inhibited when we are only displaying one half of a page. The address so produced is presented on the address bus and the required Page Memory is activated by the Store Select Outputs. The address drivers are tristate thus allowing easy bus interface.

Input Latches and Character Read-Only Memory—The data being read from the required Page Memory is placed on the Data Bus and is latched into the Data Bus latches. A total of 650ns is allowed for the RAM read cycle and thus quite slow Random Access memories may be used. Having been latched by the Video Generator chip the seven bit character is used to address the character Read Only Memory. This memory is organized as 96 characters each of 45 dots (5 x 9 array).

Data Control Latches—Certain characters indicate to the Video Generator a change in display status. These characters are contained within columns 0 and 1 of the normal Teletext/Viewdata character set and may be used to change character color, background color, height etc. These facilities, and the control of them, are fully described in the British Broadcasting Teletext Specification (Sept. 1976) published by the BBC, IBA and BREMA.

Output Logic and Drivers—The output logic reads the character ROM into a six bit parallel to serial shift register. This operation occurs at the left-hand side of the character to be displayed, the data in the register is then shifted out at 6MHz (character dot-rate) the data bits selecting between character and background information. This information is used to drive the fast Gun output drivers. These outputs have to be closely matched for propogation delay and rise and fall time to ensure good legibility.

DATA INTERCHANGE

During the TS11 timeslot the Video Generator can send information to or receive information from other devices attached to the TELEVIEW system busses. This is normally used by the control chip to update the control and display latched within the Video Generator. The Video Generator is enabled to receive by putting the address 1111XX0XXX on the address highway (active high).

The latches are updated by the following control words, active low signalling, most significant bit is a strobe.

Highway Free	0	0	0	0	0	0	0	0	
Control Word 1	1	0	0	0	T	S	s	s	
Control Word 2	1	0	0	1	X	C_4	C_6	C_5	Teletext
Control Word 3	1	0	1	0	C_{10}	C_9	C_8	C_7	
Control Word 4	1	0	1	1	C_{14}	C_{13}	C_{12}	C_{11}	
Control Word 2	1	0	0	1	X	F	0	0	Viewdata
Control Word 3	1	0	1	0	b_7	0	b_6	b_5	
Control Word 4	1	0	1	1	b_4	b_3	b_2	b_1	
Store Select for Display	1	1	0	0	SP	D	d	d	
Key Data	1	1	0	1	P	*	*	*	
Other Facilities	1	1	1	0	X	X	M	BC	

The Control bits are as follows:

T	TELETEXT MODE i.e. NOT VIEWDATA	
S_{SS}	Identification of Store being written to	
D_{DD}	Identification of Store being displayed from	
C_4/F	Erase page (Rows 1-23 Teletext, Rows 0-23 Viewdata)	
C_5	Newsflash	TELETEXT ONLY
C_6	Subtitle	
C_7	Suppress Header	
C_8	Update Indicator	TELETEXT ONLY
C_9	No action	
C_{10}	Inhibit display	
C_{11}	No action	
C_{12}-C	Switches rounding off if all set	
b_7-b_1	Cursor bits (Viewdata Only)	
001 0001	Cursor ON	
001 0100	Cursor OFF	
F	Form feed or first appearance	
SP	Sets Picture/Text to picture (For initialization)	
P	P Key pressed	
M	Mix Mode	
BC	Box Clock (Teletext Only)	
***	These are coded as follows	
001	Picture/Text Key pressed	
010	Reveal/Conceal Key pressed	
011	Update/Clear Key pressed	
100	½ Page Key pressed (Cycles Full, Top, Bottom, Full etc.).	

PIN FUNCTIONS

Pin No.	Name	Functions
1	V_{SS}	This is the negative supply for the chip and is used as a reference for all the electrical parameters.
2	$\overline{\text{Chip Select}}$ Input	The Chip can be put into its passive state with all Bus and Gun outputs off by taking this input high. This input is internally loaded low. This facility is useful in comprehensive display systems, where several devices may be required to drive the display.
3-12	Addresses 0-9	These pins are connected to the Address Bus of the TELEVIEW system. They are used for address Input/Output.
13	Read/$\overline{\text{Write}}$ Output	This output is used to drive the Random Access Memories forming the Page Memory.
14-16	Store Select Outputs 0-2	These outputs are used to select the required page store.
17,18	Time Slot Outputs 1 and 2	These outputs are generated by the Video Generator from the status of the raster scan and are used to indicate this status to other chips within the TELEVIEW system.
19,20	19.2KHz and 1.2KHz Outputs	These outputs provide 19.2KHz and 1.2KHz square wave signals which are used by the UAR/T as reception and transmission clocks respectively.
21	6MHz Input	This input is fed from a 6MHz oscillator which may be phase locked to the normal transmission. During 'off-hours' working a crystal oscillator is normally used.
22	$\overline{\text{RSYNC}}$ Output	This output is an open-drain output and is used to indicate the presence of Teletext lines to the D.A.Chip and Data Grabber. The timing of this signal is indicated in Fig. 4.
23-25	Red, Green and Blue Gun Outputs	These outputs are push-pull outputs which go high to turn on the relevant color gun for displaying. These outputs are closely matched for propogation delay and rise and fall times.
26	Picture/$\overline{\text{Text}}$ Output	This output is used by the TELEVIEW system to indicate to the receiver if data is to be displayed and is used to change the display from normal video to data video from the Red, Green and Blue chip outputs. In the mix mode this generates Black and White data video. It will then be matched to the gun outputs for propogation delay and rise and fall times.
27-34	Data Inputs $\overline{\phi}$ to $\overline{7}$	The Data Inputs from the communication highway between the Video Generator and the Control Processor and Page Memory.
35	Phase Comparator Output	In on-hours operation the display Line Flyback signal is compared for phase with an internal 64μs period signal derived from the 6MHz display clock. The output is a pulse which, when integrated, produces a voltage for controlling a V.C.O. 6MHz display oscillator, thus locking the display to the incoming picture. In off hours operation this open drain output goes low permanently, and thus can be used as an indication of on-hours/off-hours status.
36	Line Flyback Input	The Line Flyback input is a signal from the display deflection circuitry which is used for positioning the display on the T.V. screen.
37	Comp. Sync Output	The Comp. Sync Output outputs either the Comp. Video input in 'on-hours' operation or an internally generated Comp. sync signal in 'off-hours' operation.
38	Comp. Sync Input	The Comp. Sync Input monitors the composite video being received and extracts synchronizing information and 'on-hours' 'off-hours' information for the Video Generator.
39	V_{CC}	This pin is connected to the +5.0V supply. This supply has a low current requirement .
40	V_{DD}	The V_{DD} forms the positive supply for the chip.

DISPLAY OPTIONS

Logic is contained on the Video Generator chip to process the Display Modes as described in the Broadcast Teletext Specification. These facilities are outlined below. Some extra facilities are also included.

Character Set

The chip can display 96 Alphanumeric characters and 64 Graphic shapes which may be either contiguous or separated. The alphanumeric format is determined by a 4320 bit Read Only Memory organized as:

96 (character) x 5 (dots) x 9 (lines) = 4320

The graphic shapes are determined directly from the bits of the character code Fig. 5.

Display and Background Color

The characters and the background can be displayed in one of seven colors. In addition the background may be black. This information is stored in two sets of three latches representing character and background colors.

Conceal and Flash

Selected characters can be concealed and optionally released by the viewer. Selected characters can be flashed on command. The flashing is controlled by an on-chip flash oscillator. During the flash period or when concealed only background information is displayed.

Boxing

Text or graphics characters can be inserted in a normal video picture when required. This is achieved by means of the Picture-/$\overline{\text{Text}}$ output which can be used externally to switch the guns between Picture and text signals.

Double Height

Double height characters are characters contained between the control characters "Double Height" and "Normal Height" (or end of line). When a "Double Height" control character is read from the RAM only the top half of the subsequent character(s) are displayed during the 10 raster scans. During the next 10 scan lines, 40 is subtracted from the addresses being output on A0-A9 so the same 40 addresses are read for another 10 times. Characters which are not double height are displayed as the background color and the bottom(s) of the double height character(s) is (are) displayed.

Hold Graphics

When this latch is set, any subsequent control characters (except Double/Normal Height or change alpha/graphics) are displayed as the last graphics characters.

Special Graphics

This is a high resolution graphics facility, not available in normal Teletext/Viewdata systems. There is a one to one correspondence between data bits b_1, b_2, b_3, b_4, b_5, b_7 and the six dots in each horizontal line of a character. This gives an overall graphics resolution of 6 x 20 for each character.

Box Clock

The last eight characters of the top row (Row 0) of a teletext page can be boxed in double height into a normal television picture. These eight characters contain the time in BBC/IBA broadcasts.

Half-page Operation

This allows either the top or bottom half of a normal Teletext/Viewdata page to be displayed over the whole screen, with each character in double height. This makes the display easier to read from a distance. Double height characters are ignored in this mode.

Black and White Output

In normal operation this is the Picture/Text output and is used to blank the normal picture information for boxing newsflashes or displaying a page of teletext information, etc.
In the mix mode this outputs black and white teletext information which is matched to the Gun Output signals in delay and drive. This can be used to superimpose text onto a picture by "cutting away" the picture below text data or as an output for Black and White displays or printers.

Character Rounding Inhibit

Normally characters are rounded, i.e. half dots are added to smooth diagonals on an interlaced television display. This can be switched off when outputting to a printer.

Cursor

The cursor is stored as bit eight in the Page Store Data Character. It is displayed as a flashing bar on the bottom line of a character. The flashing is complementary to the normal character flashing and any character information on the bottom line (tails or graphics information) is suppressed to improve legibility.

SIGNAL DETECTION CRITERIA

The Video Generator detection circuitry for incoming sync signals is designed to prevent mis-operations in the presence of noise. The criteria for detection is defined below.

Line Sync

The Comp. Video Input must be negative for greater than 3μs.

Frame Sync

The Comp. Video Input must be negative for greater than 10μs and at least 310 lines (Line Flyback pulses) must have occurred since the previous Frame Sync detection.

Odd Frame Detection

Odd Frame Detection occurs when a Line Flyback pulse falls in a window 326-354 uS after Frame Sync Detection. However this detection must disagree with the internal Odd/Even frame status for 4 successive full frames before the internal status is inverted.

On-Hours/Off-Hours Detection

The Line Flyback pulse is compared for synchronism with the detected Line Sync such that the negative edge of Line Flyback should occur within 14μs of the negative edge of an incoming Line Sync signal. If such synchronism does not occur the number is accumulated and if more than 16 occur for two successive ½ frames the logic deems that the composite sync does not represent a valid transmitted signal and the Video Generator goes "Off-Hours". If however, less than eight occur in any two successive ½ frames, the logic deems that a valid Comp. Sync is being received and the system goes "On-Hours". If between eight and sixteen occurrances of no synchronism happen, then the system stays as it was.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

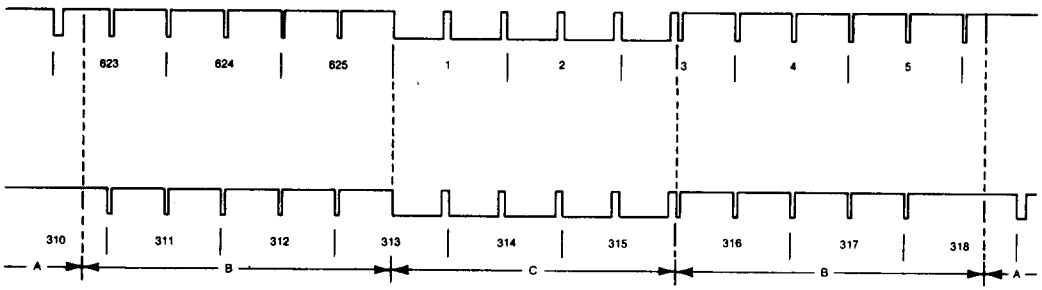
Voltage on any pin with respect to V_{SS} ..... −0.3 to +15V
Storage temperature range ..... −55°C to +150°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise indicated)
V_{SS} = 0V (substrate voltage) V_{CC} = +5V ± 5% V_{DD} = +12V ± 5% Operating Temperature T_A = 0°C to +70

Characteristic	Min	Typ	Max	Units	Conditions
INPUTS					
Chip Select					
Input Logic High	2.0	—	V_{DD}	V	
Input Logic Low	V_{SS}	—	0.8	V	
Input Current	25	—	120	μA	V_{IN} = 5V
COMP					
Input Logic High	2.5	—	V_{DD}		
Input Logic Low	V_{SS}	—	0.3		
Input Capacitance	—	—	15	pF	V_{IN} = 0V
6MHz					
Input Logic High	2.0	—	V_{DD}	V	
Input Logic Low	V_{SS}	—	0.8	V	
Input Capacitance	—	—	25	pF	V_{IN} = 0V
Mark to Space Ratio	45:55	—	55:45		
Frequency	1.0	—	6.5	MHz	
ALL OTHER INPUTS					
Input Logic High	2.0	—	V_{DD}	V	
Input Logic Low	V_{SS}	—	0.8	V	
Input Capacitance	—	—	15	pF	V_{IN} = 0V
Input Leakage	—	—	10	μA	V_{IN} = 12V
OUTPUTS					
Addresses, Read/Write					
Store Select (Tri-state)					
Logic High Output	2.4	—	V_{CC}	V	I_{OH} = -320μA
Logic Low Output	V_{SS}	0.2	0.4	V	I_{OL} = 3.2mA
Capacitance	—	—	15	pF	V_{IN} = 0V @ 1MHz
T_{RISE}, T_{FALL}	—	—	200	ns	C_{LOAD} = 100pF
Leakage (Disabled)	—	—	10	μA	V_O = 0V, 5V
TIME SLOTS (TS1, TS2)					
(PUSH-PULL)					
Logic High Output	2.4	—	V_{CC}	V	I_{OH} = -320μA
Logic Log Output	V_{SS}	0.2	0.4	V	I_{OL} = 3.2mA
T_{RISE}, T_{FALL}	—	—	200	ns	C_{LOAD} = 100pF
COMP VIDEO (PUSH—PULL)					
Logic High Output	4	—	V_{DD}	V	I_{SOURCE} = −500μA) } Off Hours Mode
Logic Low Output	V_{SS}	—	0.4	V	I_{SINK} = 1.6mA) }
Capacitance	—	—	20	pF	
Series Resistance	—	—	100	ohms	Comp. Video In = 2V), On Hours Mode
RSYNC (OPEN DRAIN)					
Logic Low Output	V_{SS}	—	0.4	V	I_{OL} = 4.0mA
Logic High leakage	—	—	10	μA	V_O = 5V
Capacitance	—	—	15	pF	V_{IN} = 0V
PHASE COMPARATOR (OPEN DRAIN)					
Logic Low Output	V_{SS}	—	0.5	V	I_{OL} = 5mA
Logic High Leakage	—	—	10	μA	V_O = 5V
Capacitance	—	—	15	pF	V_{IN} = 0V
R.G.B. GUN OUTPUTS					
PICTURE/TEXT OUTPUTS (TRISTATE)					
Logic High Output	V_{CC}-1	—	V_{CC}	V	I_{SOURCE} = 2mA
Logic Low Output	V_{SS}	—	1	V	I_{SINK} = 5mA
Capacitance	—	—	20	pF	V_{IN} = 0V
T_{RISE}, T_{FALL} (10%-90%)	—	—	30	ns	C_O = 30pF
Differential T_{RISE}, T_{FALL}	—	—	30	ns	C_O = 30pF Picture/$\overline{\text{Text}}$ matched in mix mode only
Leakage (Disabled)	—	—	10	μA	V_O = 0, 5V[1]
POWER					
V_{CC} Supply	—	—	25	mA	V_{CC} = 5V
V_{DD} Supply	—	—	80	mA	V_{DD} = 12V

PERSONAL TERMINAL



A. LINE SYNC PULSES NEGATIVE. 5μS WIDTH. 64μS PERIOD.
B. EQUALIZING PULSES NEGATIVE. 2μS WIDTH. 32μS PERIOD.
C. BROAD PUSLES POSITIVE 4μS WIDTH. 32μS PERIOD.
ALL NEGATIVE EDGES AT 64μS OR 32μS INTERVALS.

Fig. 2 COMPOSITE SYNC

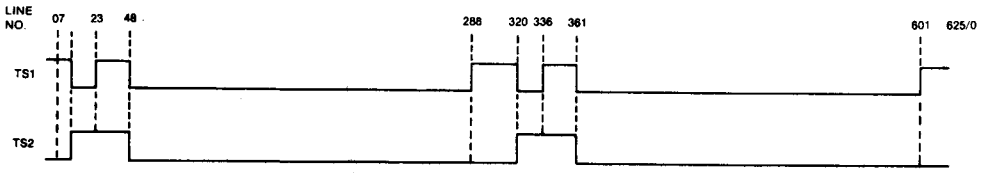


Fig. 3 TIME SLOT OUTPUTS

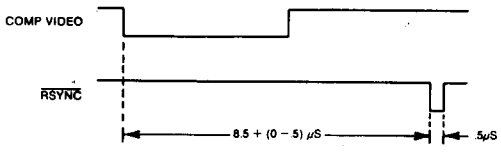
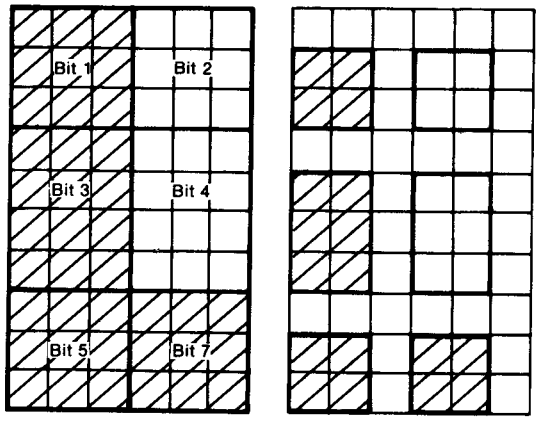


Fig. 4 $\overline{\text{RSYNC}}$ TIMING



BIT 1 IS LEAST SIGNIFICANT, BIT 6 = 1

SHADED EXAMPLE 1110101

Fig. 5 GRAPHICS FORMAT

Universal Active Filter

FEATURES

- Low Pass, High Pass, Band Pass, and Band Reject responses from the same unit
- Independent control of Frequency, Q and Amplifier Gain
- External resistors need not temperature track internal NPO capacitors
- 10Hz to 10kHz operating frequency range
- 0.5 to 50 adjustable Q range

DESCRIPTION

The schematic diagram for the ACF 7092C is shown in Figure 1. The filter is composed of 4 operational amplifiers. The first three form the basic state variable configuration (triad) and the fourth can be utilized for increased gain or in the biquadratic configuration with the addition of external components. Two filter inputs are provided; a non-inverting input and an inverting input.

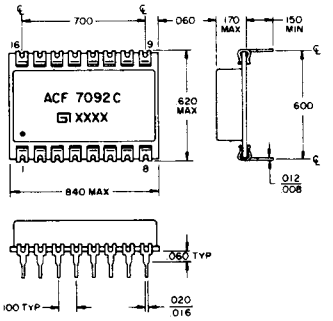
In the Triad configuration, amplifier A_1 is a summing amplifier providing the high pass output, amplifiers A_2 and A_3 are integrators providing band pass and low pass outputs. The external resistors establish the operating parameters for each filter mode. R_1 and R_2 determine the resonant frequency (Fn). R_7 and R_3 or R_7 and R_8 determine the values for gain and Q.

APPLICATIONS

General Instrument Hybrid universal active filters are low cost units that can be used to generate any filter response. Some common applications for these filters are found in sonar systems, telephone and paging systems, navigation systems, modems, transducers, biomedical measuring systems, process control equipment, data acquisition systems, radar systems, audio signal processing equipment and seismology.

PACKAGE INFORMATION
PIN CONFIGURATION

16 LEAD DUAL IN LINE
ACF 7092C



PIN	FUNCTION
1	A1(+IN)
2	A1 (—IN)
3	VHP
4	V+
5	VLP
6	A4 (+IN)
7	A3 (—IN)
8	NC
9	GND
10	A4 (—IN)
11	VO
12	V—
13	VBP
14	A2 (—IN)
15	NC
16	NC

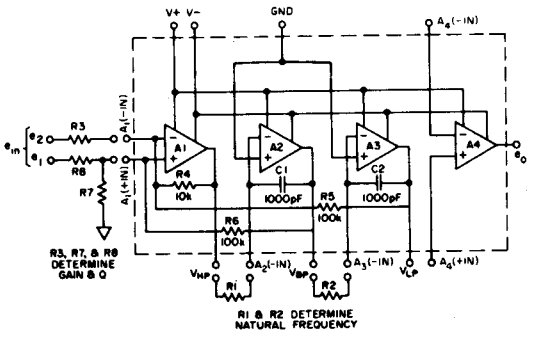


Fig. 1 SCHEMATIC

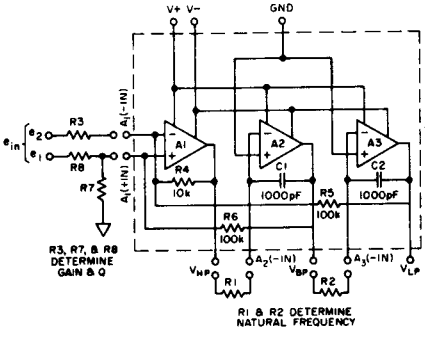


Fig. 2 TRIAD CONFIGURATION

TELECOM