SP9921

50 MBIT MANCHESTER BIPHASE DECODER

The SP9921 is a bipolar monolithic silicon integrated circuit for clock and data recovery from a Manchester biphase-mark encoded signal. It operates from a single 5V supply and has ECL outputs.

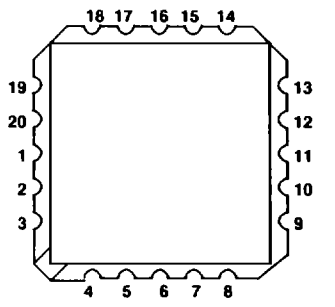
The device is also available as the SP9921AC, which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- -40°C to +85°C Operating Temperature Range
- 50Mbit/s Clock and Data Rates.
- Single Supply Voltage
- Sensitive Differential Input
- ECL Outputs
- Input Signal Detection from Lock Detect Output
- No False Frequency Lock
- Correct Phase Lock on Random Data

APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface



Pin	Description	Pin	Description
1	RX –	11	RXD
2	NC	12	RXC
3	V_{EE}	13	RXO
4	V_{EE}	14	V_{CC}
5	RECF	15	V_{CC}
6	BD	16	NC
7	REFF	17	RCI
8	V_{EE}	18	V_{CC}
9	RCO	19	V_{CC}
10	PLO	20	RX+

Fig.1 Pin connections - top view

ORDERING INFORMATION

SP9921 B LC (Industrial - leadless chip carrier)
SP9921 AC LC (Military - leadless chip carrier, screened to MIL-STD-883C CLASS B)

ASSOCIATED PRODUCTS

SL9901 50MHz Transimpedance Amplifier
SP9960 50M-Bit Manchester Biphase Encoder

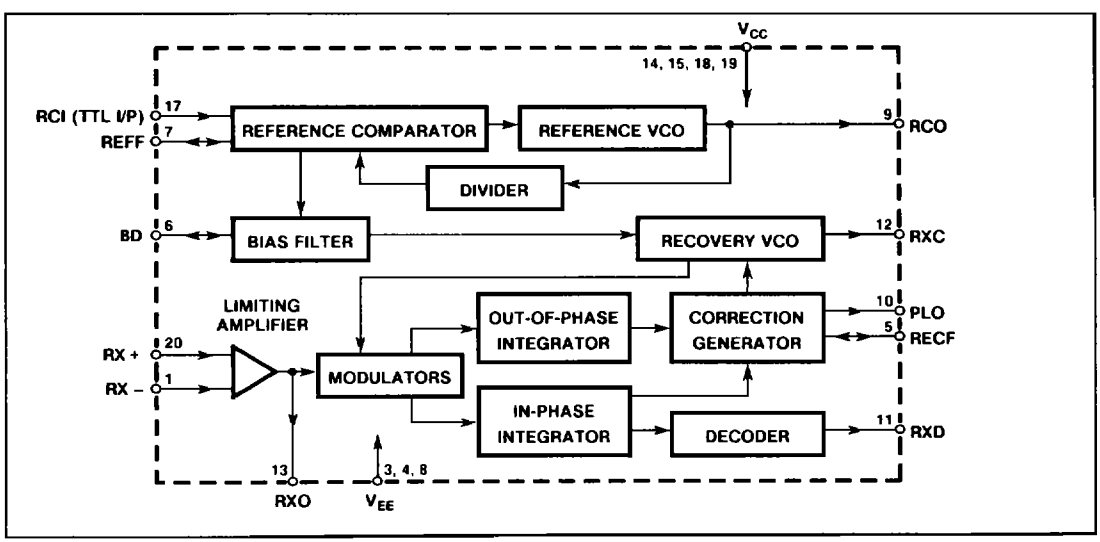


Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply voltage V_{CC} = +4.50V to +5.50V. T_{AMB} = -40°C to +85°C
Programming input low voltage V_{ILP} = 0V to 0.4V. TTL input low voltage V_{ILT} = 0.8V max, TTL input high voltage V_{IHT} = 2.0V min. Differential receiver voltage V_{RD} = 10mV to 2.00V peak to peak Bit Error Rate BER = 10^{-9} max

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
Supply current	I_{CC}		200	mA	Output Unloaded
TTL input sink current	I_T		10	µA	T_{AMB} = +25°C
			30	µA	T_{AMB} = +25°C.
ECL output high voltage	V_{OH}	V_{CC}-0 96	V_{CC}-0 81	V	T_{AMB} = +25°C See note 1
		V_{CC}-0 89	V_{CC}-0 70	V	T_{AMB} = +85°C See note 1
		V_{CC}-1 06	V_{CC}-0.89	V	T_{AMB} = -40°C See note 1
ECL output low voltage	V_{OL}	V_{CC}-1 85	V_{CC}-1 62	V	T_{AMB} = +25°C See note 1
		V_{CC}-1 82	V_{CC}-1.61	V	T_{AMB} = +85°C See note 1
		V_{CC}-1.89	V_{CC}-1 67	V	T_{AMB} = -40°C See note 1
Receive offset voltage	V_{RO}		5 0	mV	
Minimum VCO frequency	fL		20	MHz	
Maximum VCO frequency	fH	50		MHz	

NOTE 1 $[V_{RX}+] - [V_{RX}-] > 100mV$ to ensure a good ECL output on RXO output load as per Fig 4b

GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested, for the SP9921 at +25°C and over the full supply voltage range (+4.50V to +5 50V) Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
ECL output source current	I_{SOURCE}	1.2		mA	See Fig 5.
RCI frequency	f_R	3 9	10 1	MHz	
PCM clock high period	t_{RH}	20		ns	
PCM clock low period	t_{RL}	20		ns	
RCO rise or fall time	t_{RRF}		4	ns	R_L = 1kΩ, Fig 4a.
REFF source current pulse	I_{RF+}	100	350	µA	
REFF sink current pulse	I_{RF-}	100	350	µA	
Minimum half period	t_{MIN}	$0.3t_B$		ns	See note 2
Minimum half period	t_{MAX}		$0.7t_B$	ns	See note 2
Operating voltage (REFC)	V_{OP}	V_R-0.33	V_R + 0.33	V	See note 3
Free-running voltage (REFC)	V_{FR}	V_R-0.33	V_R + 0 33	V	See note 3
Free-running frequency offset (wrt f_{RCO})	Δ_{FR}	-2.0	+2 0	%	Input grounded
Lock on range (wrt f_{RCC})	Δ_L	-2 0	+2 0	%	Circuit as Fig 11 With C5 = 0

GUARANTEED CHARACTERISTICS (continued)

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
RXC fall time	t_{RXF}		4	ns	R_L = 1kΩ, Fig. 4a.
RXC rise time	t_{RXR}		4	ns	R_L = 1kΩ, Fig. 4a.
Output delay	t_{OD}		5	ns	R_L = 1kΩ, Fig. 4a.

NOTES
2. t_B typically = $1/f_{RCO}$ secs
3. V_R typically = V_{CC}-1 volts

ADDITIONAL INFORMATION

The following characteristics are typical for the SP9921B at +25°C, but not tested.

Characteristic	Symbol	Value	Units	Conditions
Thermal resistance chip-to-case	θ_{CC}	28	°C/W	
Thermal resistance chip-to-ambient	θ_{CA}	73	°C/W	
Pin capacitance	C_P	3	pF	Pin to supplies
ECL output sink current	I_{SINK}	2	mA	See Fig. 5
Receive bias voltage	V_{RB}	$V_{CC}/2$	V	
Receive input impedance	Z_{RI}	1000	Ω	Differential input
RCI rise time	t_{RR}	20	ns	
RCI fall time	t_{RF}	20	ns	
fH temperature coefficient	ΔfH	-0.2	MHz/°C	
RCO frequency	f_{RCO}	18	MHz	V_{REFF} = 2.5V
		46	MHz	V_{REFF} = 3.0V
		54	MHz	V_{REFF} = 3.5V
Reference loop gain	G_{REF}	40	MHz/V	f_{RCO} = 20MHz
		100	MHz/V	f_{RCO} = 30MHz
		55	MHz/V	f_{RCO} = 40MHz
		20	MHz/V	f_{RCO} = 50MHz
Frequency - voltage ratio	OCF/V	8.5	MHz/V	f_{RCO} = 50MHz
		9.5	MHz/V	f_{RCO} = 40MHz
		11.0	MHz/V	f_{RCO} = 30MHz
		6.5	MHz/V	f_{RCO} = 20MHz

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V
Input voltage	- 0.3V to V_{CC} + 0.3V
Output voltage	0V to V_{CC}
Storage temperature range	- 55°C to + 150°C
Maximum junction temperature	+ 175°C

PIN DESCRIPTIONS

Symbol	Pin no	Description
REFF	7	**Reference Filter (Current Output/Voltage Input)** A series RC network should be connected between this pin and ground to provide the filtering for the control of the reference VCO.
V_{EE}	8	**Negative Power Supply**
RCO	9	**Reference Clock Out (ECL Output)** This pin should output a clock which is frequency-locked to the reference clock input (RCI pin) but which is 5 times its frequency
PLO	10	**Phase Lock Out (ECL Output)** This pin goes low for any bits where the output of the in-phase integrator (data) fails to exceed the output of the out-of-phase integrator (error) by a set margin
RXD	11	**Received Data** (ecl output). This pin outputs the decode received data.
RXC	12	**Received Clock (ECL Output)** This pin outputs the recovered clock
RXO	13	**Receive Out (ECL Output)** This pin outputs the undecoded received data.
V_{CC}	14, 15	**Positive Power Supply**
NC	16, 2	**No Connection** This pin should be left unconnected for normal operation.
RCI	17	**Receive Clock In (TTL Input)** This is the input for the reference clock which sets the free-running frequency for the recovery VCO. Its frequency should be close to one fifth of the received data rate
V_{CC}	18, 19	**Positive Power Supply**
RX + **RX –**	20 1	**Receive Plus and Minus (Analog Voltage Inputs).** These are the differential inputs to the limiting receive amplifier They are self-biasing and would normally be capacitively coupled. For a single-ended input the unused pin should be capacitively coupled to ground
V_{EE}	3, 4	**Negative Power Supply**
RECF	5	**Recovery Filter (Current Output/Voltage Input)** A series RC network should be connected between this pin and ground to provide the filtering for the control of he recovery VCO.
BD	6	**Bias Decoupling (Decoupling Node).** A capacitor should be connected between this pin and ground to eliminate noise on the bias voltage generated by the reference PLL and which sets the free-running frequency of the recovery VCO.

FUNCTIONAL DESCRIPTION

Fig. 2 shows the simplified block diagram of the device It locks onto incoming data, recovers the clock and decodes the data making use of a reference clock input at one fifth of the data rate.

Receive Path

Data is received at the differential input pins (RX+/-) of the limiting amplifier which outputs the digital received signal for monitoring at the amplifier output pin (RXO) This signal is fed into a modified Costas loop which outputs the recovered clock (RXC pin) and the decoded data (RXD pin)

Fig. 3 shows how the input signal is decoded The Manchester biphase-mark code uses a transition at the centre of the bit to indicate a one and the absence of a transition to indicate a zero. In addition there is always a transition at the end of the bit

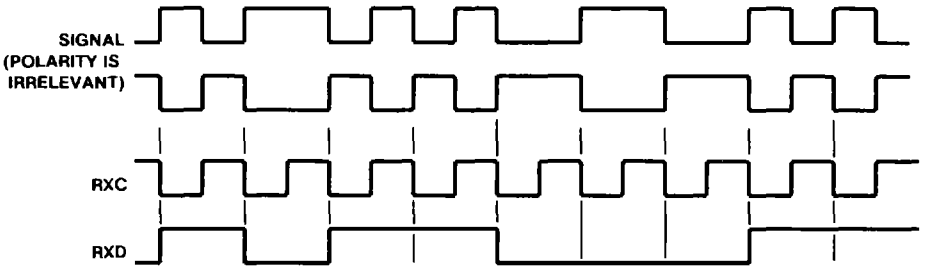
Phase-Locking and Signal Recovery

The SP9921 can be used in systems operating over a wide range of data rates without false frequency lock. This is achieved using a reference VCO and a recovery VCO.

The reference VCO is phase-locked to the reference clock input (RCI pin) This generates an internal clock at 5 times the frequency of the reference clock input The output of this VCO is output for monitoring on the reference clock output (RCO pin). Filtering of the bias control signal to the VCO is performed at the reference filter pin (REFF)

The bias control signal for the reference VCO is filtered at the bias decoupling pin (BD) and used to set the free-running frequency of the recovery VCO. The recovery VCO drivers the receive clock (RXC pin) and the modulators which in turn drive the integrators. The integrators analyse the components of the signal which are in phase and 90° out of phase and so obtain the recovered data and the correction signal for the modified Costas loop. The correction signal is filtered at the recovery filter pin (RECF)

The modified Costas loop also pulls the phase-lock output pin (PLO) low for any bits when the output of the in-phase integrator (data) does not exceed the output of the out-of-phase integrator (error) by a set margin This can occur when there is a loss of data, if there is too much noise on the link (even if no data is corrupted) or if the Costas loop has difficulty locking.



NOTE: There is a delay of 3 clock cycles between the input signal and the decoded data output

Fig. 3 Biphase-Mark Decoding

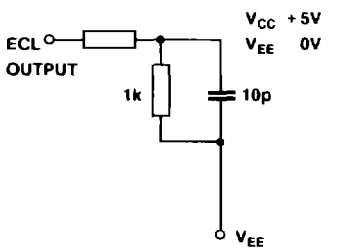


Fig. 4a

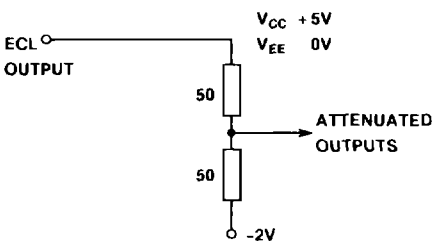


Fig. 4b

Fig. 4 ECL Output test loading

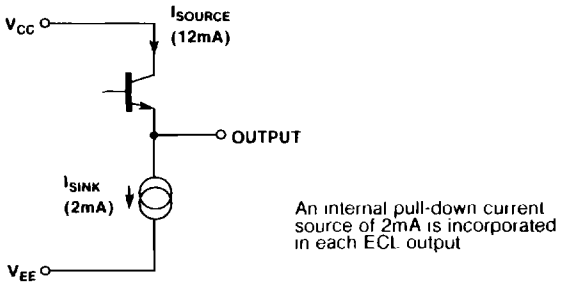


Fig. 5 ECL output circuitry

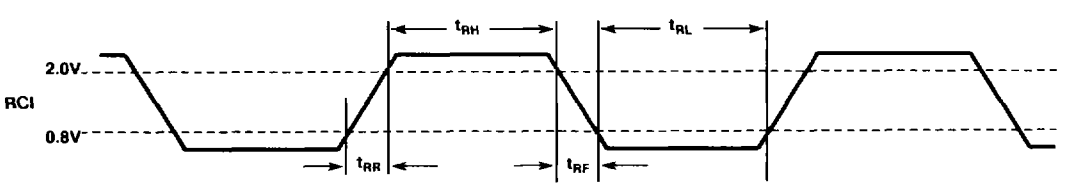


Fig. 6 Timing - reference clock in

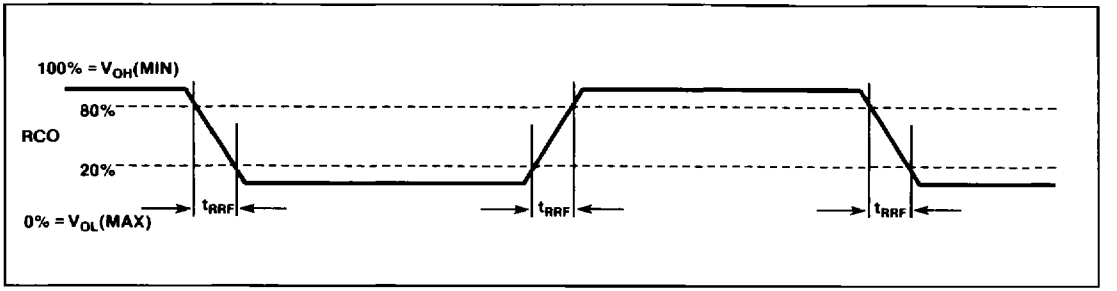


Fig. 7 Timing - reference clock out

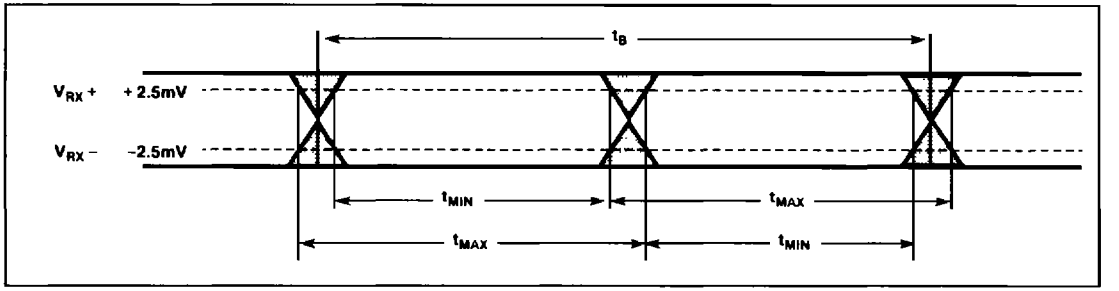


Fig. 8 Timing - receive data

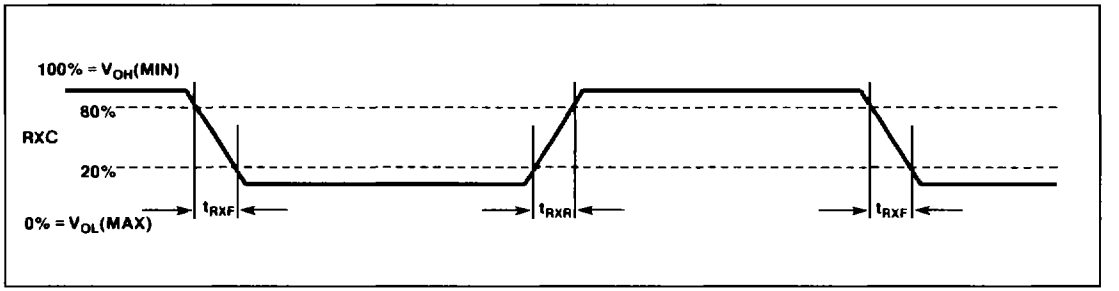


Fig. 9 Timing receive clock

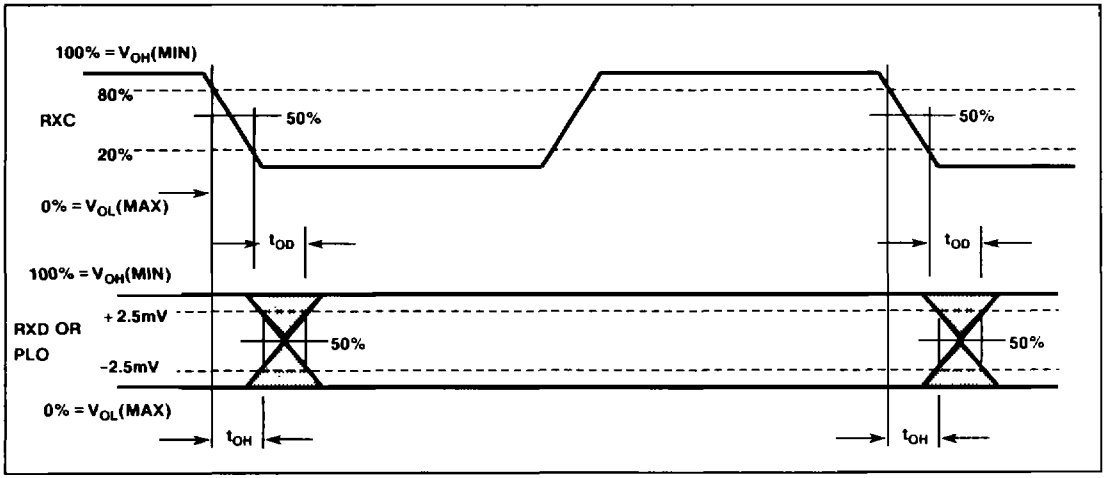
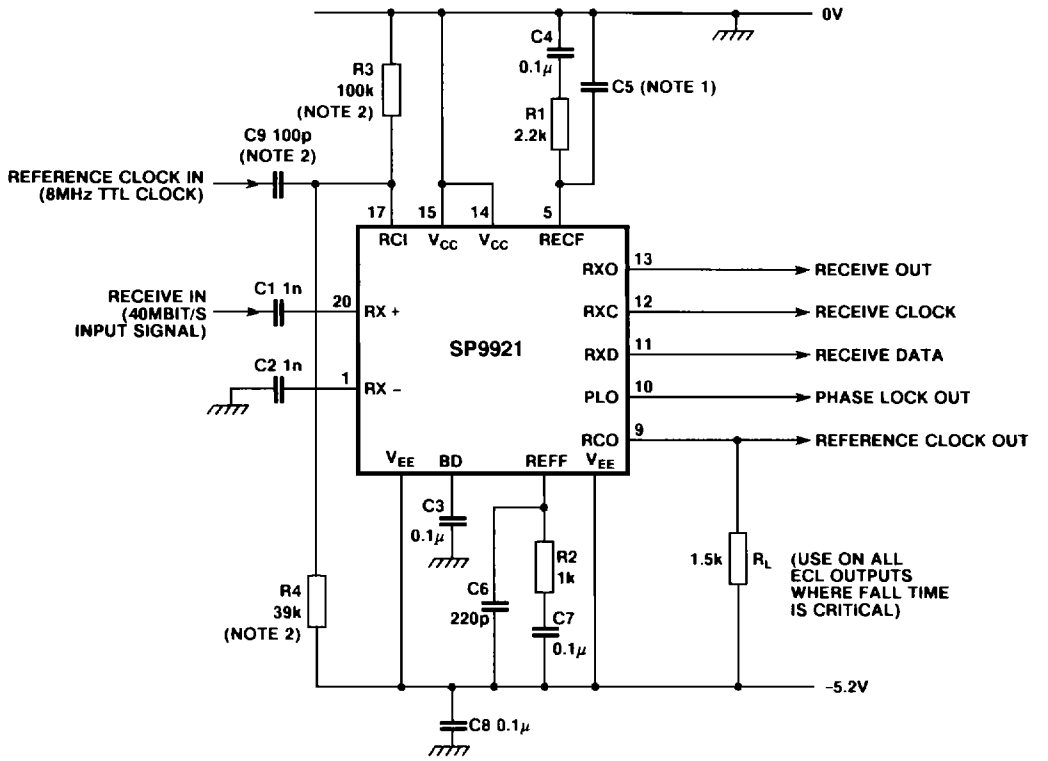


Fig. 10 Timing - receive data and phase lock out



1. C5 should be zero for most applications to maximise capture range, in applications where jitter is of paramount importance then a small value up to 47pF maybe used.
2. C9, R3 and R4 may be removed and the TTL reference clock connected directly to pin 17, provided that the TTL signal is referenced to V_{EE}

Fig.11. Typical application circuit