SP8741

300MHz÷6/7

The SP 8741 is an ECL ÷6/7 two-modulus divider, with ECL10K compatible outputs. It divides by 6 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 7 when both are low (or open circuit). An AC coupled input of 600mVp-p is required.

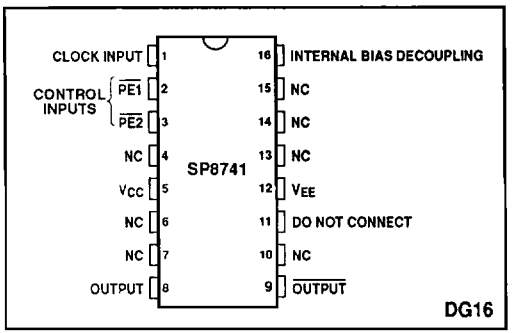


Fig. 1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC-Coupled Input (Internal Bias)
- ECL Compatible Control Inputs

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 240mW
- Temperature Range: −55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−8V
Output current	20mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8741 A DG
5962-91590 (SMD)

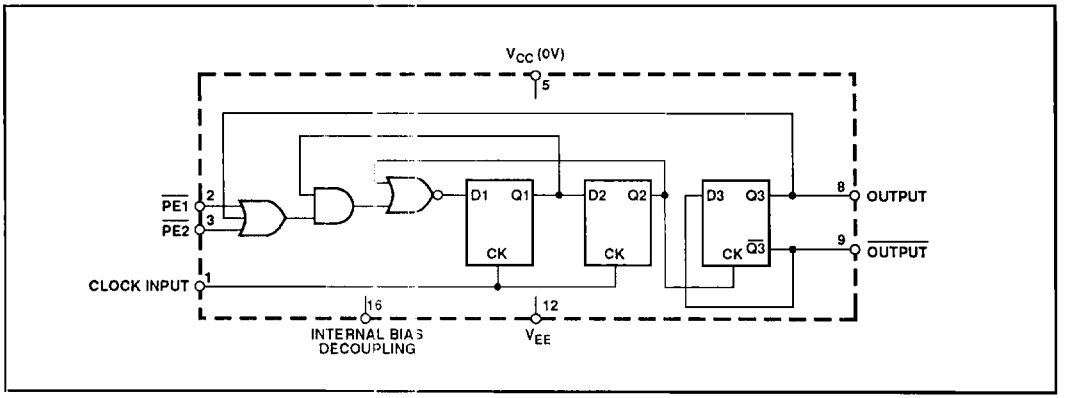


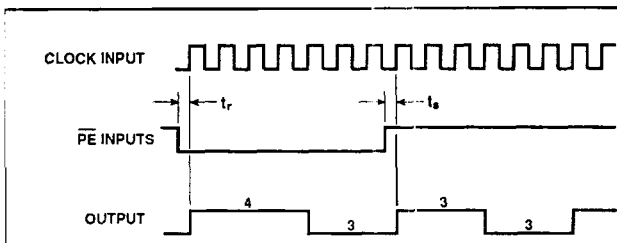
Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	300		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		60	mA	V_{EE} = −5·2V	
Output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V (25°C)	
Output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to output delay	t_p		6	ns		5
Set-up time	t_s	2·5		ns		3, 5
Release time	t_r	3		ns		4, 5

NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that ÷6 is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that ÷7 is obtained.
5. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division ratio
L	L	7
H	L	6
L	H	6
H	H	6

Fig. 3 Timing diagram

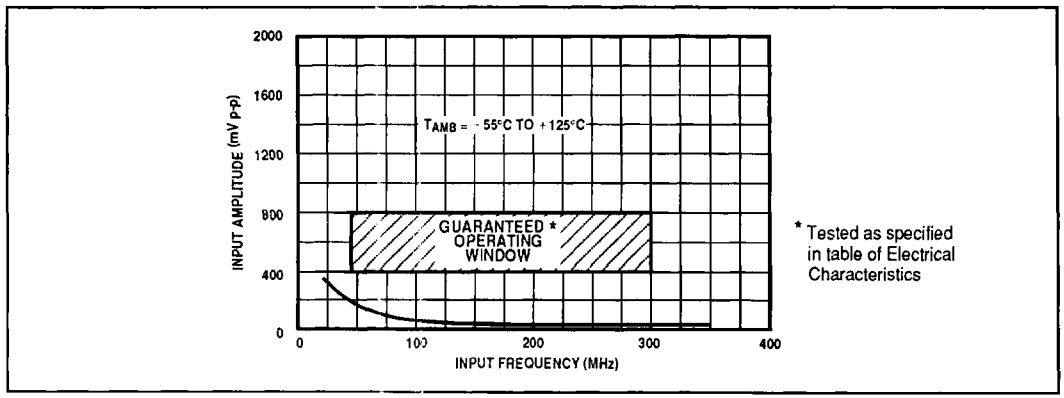


Fig 4 Typical input characteristic

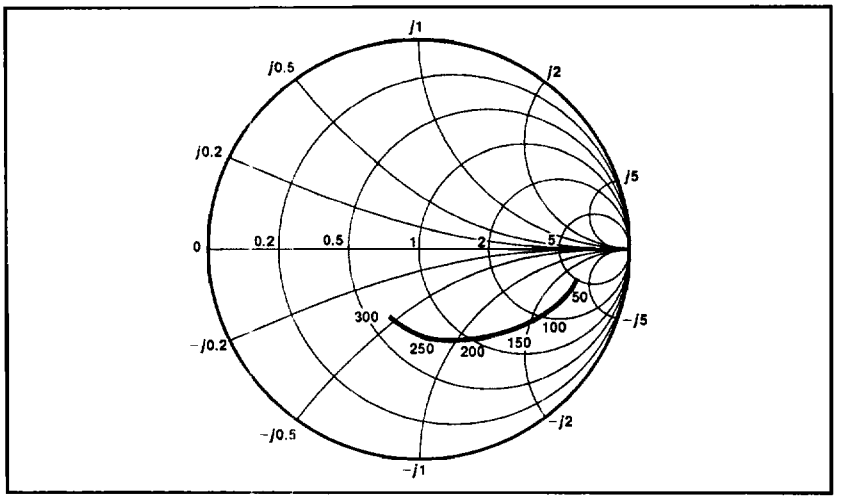


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = −5·2V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

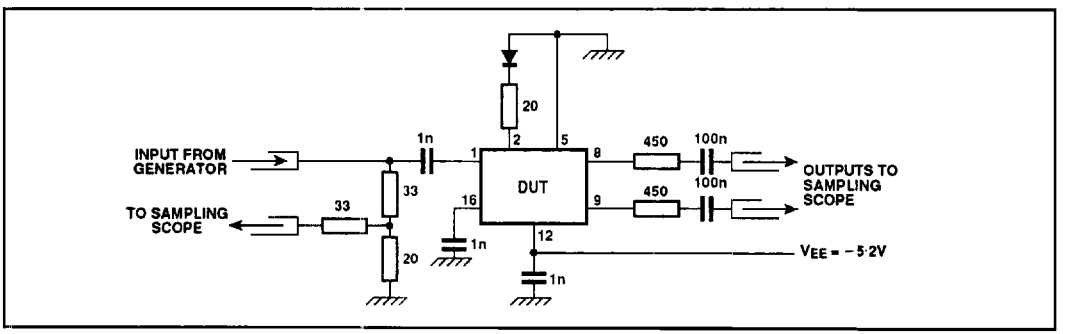


Fig. 6 Test circuit

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected from pin 16 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the clock input (pin 1) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\overline{Q}$ outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2kΩ at each output.
5. The PE inputs are ECLIII/10K compatible and include 4·3kΩ pulldown resistors. Unused inputs can therefore be left open.
6. The input impedance of the SP8741 varies as a function of frequency, see Fig. 5.
7. All components should be suitable for the frequency in use.

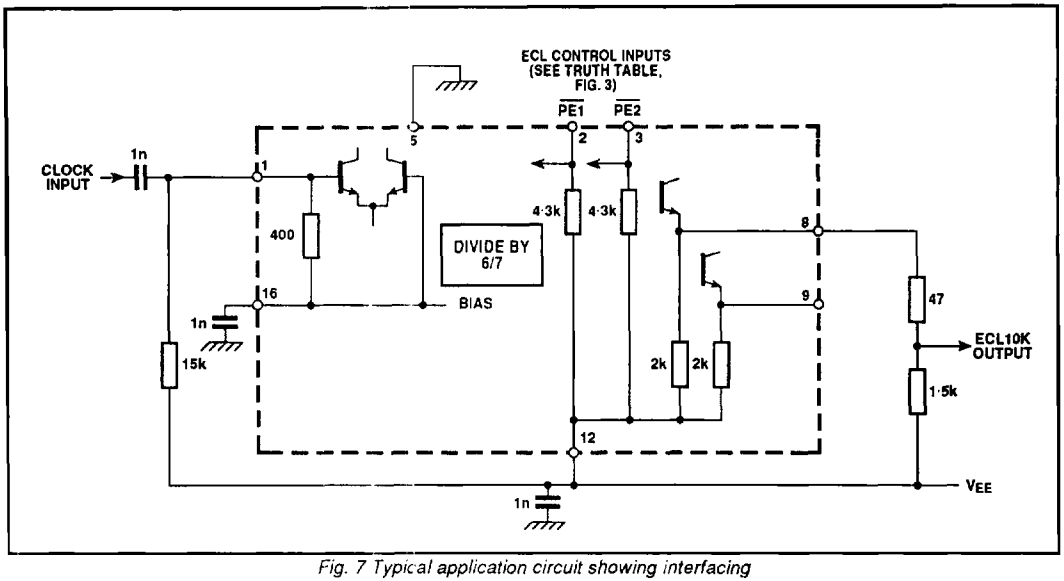


Fig. 7 Typical application circuit showing interfacing