

GD54/74HC194, GD54/74HCT194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

General Description

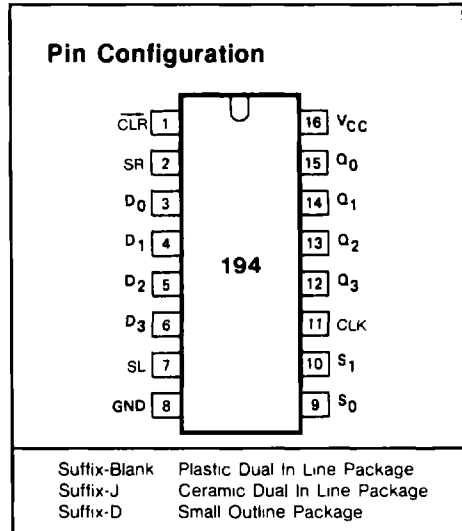
These devices are identical in pinout to the 54/74LS194. This circuit has virtually all of the features a system designer may want in a shift register. It features parallel load, parallel outputs, right & left shift serial inputs, mode control inputs, and a direct overriding clear line. This register has four distinct modes of operation:

- Inhibit Clock (Do nothing)
- Shift Right (In the direction Q_0 toward Q_3)
- Shift Left (In the direction Q_3 toward Q_0)
- Parallel (Broadside) Load

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: $1\mu\text{A}$ Max.
- Low quiescent current: $80\mu\text{A}$ Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs



Function Table

OPERATING MODES	INPUTS										OUTPUTS			
	CLK	CLR	S ₁	S ₀	SR	SL	D ₃	D ₂	D ₁	D ₀	Q ₃	Q ₂	Q ₁	Q ₀
reset (clear)	X	L	X	X	X	X	X	X	X	X	L	L	L	L
hold ("do nothing")	X	H	L	L	X	X	X	X	X	X	q ₀	q ₁	q ₂	q ₃
shift left	↑	H	h	L	X	L	X	X	X	X	q ₁	q ₂	q ₃	L
	↑	H	h	L	X	h	X	X	X	X	q ₁	q ₂	q ₃	H
shift right	↑	H	L	h	L	X	X	X	X	L	q ₀	q ₁	q ₂	q ₃
	↑	H	L	h	h	X	X	X	X	H	q ₀	q ₁	q ₂	q ₃
parallel load	↑	H	h	h	X	X	d ₃	d ₂	d ₁	d ₀	d ₃	d ₂	d ₁	d ₀

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
- q,d = lower case letters indicate the state of the referenced input for output one set-up time prior to the LOW-to-HIGH CLK transition
- X = don't care
- ↑ = LOW-to-HIGH CLK transition

Logic Diagram

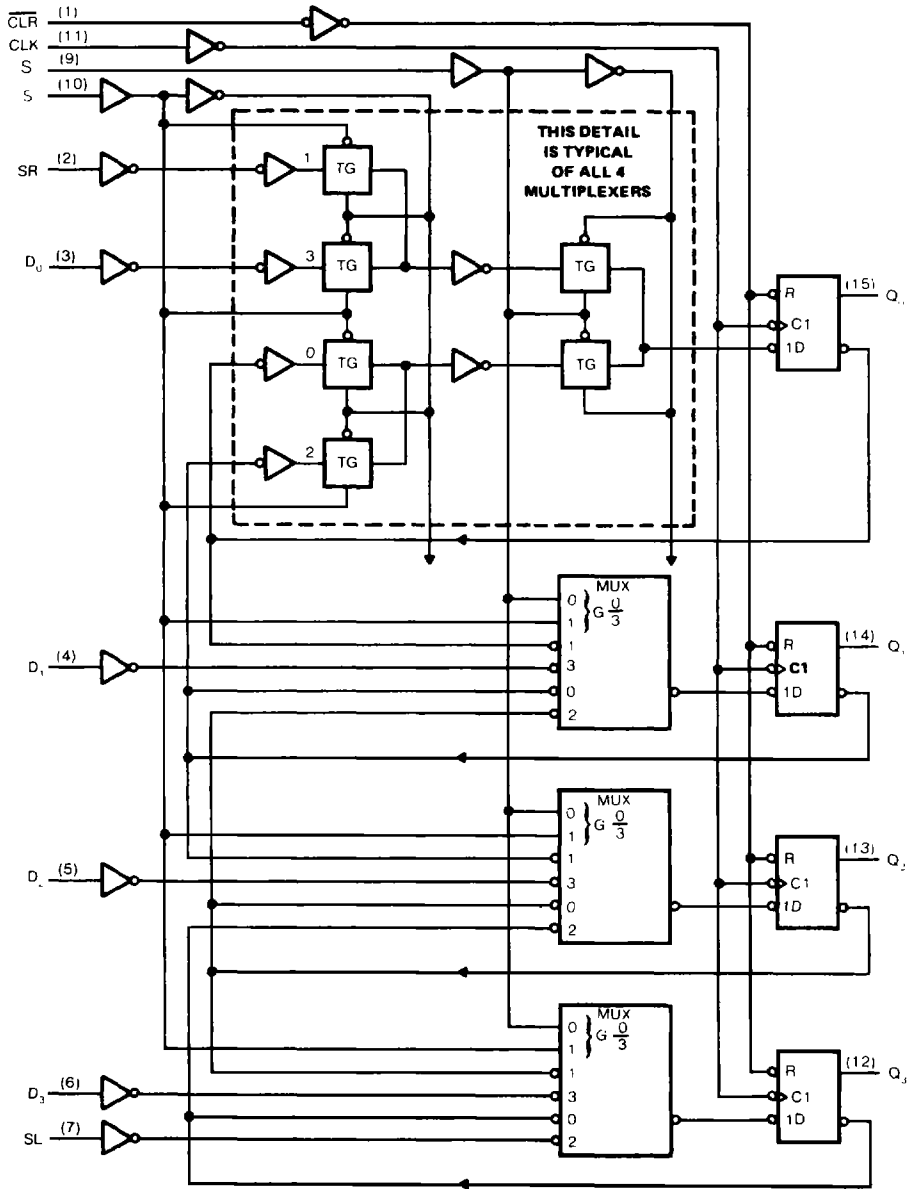


Fig. 1. Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		{20}	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		{25}	mA
I_{CC}	DC V_{CC} or GND current			{50}	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C. derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN	MAX	
Supply-Voltage Range V_{CC} GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f GD54 74HC Types at 2V at 4.5V at 6V GD54 74HCT Types at 4.5V		1000 500 400 500	ns

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit and Clear Sequences

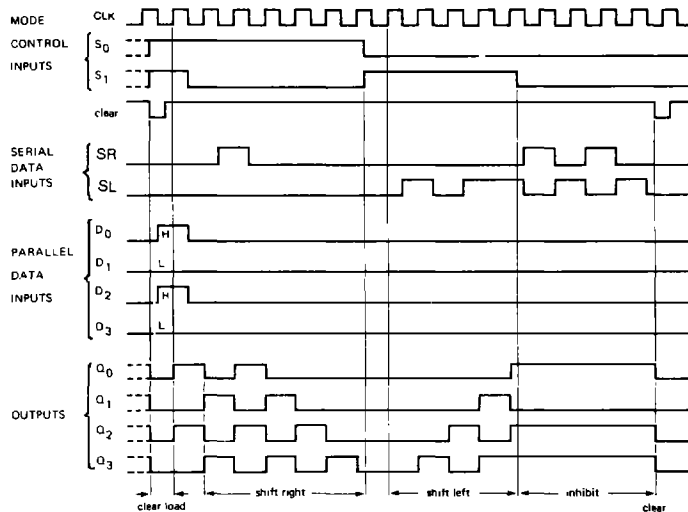


Fig. 2 Typical load right-shift left-shift inhibit and clear sequences

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC194		GD54HC194		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		2.0	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6.0	4.2			4.2		4.2		
V _{IL}	LOW level input voltage		2.0			0.3		0.3		0.3	V
			4.5			0.9		0.9		0.9	
			6.0			1.2		1.2		1.2	
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	2.0	1.9	2.0		1.9		1.9		V
			4.5	4.4	4.5		4.4		4.4		
			6.0	5.9	6.0		5.9		5.9		
	or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5	3.98	4.3		3.84		3.7		
			6.0	5.48	5.2		5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	2.0			0.1		0.1		0.1	V
			4.5			0.1		0.1		0.1	
			6.0			0.1		0.1		0.1	
	or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5		0.17	0.26		0.33		0.4	
			6.0		0.15	0.26		0.33		0.4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT194		GD54HCT194		UNIT		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
V _{IH}	HIGH level input Voltage		4.5 to 5.5	2.0			2.0		2.0		V		
V _{IL}	LOW level input voltage		4.5 to 5.5			0.8		0.8		0.8	V		
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH} I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4		V		
			4.5	3.98	4.3		3.84		3.7				
		or V _{IL}	I _{OH} =-4mA	4.5									
				6.0									
V _{OL}	LOW level output voltage	V _{IN} =V _{IH} I _{OL} =20μA	4.5			0.1		0.1		0.1	V		
			4.5			0.17	0.26		0.33			0.4	
		or V _{IL}	I _{OL} =4mA	4.5			0.17	0.26		0.33			0.4
				6.0									
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA		
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA		

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Timing Requirements for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HC194		GD54HC194		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	$\overline{\text{CLR}}$ low, CLK	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			17		20		
t _{su}	Setup time	Sn, Dn to CLK	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	12			17		20		
t _h	Hold time	Dn to CLK	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r = t_f = 6\text{ns}$ $C_L = 50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A = 25°C			GD74HC194		GD54HC194		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum Clock Pulse Frequency		2.0	6			5		4.2		Mhz
			4.5	31			25		21		
			6.0	36			29		25		
t _{PLH'} t _{PHL}	Propagation Delay Time CLK to Qn		2.0		47	145		180		220	ns
			4.5		16	29		36		44	
			6.0		13	25		31		36	
t _{PLH'} t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn		2.0		39	140		175		210	ns
			4.5		13	28		35		42	
			6.0		11	24		30		35	
t _{THL'} t _{THL}	Output Transition Time		2.0		19	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

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Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT194		GD54HCT194		UNIT
				MIN	TYP	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{\text{CLR}}$ low. CLK	4.5	16			20		24		ns
t_{su}	Setup time	Sn, Dn to CLK	4.5	16			20		24		ns
t_h	Hold time	Dn to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT194		GD54HCT194		UNIT
				MIN	TYP	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum clock pulse frequency		4.5	30			23		20		Mhz
t_{PLH}^1 t_{PHL}	Propagation Delay Time $\overline{\text{CLK}}$ to Qn		4.5		19	32		40		48	ns
t_{PLH}^1 t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn		4.5		16	31		39		46	ns
t_{THL}^2 t_{TFL}	Output Transition Time		4.5		7	15		19		22	ns

AC Waveforms

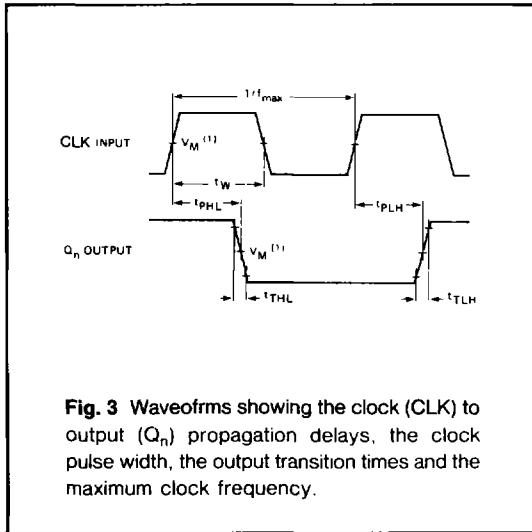


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

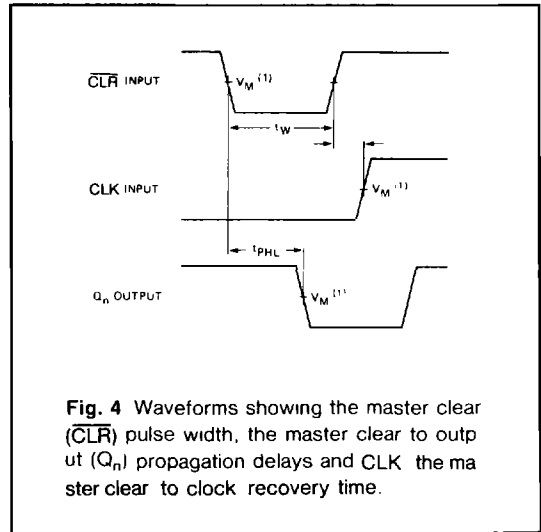


Fig. 4 Waveforms showing the master clear (\overline{CLR}) pulse width, the master clear to output (Q_n) propagation delays and CLK the master clear to clock recovery time.

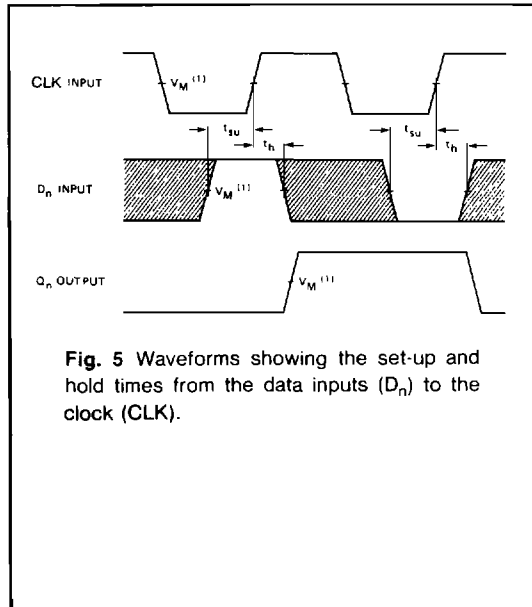


Fig. 5 Waveforms showing the set-up and hold times from the data inputs (D_n) to the clock (CLK).

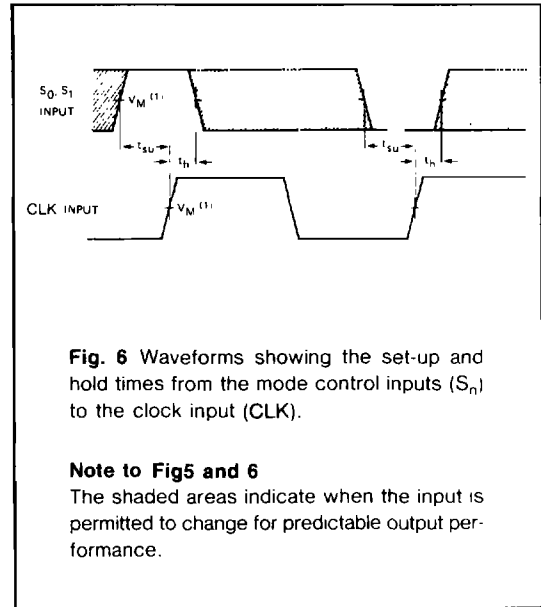


Fig. 6 Waveforms showing the set-up and hold times from the mode control inputs (S_n) to the clock input (CLK).

Note to Fig5 and 6
The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$ $V_I = GND$ to V_{CC}
HCT : $V_M = 1.3V$; $V_I = GND$ to $3V$