

## Sine-wave Generator for CCFL Supply

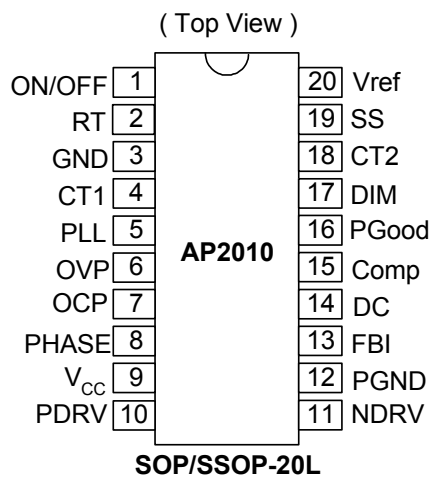
### ■ Features

- ON/OFF pin to enter stand-by Mode
- Operating voltage from 4.5 to 20V
- Max. Duty up to 48%
- Under voltage Lockout (UVLO) Protection
- Variable Oscillator Frequency to 100KHz Max.
- Self-trigger Oscillator (Sine-wave generator).
- Soft-start, OCP, OVP, PGOOD, Shutdown function.
- Dim Oscillator and Dimming Control Input
- **Pb-Free** Package :20-pin SOP & SSOP

### ■ Applications

- CCFL power supply.

### ■ Pin Assignments



### ■ General Description

The AP2010 series integrates Sine-wave generator control circuit into a single chip, mainly designed for CCFL power-supply regulator. All the functions included an adjustable dimming oscillator, self-trigger oscillator, UVLO, soft-start, OVP, PGOOD, current limit & shutdown circuitry.

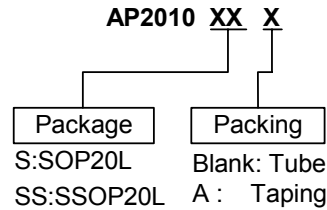
The Duty can provide from 5% to 48%. Switching frequency can be adjustable up to 100KHz by external L, C, and set CT. During low  $V_{CC}$  situation, the UVLO makes sure that the outputs are off until the internal circuit is operational normally.

### ■ Pin Descriptions

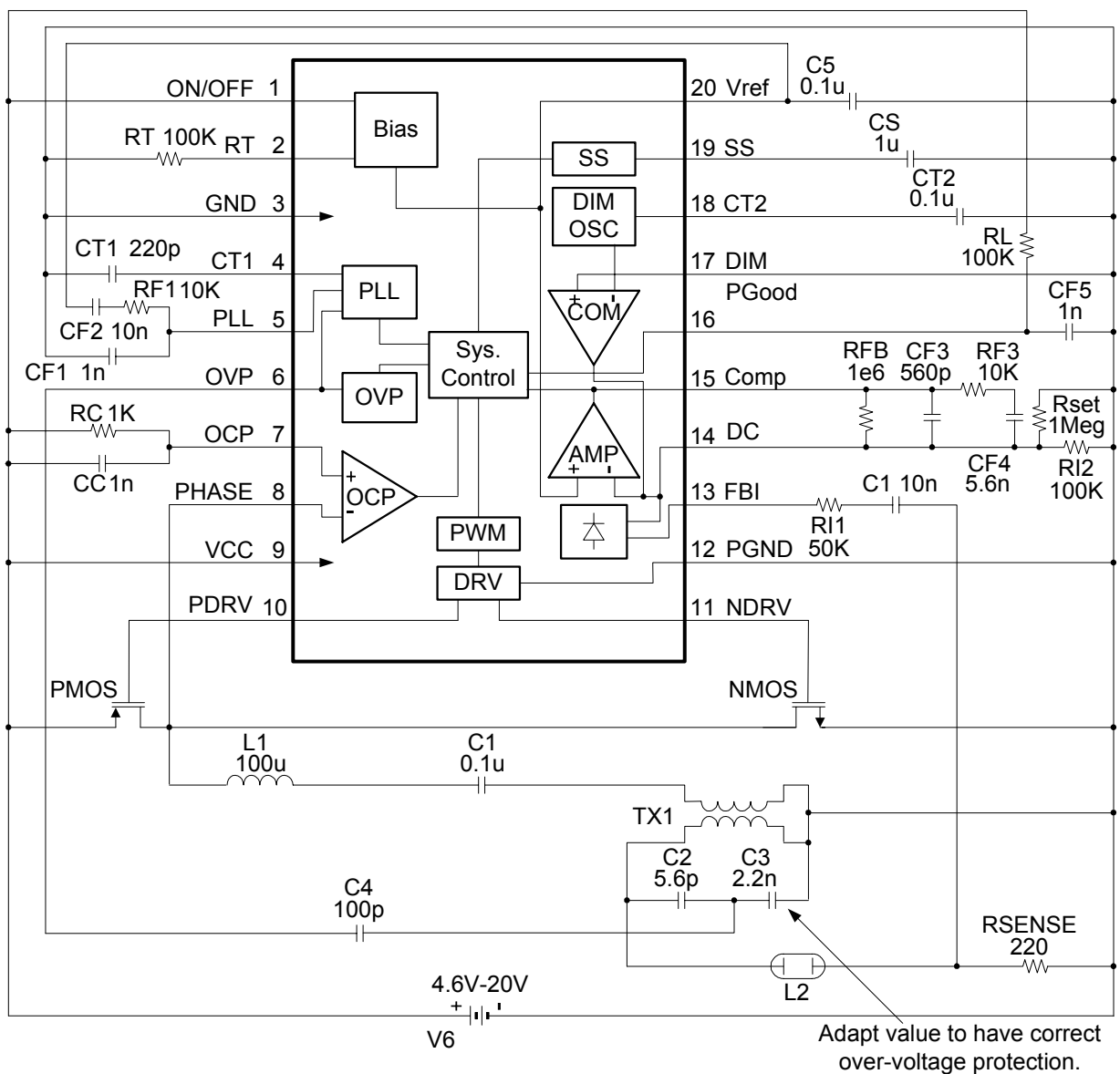
Name	Pin No.	Description
ON/OFF	1	Standby/ON
RT	2	Internal bias current setting pin
GND	3	Signal ground
CT1	4	Set PWM frequency
PLL	5	PLL compensation pin
OVP	6	Over voltage protect pin
OCP	7	Over current protection
PHASE	8	Phase input pin.
$V_{CC}$	9	$V_{CC}$ Input Pin
PDRV	10	High side PMOS driver
NDRV	11	Low side NMOS driver
PGND	12	Power ground
FBI	13	Current Feedback Sense Pin
DC	14	DC lamp current output
Comp	15	Compensation pin
PGood	16	Power good output Pin
DIM	17	Set DIM duty cycle
CT2	18	Set Dim frequency
SS	19	Soft-start (Slow Start Time)
Vref	20	Reference voltage output pin

## Sine-wave Generator for CCFL Supply

### ■ Ordering Information



### ■ Block Diagram





Sine-wave Generator for CCFL Supply

■ Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V <sub>CC</sub>	Supply voltage	22	V
V <sub>I</sub>	Amplifier input voltage	22	V
V <sub>O</sub>	Output voltage	22	V
T <sub>OP</sub>	Operating temperature range	-20 to +85	°C
T <sub>ST</sub>	Storage temperature range	-65 to +150	°C
T <sub>LEAD</sub>	Lead temperature 1.6 mm(1/16 inch) from case for 10 seconds	260	°C

■ Electrical Characteristics (T<sub>A</sub>=25°C, V<sub>CC</sub>=12V, f=100 KHz)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Power Supply</b>						
V <sub>CC</sub>	Supply Voltage		4.5	-	20	V
I <sub>CC</sub>	Supply Current	EN = V <sub>CC</sub>	-	10	15	mA
I <sub>sd</sub>	shutdown current	EN = Gnd	-	50	150	uA
<b>Reference (REF)</b>						
V <sub>REF</sub>	Reference Voltage		1.15	1.18	1.21	V
	Reference voltage change with temperature	T <sub>A</sub> = -20°C ~ 25°C	-	-0.1	±1	%
		T <sub>A</sub> = 25°C ~ 85°C	-	-0.2	±2	%
	Change with supply	V <sub>CC</sub> =4.5V ~ 20V	-	5	10	mV
<b>Under voltage lockout (UVLO)</b>						
V <sub>UT</sub>	Upper threshold voltage (V <sub>CC</sub> )		4.4	-	4.5	V
V <sub>LWT</sub>	Lower threshold voltage (V <sub>CC</sub> )		4.3	-	4.4	V
V <sub>HT</sub>	Hysteresis (V <sub>CC</sub> )		-	100	-	mV
<b>Over Voltage Protection (OVP)</b>						
V <sub>T-OVP</sub>	OVP Threshold Voltage		-	3	-	V
I <sub>OVP</sub>	OVP Source Current	V <sub>OVP</sub> = 3V	-	1	-	mA
V <sub>OVP</sub>	Open Circuit Voltage		-	1.5	-	V
<b>Current Sense (FBI)</b>						
V <sub>R</sub>	reference voltage, normal control		-	1.25	-	V
V <sub>L</sub>	over-current threshold		-	1.5	-	V
I <sub>B</sub>	Input current		-5	-	+5	μA
<b>Oscillator (DIM OSC)</b>						
F <sub>OSC</sub>	Frequency	C <sub>T2</sub> = 0.1uF, RT=100K	-	200	-	Hz
I <sub>CT2</sub>	Charge Current	RT=100K	-	± 80	-	uA
V <sub>CT2</sub>	Oscillator Amplitude		-	2	-	Vpp
<b>Enable (ON/OFF)</b>						
V <sub>ON/OFF</sub>	ON (floating) internal pull high		2	-	V <sub>CC</sub>	V
	OFF		0	-	0.8	
I <sub>ON</sub>	Input current	V <sub>ON/OFF</sub> =2V	-	2	5	uA
<b>Dimming Control (DIM)</b>						
V <sub>DIM</sub>	Voltage for 100% ON		0.90	0.95	1.00	V
	Voltage for 10% ON		2.5	2.6	2.7	
I <sub>DIM</sub>	Input current	V <sub>DIM</sub> =2V	-	-	1	uA
<b>Error Amplifier</b>						
A <sub>OL</sub>	Gain (A <sub>OL</sub> )		-	50	-	dB



## Sine-wave Generator for CCFL Supply

**Electrical Characteristics (Continued)** ( $T_A=25^{\circ}\text{C}$ ,  $V_{CC}=12\text{V}$ ,  $f=100\text{ KHz}$ )

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>MOSFET Drivers</b>						
$I_{PDRV}$	PDRV2 Sink/ Source	$V_{CC} - V_{PDRV1} = 4.5\text{V}$ $V_{PDRV1} - \text{GND} = 2\text{V}$	300	-	-	mA
$I_{NDRV}$	NDRV2 Sink/ Source	$V_{CC} - V_{NDRV1} = 4.5\text{V}$ $V_{NDRV1} - \text{GND} = 2\text{V}$	300	-	-	mA
Don/off	PDRV2 & NDRV2 duty cycle of self trigger sin oscillator	$30\text{KHz} < f_{\text{OSC}} < 100\text{KHz}$	46	50	54	%
$T_{\text{DEAD}}$	Dead time between PDRV and NDRV		45	-	300	nS
<b>Soft Start</b>						
$I_{\text{SSC}}$	Charge Current	$V_{\text{SS}} = 1.5\text{V}$	8.0	10	12	$\mu\text{A}$
$I_{\text{SSD}}$	Discharge Current	$V_{\text{SS}} = 1.5\text{V}$	1.5	3	4.5	$\mu\text{A}$
<b>PWM Oscillator and PLL</b>						
$I_{\text{CT1}}$	Charge Current	$\text{RT} = 100\text{K}$	-	$\pm 70$	-	$\mu\text{A}$
$V_{\text{CT1}}$	Oscillator Amplitude		-	2	-	Vpp
$f_c$	Center frequency	$\text{CT1} = 220\text{pF}$ , $\text{RT} = 100\text{K}$	-	50	-	kHz
$\Delta f$	PLL Lock In Range	$\text{CT1} = 220\text{pF}$ , $\text{RT} = 100\text{K}$	10	-	-	kHz
<b>Power Good</b>						
$I_{\text{PGOOD}}$	Open Collector output	No current if power good	1	-	-	mA
<b>Over Current Protection and PHASE input</b>						
$V_{\text{OCP}}$	Operating Voltage Range		4	-	$V_{\text{CC}}$	V
$I_{\text{OCP}}$	Sink Current	$\text{RT} = 100\text{K}$ (Note 2)	155	175	195	$\mu\text{A}$
$V_{\text{PHASE}}$	Operating Voltage Range		0	-	$V_{\text{CC}}$	V
$I_{\text{PHASE}}$	Sink Current	$\text{RT} = 100\text{K}$ (Note 2)	18	20	22	$\mu\text{A}$

**Note 1:** If  $V_{17} < 0.9\text{V}$  the output drive is permanent ON, if  $V_{17} > 3.1\text{V}$  the output drive is permanently inhibited.

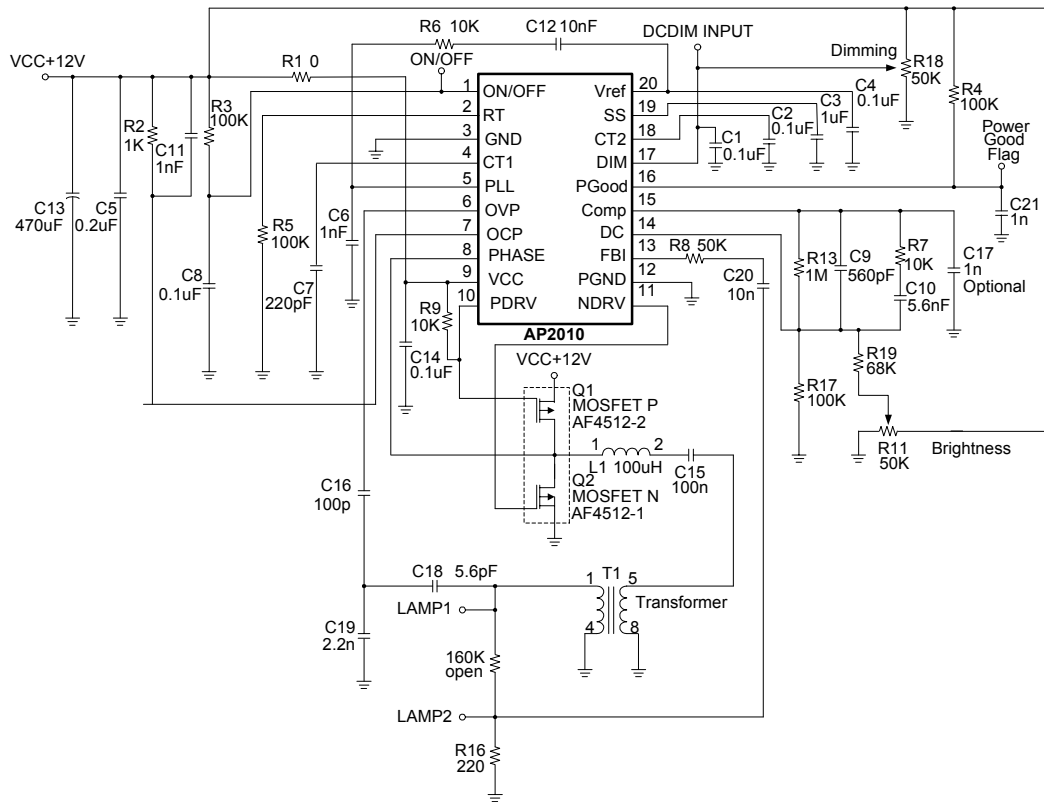
**Note 2:** If, while the PMOS is ON, the voltage at pin 8 (OCP) is below that at pin 7 (PHASE), the over-current protection is activated.

**Note 3:** If at any time the voltage at pin 6 (OVP) is above 3V, the over-voltage protection is activated.

**Note 4:** If  $V_{\text{CC}} < 4.5\text{V}$  the SS pin is forced low.

## Sine-wave Generator for CCFL Supply

### ■ Typical Application Circuit



## Sine-wave Generator for CCFL Supply

### ■ Function Description

#### General

Although the IC may operate from  $V_{CC}=4.5V$  up to  $V_{CC}=20V$  it is recommended not to use this wide range in one application. Circuit design and circuit safety will be much higher if the nominal  $V_{CC}$  is kept within low tolerances. At  $V_{CC}=5V$  a possible deviation of less than 10% is mandatory, while at higher supplies there is more headroom. Nevertheless it is recommended not to exceed a supply tolerance of 10%.

#### Self Trigger Sin Oscillator

The transformer TX1 stepping up the voltage applied to the CCFL is not driven directly by a 50% square-wave voltage of sufficient amplitude as in conventional circuits. Instead of there is a tuned circuit connected between the output transistors and the transformer. This has two advantages:

- The voltage applied to the lamp has only little harmonics
- The pulses driving the circuit need not to be a 50% square-wave

The latter offers the opportunity to omit the amplitude control of the pulses driving the circuit and use instead of a pulse width modulation to control the energy pumped into the circuit. To secure a safe start up of the circuit an oscillator is used which center frequency should be identical to that of the tuned circuit. To cope with the tolerances of the external components mainly L1 and C1 this oscillator is controlled by a PLL which takes care that the phase of the pulses driving the tuned circuit are always correct in time. The center-frequency of the PLL is set by RT and CT1:

$$f_{PLL} = \frac{7}{4 \times RT \times CT1}$$

Because RT sets several internal currents its value should stay around 100K.

#### Lamp Current Control Loop

The lamp current is sensed at  $R_{SENSE}$  and feed via CI and RI1 into the current rectifier. This is a full-wave rectifier converting the AC input current at terminal 13 (FBI) into a DC current at terminal 14 (DC). Using a full-wave rectifier eases the loop filter design of the current control loop because the AC

component at the filter input has twice the frequency as it would have with a half-wave rectifier. Due to this construction and because the reference voltage at the control amplifier AMP is 1.18V the actual effective lamp current is:

$$I_{eff} = 1.18V \cdot \frac{1.1 \times RI1}{R_{SENSE} \times RI2}$$

#### Dim Circuit

For adjusting the lamp current in a wider range a dim circuit is used. The triangle of the DIM oscillator is sliced by the comparator COMP at the DC level applied to terminal 17 (DIM). Whenever the oscillator triangle is lower than the DC applied to terminal 17 a large current is added to the AMP input. This indicates to the current control loop that a large lamp current is already present and thus cutting off the PWM modulator. The frequency of the DIM oscillator is set by RT and CT2:

$$f_{DIM} = \frac{2}{RT \times CT2}$$

Because RT sets several internal currents its value should stay around 100K. Be aware that with the DIM Circuit in action also the  $P_{GOOD}$  will switch ON and OFF.

#### Under - Voltage Lockout

To guarantee that at start of operation all parameters of the circuit are within their target values, the under voltage lockout releases the drive of the external MOS transistors only if  $V_{CC}$  is above 4.5V. If  $V_{CC}$  falls thereafter below 4.4V the drive of the external MOS transistors is inhibited again. If the drive is inhibited the external NMOS is switched ON (as far as this is possible) while the external PMOS is switched OFF.

#### Over -Voltage Protection

The indication of an over-voltage is that the peak voltage at terminal 6 (OVP) is above 3V. If this is detected the drive of the output is inhibited and Hiccup Mode is entered. The average DC voltage at terminal 6 (OVP) is set internally to 1.5V so an AC peak voltage of 1.5V will trigger the circuit. Any voltage supplied to this terminal must come in via a capacitor.

## Sine-wave Generator for CCFL Supply

### ■ Function Description (Continued)

#### Power Good

The power good flag (output terminal 16, P<sub>GOOD</sub>) is high as long as the voltage at terminal 14 (DC) is within 10% of the internal GAP voltage. The output is an open collector NPN output. As there will be a residual ripple voltage of twice the MWM frequency at terminal 14 (DC) entering and leaving the P<sub>GOOD</sub> mode is accompanied by several glitches. To suppress them sufficiently the filter capacitor CF5 is necessary. Be aware that if DIM control is active also P<sub>GOOD</sub> is switching ON and OFF.

#### Solow Start

At start up the capacitor CS is at zero volts and held there as long as the supply is below 4.2V. Thereafter the capacitor is charged with 10uA until it is up to 3V. As long as the output voltage of the current loop amplifier intends to be higher than the voltage at terminal 20 (SS) the output of the current loop amplifier AMP is clamped to this voltage. By this the duty cycle of the PWM controller is increased slowly from zero to a value necessary to generate the desired output current. This is to ramp up the lamp voltage slowly until ignition at start up time.

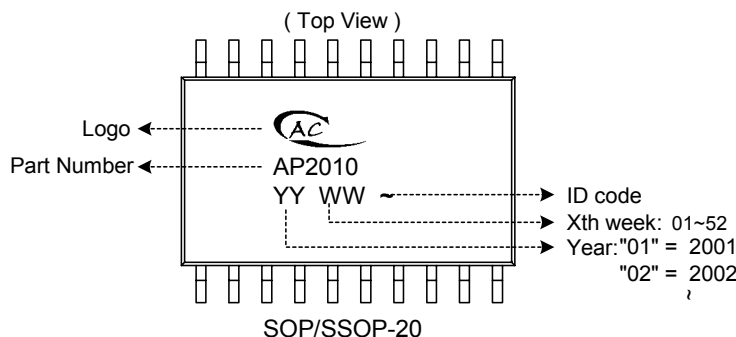
#### Current Limiting

This circuit compares the voltage drop (Vsd) at the external PMOS during its on time with a voltage set by the application. This reference voltage is the voltage drop on the resistor between V<sub>CC</sub> and terminal 8 (OCP). The voltage drop on this resistor is due to an internal current sink of 200uA. The current sample is taken right in the center of the ON time of the external PMOS transistor. If an over-current is detected the drive of the external power MOS transistors is switched off and Hiccup Mode is entered. Because of IC internal restrictions this measurement can only take place if the ON time of the external PMOS is larger than 1.5us.

#### Hiccup Mode

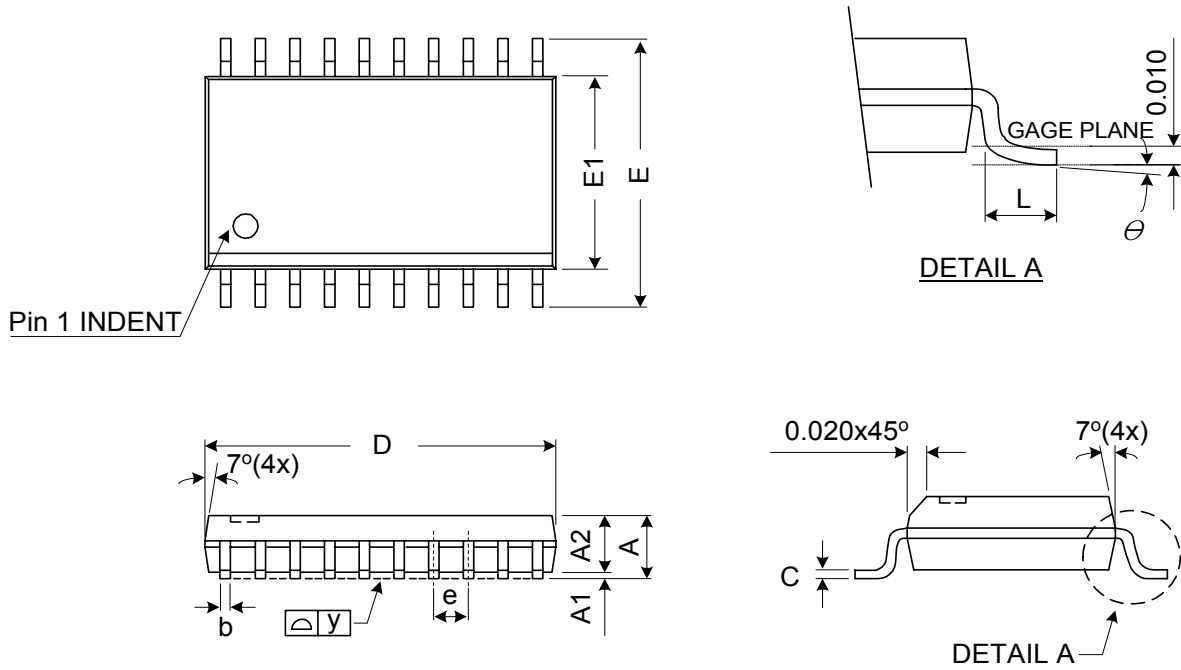
If an over-current or an over-voltage is detected then the external PMOS transistors is switched off while the external NMOS is turned on. By this setting the output voltage will decrease rapidly. At the same time the external soft start capacitor at terminal 20 (SS) is discharged by a current of 2uA. As soon the voltage at it is below 0.8V a new soft start is initiated. By this the pause between the occurrence of an over-current and a restart is about 5 times the slow-start time.

### ■ Marking Information



### ■ Package Information

(1) Package Type: SOP-20L

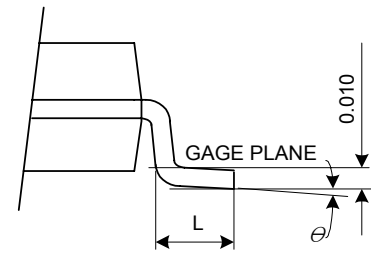
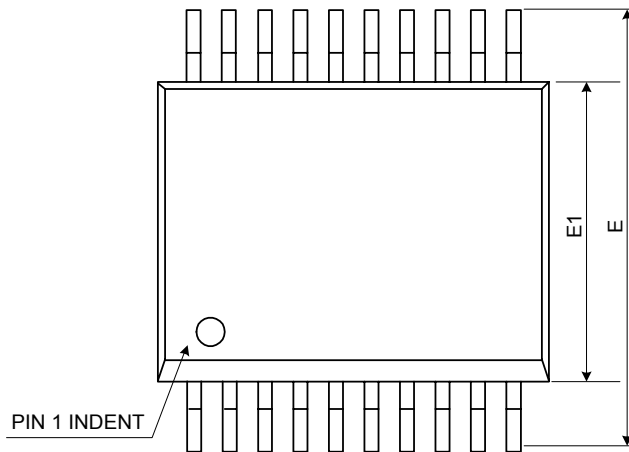


Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.36	2.50	2.64	0.093	0.098	0.104
A1	0.10	-	0.30	0.004	-	0.012
A2	-	2.31	-	-	0.091	-
b	0.33	0.42	0.51	0.013	0.017	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	12.60	12.75	12.90	0.496	0.502	0.508
E	10.01	10.33	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	-	1.27	-	-	0.050	-
L	0.38	0.83	1.27	0.015	0.032	0.050
y	-	-	0.076	-	-	0.003
θ	0°	-	8°	0°	-	8°

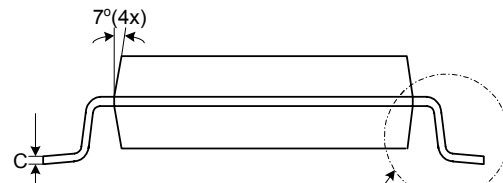
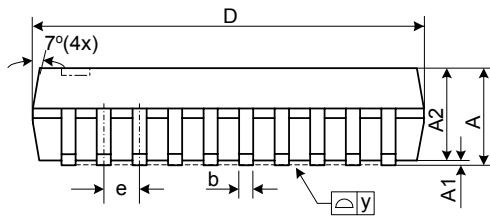


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(2)Package Type: SSOP-20L (300mil)



DETAIL A



DETAIL A

Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.00	-	-	0.079
A1	0.05	-	-	0.002	-	-
A2	-	1.75	-	-	0.069	-
b	0.22	0.30	0.38	0.009	0.012	0.015
C	0.13	0.17	0.20	0.005	0.006	0.008
D	7.08	7.21	7.34	0.279	0.284	0.289
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	-	0.65	-	-	0.026	-
L	0.56	0.77	0.97	0.022	0.030	0.038
y	-	-	0.076	-	-	0.003
$\theta$	-	$4^\circ$	$8^\circ$	-	$4^\circ$	$8^\circ$