



# Dual TTL-to-MECL Translator

**ELECTRICALLY TESTED PER:  
5962-8756001**

The 10H524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

2

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
BOUT	1	5	2	51 Ω to V <sub>TT</sub>
AOUT	2	6	3	51 Ω to V <sub>TT</sub>
$\overline{\text{BOUT}}$	3	7	4	51 Ω to V <sub>TT</sub>
$\overline{\text{AOUT}}$	4	8	5	51 Ω to V <sub>TT</sub>
A <sub>IN</sub>	5	9	7	V <sub>CC</sub>
Common Strobe	6	10	8	V <sub>CC</sub>
B <sub>IN</sub>	7	11	9	V <sub>CC</sub>
VEE	8	12	10	VEE
V <sub>CC</sub>	9	13	12	V <sub>CC</sub>
C <sub>IN</sub>	10	14	13	V <sub>CC</sub>
D <sub>IN</sub>	11	15	14	V <sub>CC</sub>
$\overline{\text{COUT}}$	12	16	15	51 Ω to V <sub>TT</sub>
$\overline{\text{DOUT}}$	13	1	17	51 Ω to V <sub>TT</sub>
D <sub>OUT</sub>	14	2	18	51 Ω to V <sub>TT</sub>
C <sub>OUT</sub>	15	3	19	51 Ω to V <sub>TT</sub>
GND	16	4	20	GND

**BURN - IN CONDITIONS:**

V<sub>TT</sub> = - 2.0 V MAX/ - 2.2 V MIN

VEE = - 5.7 V MAX/ - 5.2 V MIN

## Military 10H524

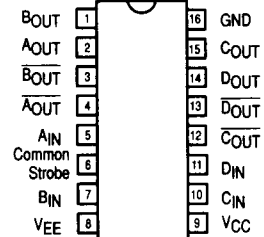


**AVAILABLE AS**

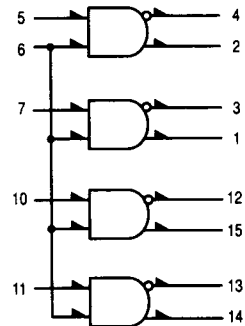
- 1) JAN: N/A
  - 2) SMD: 5962-8756001
  - 3) 883: 10H524/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

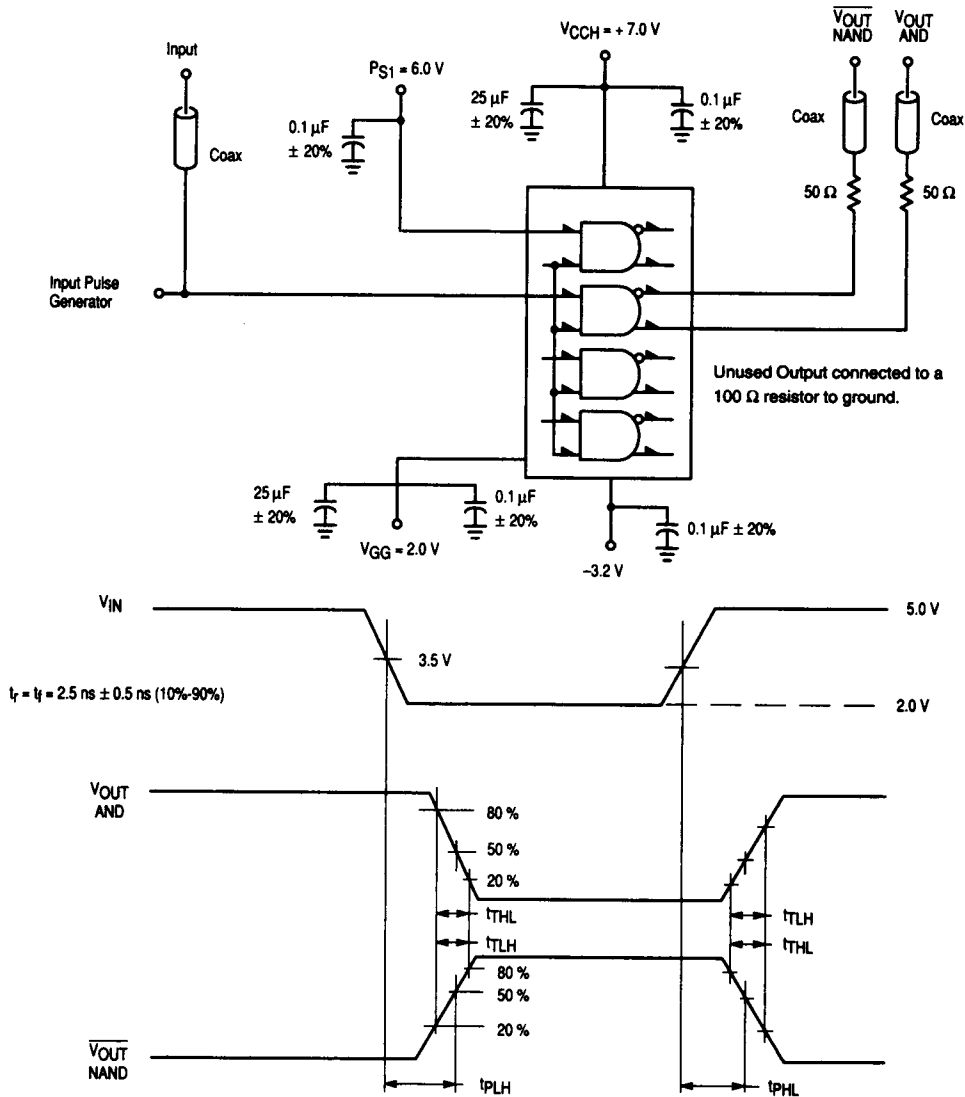
PACKAGE: CERDIP: E  
CERFLAT: F  
LCC: 2

The letter "M" appears before the slash on LCC.



**POSITIVE LOGIC DIAGRAM**





**NOTES**

1.  $50\ \Omega$  termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of  $50\ \Omega$  coaxial cable. Wire length should be  $< 164$  inch from  $TP_{IN}$  to input pin and  $TP_{OUT}$  to output pin.

**Figure 1. Switching Test Circuit and Waveforms**

# 10H524 QUIESCENT LIMIT TABLE\*

Test Temperature	Test Voltage Values (Volts)												
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>RH</sub>	V <sub>R</sub>	V <sub>F</sub>	PS1	VEEL	VEE1	VEE2	BVIN	VCC	VCCH	VGG
T <sub>A</sub> =25 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	-2.94	-5.46	-4.94	+5.5	+5.0	+7.0	+2.0
T <sub>A</sub> =125 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	-2.94	-5.46	-4.94	+5.5	+5.0	+7.0	+2.0
T <sub>A</sub> =55 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	-2.94	-5.46	-4.94	+5.5	+5.0	+7.0	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments I <sub>D1</sub> = - 10 mA, I <sub>D2</sub> = - 20 mA Output Load = 100 Ω to GND								
Functional Parameters:		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max										
V <sub>OH</sub>	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	V <sub>EE1</sub>	V <sub>EE2</sub>	GND	VCC	P. U. T.
V <sub>OL</sub>	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V				5, 7 10, 11	8		16	9	1-4 12-15
V <sub>OH1</sub>	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	5-7 10, 11	5-7 10, 11	5-7 10, 11	10, 11	8	8	16	9	1-4 12-15
V <sub>OL1</sub>	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	5-7 10, 11	5-7 10, 11	5-7 10, 11	7	8	8	16	9	1-4 12-15
IEE	Power Supply Current	-66		-72		-72		mA					8		16	9	8
IF1	Forward Current		-3.2		-3.2		-3.2	mA				5, 7 10, 11	8		16	9	5, 7 10, 11
IF2	Forward Current		-12.8		-12.8		-12.8	mA				5, 7 10, 11	8		16	9	6

### \* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

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Test Temperature	Test Voltage Values (Volts)											
	V <sub>H1</sub>	V <sub>I1</sub>	V <sub>RH</sub>	V <sub>R</sub>	V <sub>F</sub>	F <sub>S1</sub>	V <sub>EEL</sub>	V <sub>EE1</sub>	V <sub>EE2</sub>	B <sub>VIN</sub>	V <sub>CCH</sub>	V <sub>GG</sub>
T <sub>A</sub> =25 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	-2.94	-5.46	-4.94	+5.5	+7.0	+2.0
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		Subgroup 1	Subgroup 2	Subgroup 3	Subgroup 1	Subgroup 2	Subgroup 3		V <sub>F</sub>	V <sub>R</sub>	V <sub>RH</sub>	B <sub>VIN</sub>	I <sub>D1</sub>	I <sub>D2</sub>	V <sub>EE1</sub>	GND	V <sub>CC</sub>
V <sub>ID</sub>	Input Clamp Voltage	Min	Max	Min	Max	Min	Max	V				5, 7 10, 11	6	8	16	5, 7 10, 11	
I <sub>CC</sub>	Positive Power Supply Current Drain		25		25		25	mA					10				
I <sub>CCH</sub>	Positive Power Supply Current Drain		16		18		16	mA								5, 7 10, 11	9
I <sub>IN</sub>	Input Current		1.0		1.0		1.0	mA					6			5, 7 10, 11	9
I <sub>R1</sub>	Reverse Current		50		50		50	μA					6			5, 7 10, 11	9
I <sub>R2</sub>	Reverse Current		200		200		200	μA					6			5, 7 10, 11	9

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		Subgroup 9		Subgroup 10		Subgroup 11			VIN	VOUT	VCCH	VEEL	VGG	PS1	P.U.T
t <sub>r</sub>	Rise Time	0.45	2.0	0.5	2.5	0.4	1.8	ns	5	4	9	8	16	6	1 - 3, 12 - 15
t <sub>f</sub>	Fall Time	0.45	2.0	0.5	2.5	0.4	1.8	ns	5	4	9	8	16	6	1 - 3, 12 - 15
t <sub>pHL</sub>	Propagation Delay Pin 6	0.55	2.5	0.85	3.6	0.5	2.0	ns	10	12	9	8	16	6	1 - 4, 13 - 15
t <sub>pLH</sub>	Propagation Delay Pin 6	0.55	2.5	0.85	3.6	0.5	2.0	ns	10	12	9	8	16	6	1 - 4, 13 - 15
t <sub>pHL</sub>	Propagation Delay Pins 5, 7, 10, 11	0.55	2.4	0.85	3.5	0.55	2.1	ns	10	12	9	8	16	6	1 - 4, 13 - 15
t <sub>pLH</sub>	Propagation Delay Pins 5, 7, 10, 11	0.55	2.4	0.85	3.5	0.55	2.1	ns	10	12	9	8	16	6	1 - 4, 13 - 15

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