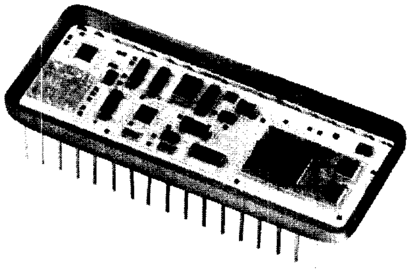
NATEL

HSRD1056

Improved 2nd Generation, Programmable Synchro/Resolver-to-Digital Converter Microprocessor Compatible 16-bit Hybrid

Features

- **1.3 Arc-minute Accuracy**
- ✓ **True Single Supply - 5 Volts Only** (prevents ground-loop problems)
- ✓ **50 mW Power Dissipation**
- **BIT Output** (Built-in Test)
- ✓ **Reference Synthesizer** (for improved dynamic accuracy)
- ✓ **No 180° False Lock-up**
- ✓ **Analog Velocity Output** (use as Tachometer)
- ✓ **Automatic Gain Control** (allows 2:1 signal variation)
- ✓ **Very High Tracking Rate** (7200°/second for high frequency option)
- **Synchro/Resolver Pin Programmable**
- **14-/16-bit Programmable Resolution**
- **8- and 16-Bit Microprocessor Compatible**
- **Hermetic 36-Pin DDIP Package**
- **MIL-STD-883 Processing Is Available**



ACTUAL SIZE

Applications

Avionics systems
Antenna monitoring
Servo systems
Coordinate conversion
Fire control systems
Axis rotation
Engine controllers
Industrial control systems
Simulation
Robotics
Machine tool control systems
Solar panel control systems

Description

The HSRD1056 is an advanced, Second Generation, improved version of the very popular Natel Model 1006 converter. Packaged in a 36-pin DDIP hybrid, it is pin compatible with the Model 1006 while offering the most advanced performance features ever available in Synchro/Resolver-to-Digital converters. The 1056, like the 1006, operates from a single 5 V-dc power supply and consumes only 10 mA of current. The low power dissipation of 50 mW not only makes the Natel 1056 run cool, but it puts less strain on the user's power supply, thereby improving system MTBF. The 1056 is fully compatible with 8- and 16-bit microprocessors and has a high frequency option with higher tracking speed and wider bandwidth. Additional superior features of the 1056 include Built-in Test, an anti-180° false lock-up circuit, a reference synthesizer, pin-programmable Synchro/Resolver and 14-/16-bit modes, automatic gain control, and a high-quality analog velocity output.

Using a high-accuracy differential signal conditioner for the resolver input and a resistive scott-tee for the synchro input, the converter provides common-mode rejection in excess of 70 dB. The input impedance remains constant and balanced independent of dc power to the converter, This feature prevents loading of the synchro and reference input lines when the converter is not powered. This technique also permits resistor programming for non-standard input voltages.

Model 1056 is a Type-II tracking converter with zero velocity lag error. An internal reference synthesizer permits improved dynamic accuracy by reducing the effects of "speed voltages" at high rotational speeds. The accuracy of the converter is maintained with signal-to-reference phase shifts of up to ±45 degrees. An anti-180° false lock-up circuit is used to assure that the converter does not get locked into an angle 180 degrees from the true angle when a step function of 180 degrees is applied. Transferring data from the 1056 is eased through the use of a transparent latch with three-state outputs configured as two independently enabled 8-bit bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory-mapped data interface and control with most popular 8-and 16-bit microprocessors and single-board computers.

A built-in-test (BIT) feature provides a logic "1" when the tracking error exceeds ±1°. Monitoring of converter dynamics is facilitated through the availability of analog signals corresponding to converter tracking velocity and instantaneous tracking error. The velocity output is a high-quality characterized analog signal that can be used instead of a mechanical tachometer in many servo and control systems. An AGC (automatic gain compensation) circuit is incorporated in the converter design, which allows signal voltage variations of ±30% without degradation of converter accuracy or dynamic response.

Theory of Operation

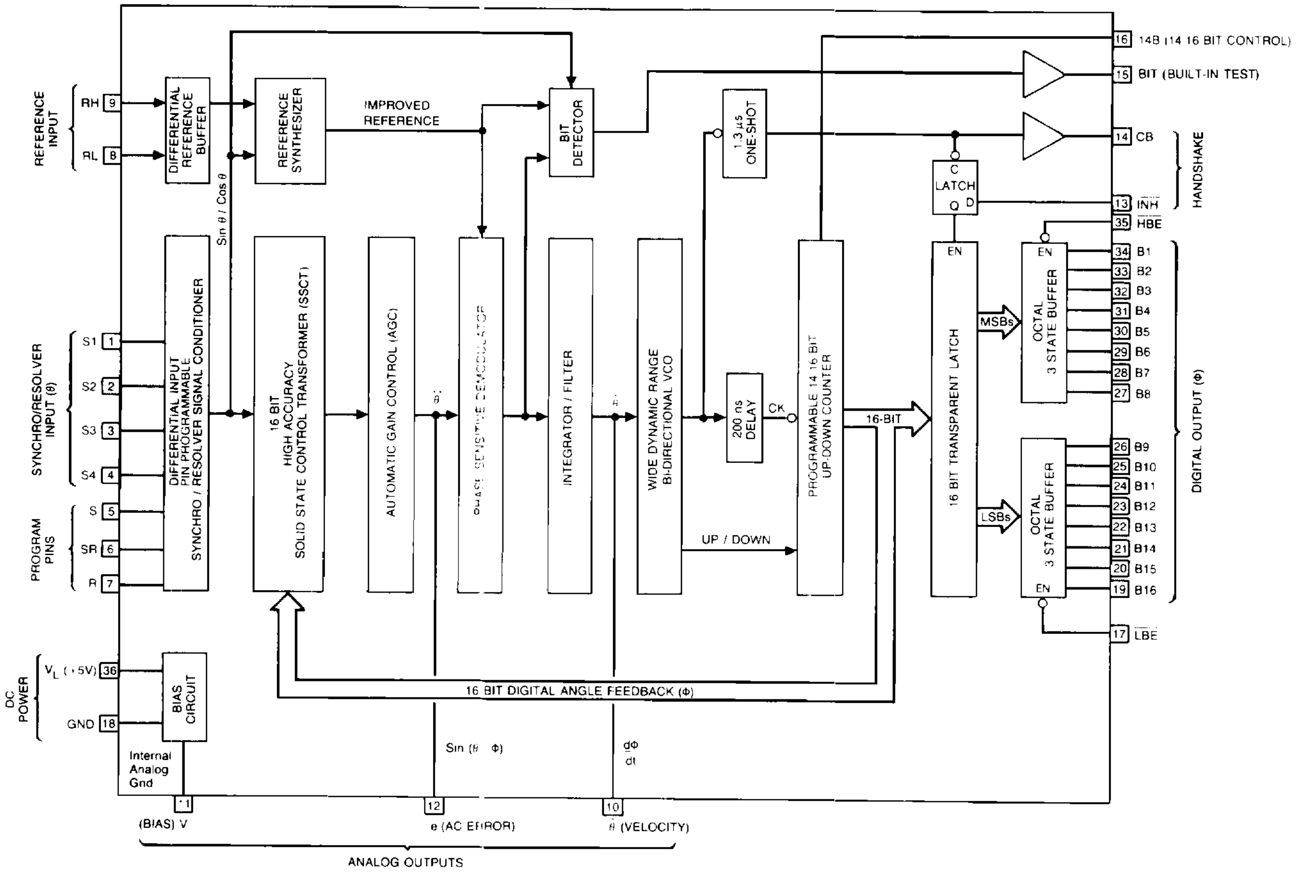


FIGURE 1 1056 Block Diagram

The operation of the Model 1056 is illustrated in the functional block diagram of Figure 1. The 1056 is a high-gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (ϕ) and the synchro (or resolver) input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage (e), according to the following trigonometric identity:

$$\text{"e"} = \sin(\theta-\phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

When the error voltage goes to null, sin (θ-ϕ) is zero, which makes the angle θ equal to the angle ϕ. Thus, the digital output represents the input shaft angle. Once synchronized, the output angle always tracks the input shaft angle without any lag error for constant velocity input.

The input "pin-programmable signal conditioner" accepts either a synchro or a resolver input and converts it into low level signals sin θ and cos θ, which are applied to the "solid state control transformer" (SSCT) discussed above. Output of the SSCT goes to "automatic gain control," which compensates for a 2:1 variation in synchro/resolver input levels. The output is applied to a "phase-sensitive demodulator" that is used to determine the polarity (phase) of the error signal "e" with respect to reference signal. Instead of using the external reference signal (RH, RL) as applied to the converter, Model 1056 generates an improved reference internally. The "reference synthesizer" obtains this improved reference from sin θ and cos θ signals and uses the external reference for coarse phase determination only. Use of the improved reference for demodulating allows the Model 1056 to better reject quadrature components in the error signal "e." The demodulated error signal is applied to an "integrator/filter" which, in addition to ripple and noise filtering, provides the first integration required for the Type II servo loop. The integrator/filter is also used for appropriate gain and phase compensation for loop stability (optmized for low over-shoot and fast settling time). The "wide dynamic range bi-directional VCO" performs a voltage-to-frequency conversion whose pulses or counts are accumulated in the "programmable 14/16 bit up-down counter." The up-down counter performs the second integration in the Type II loop. The input to the VCO inherently provides an analog indication of the digital output rate of change (velocity).

The "16-bit transparent latch" provides a means of holding the digital output steady during data transfer, while allowing the converter to continuously track the input angle. The "1.3 µs one shot" provides an output pulse (CB) for every LSB of output change. It is also used as a clock or gate for the inhibit $\overline{\text{INH}}$ "latch" to prevent attempted "data read" commands during an up-down counter output transition. The "200 ns delay" is used to prevent a race condition between the CB (Converter Busy) output and $\overline{\text{INH}}$ input.

The "3-state buffer" output is split into two 8-bit bytes to allow interfacing on both 8- and 16-bit data bus systems. The "BIT detector" provides a fault indication as well as help in eliminating false 180 degree digital output readings. The following pages provide more detailed technical discussions for some of these functions.

Reference Synthesizer

To maintain the highest accuracy under both static and dynamic conditions, the 1056 utilizes a "reference synthesizer" to correct for a phase difference between the signal and reference inputs of up to ±45°.

Conventional tracking synchro (resolver)-to-digital converters use a phase-sensitive demodulator to detect the phase and amplitude of the error voltage, sin $(\theta\text{-}\phi)$. One of the functions of the demodulator is to reject quadrature components in the error signal (e). A phase-sensitive demodulator rejects any quadrature signal (signal 90° out of phase) only if the synchro input and its reference are exactly in phase. Zero degree phase shift between reference and signal inputs is not practical in most applications using synchro (resolver)-to-digital converters. Quadrature signal voltage can result from any of the following:

— dynamic synchro/resolver "speed voltages," — a quadrature signal that is proportional to the shaft rotational speed

— synchro/resolver "null voltages"

— capacitive coupling between synchro lines

— differential phase shift in synchro/resolver lines

This quadrature voltage will cause angular error as a variable offset if there is a phase difference between input signals and reference. For example for a 60-Hz synchro with a 5° phase shift rotating at 2 rps (720°/sec), the dynamic error due to speed voltage would be 0.17 degree or 10 arc-minutes!

Natel's model 1056 greatly reduces the effects of this error by creating a synthetic reference. The sine and cosine voltages from the signal conditioner are combined to obtain an in-phase internal reference. Together with the external reference voltage (to determine phase) this improved reference is used for demodulating the error voltage.

Built-in Test (BIT)

A BIT signal (pin 15) provides an over-velocity or fault indication output signal. The error voltage of the converter is monitored continuously, and when the tracking error exceeds approximately 1 degree (over-velocity or failure), a logic "1" signal is generated to indicate invalid data. Under normal operation the BIT output is at logic "0." Possible conditions that will cause the BIT output to show fault indication are:

- Power-turn-on — BIT output will return to logic "0" when the converter synchronizes to correct input angle ±1°
- Step-input — Instantaneous input changes greater than ±1° until the converter synchronizes
- Over velocity condition
- Excessive shaft angle modulation
- Reference voltage disconnected
- Loss of signal — all signal lines are disconnected
- Converter malfunction — any converter failure which prevents synchronization to the input angle

Note that BIT output has ≥50% duty cycle logic "1" when reference lines and/or signal lines are disconnected. The cycle frequency is synchronous with the carrier frequency when either the signal or reference (but not both) is missing. When both signal and reference lines are disconnected, the cycle frequency is ≥2 Hz.

From above discussion it is apparent that the BIT output not only serves to self-test the converter but also provides an indication of the operation of the synchro transmission system as well.

No 180° False Lock-up

An additional function of the "BIT Detector" (built-in-test detector), incorporated into the Model 1056 is to eliminate "false 180° digital output readings," during instantaneous 180° input step changes. "180° false lock-up" can occur in most synchro-to-digital converters whenever the synchro (resolver) input angle is "electronically switched" or stepped from one angle to another by 180 degrees. This occurrence, is most common in applications where the input is being supplied by a digital-to-synchro converter and the MSB (180° bit) is turned "ON" or "OFF."

The reason this occurs in most synchro-to-digital converters is because the "solid-state control transformer" (SSCT) used in the conversion process can produce two (2) "nulls" at the error output "e" for a given digital feedback angle. This is easily understood by trignometric indentity

$$\begin{aligned} \sin[(\theta-\phi)+180] &= -\sin(\theta-\phi) \\ &= \sin(\theta-\phi) \\ &\text{when} \\ &(\theta-\phi) = \text{zero} \end{aligned}$$

Since error output "e" is a sine function (see theory of operation) this creates a possibility of a second null and the converter locking-up 180 degrees away from the true angle.

Natel's Model 1056 gets around this problem by continuously monitoring sin θ and cos θ signals and comparing the phase relationship with the digital output angle and reference input (RH, RL). When a 180 degree input step is applied, the internal BIT-detect circuit is activated, which forces an error in the converter loop to move the digital output angle to the correct reading. As soon as the digital output is properly phased with the shaft angle input, this "intentional error" is removed from the converter loop.

True Single-Supply 5 V-dc Operation

One of the most outstanding features of the Model 1056 is the single +5 V-dc power supply requirement. This feature simultaneously eliminates both unwanted "ground loop" problems and allows the elimination of ±15 V-dc power supplies in all-digital systems.

Without the single supply operation, systems that use separate analog and digital grounds for ±15 V-dc and +5 V-dc power, as many systems do, would be faced with potential ground loop problems. The result is usually excess noise on either the analog or digital supplies, which limits the effectiveness of single-point grounding schemes. These ground loops would be present with a converter that used both ±15 and +5V-dc power because the analog (±15 V-dc) and digital (+5 V-dc) power supplies are referenced to different grounds while most multiple supply converters have only a single internal ground. The 1056 takes the agony out of these difficult systems problems by operating entirely within the digital power and ground rails of your system.

All internal circuitry is designed to operate with power supply voltage of as low as 4.5 V-dc. This is made possible by using high signal-to-noise ratio amplifiers and a unique design approach incorporated into a custom LSI chip. No performance specification is sacrificed due to the single 5 V-dc operation. In fact, the 1056 offers the most advanced design features ever available in any Synchro/Resolver-to-Digital converter.

Operating with a 5 V-dc supply, the converter typically requires only 10 mA of current. This low power operation results in a typical junction-to-ambient (no heat sink) temperature rise of only 3° C!

Automatic Gain Compensation

An AGC circuit incorporated within the HSRD1056 allows the converter to maintain its high accuracy over a wider range (2 to 1) of signal amplitudes than any other Synchro-to-Digital converter.

In theory, the accuracy of an S/D or R/D converter is not affected by signal amplitude variations because the conversion process is ratiometric and therefore not dependent on the magnitude of the input. In practice, however, the necessity of providing hysteresis to prevent hunting or jitter in the least significant bit (LSB), introduces a controlled inaccuracy in the converter. This hysteresis is typically greater than 0.5 LSB. Ordinary converters derive this hysteresis as a fixed threshold at nominal input signal amplitude. Thus the conversion accuracy would vary directly with the Synchro input amplitude . . . becoming degraded for the lower amplitudes and creating excessive jitter at higher amplitudes. In this instance, the converter dynamics and settling times would also vary with the Synchro input amplitude.

The HSRD1056 monitors the input signals continuously and modifies the gain of the error voltage as a function of input signal amplitude to keep the overall converter loop gain constant.

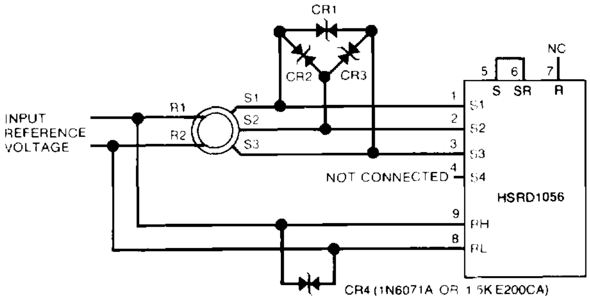
Resolution Programming

To allow speed vs. resolution tradeoffs in system design, the HSRD1056 can be programmed for either 14-bit or 16-bit resolution. This programming function is accomplished by control 14B (pin 16). A logic "1" or an open circuit at 14B makes the converter operate in the 14-bit mode (data bits 15 and 16 are forced to a logic "0"). A logic "0" or ground at pin 14B allows the converter to operate in the 16-bit mode. The loop gain of the converter is automatically compensated in both 14-bit and 16-bit modes. Although resolution is reduced in the 14-bit mode, the tracking speed and the acceleration constant are increased by a factor of 4.

Connecting the BIT output (pin 15) to 14B (pin 16) provides a method for reducing settling time while maintaining a 16-bit resolution during tracking. At power turn-on or for a large step input, the BIT output would be at a logic "1," forcing the converter to operate in the 14-bit mode (×4 tracking rate). As soon as the output is synchronized to within ±1° of the input angle, the converter automatically reverts to the 16-bit mode. This technique can be used in applications where input speeds are variable and the converter must not lose synchronization during transient high-speed rotation.

Synchro/Resolver Connections and Phasing

V_{L-L} INPUT	CR1-CR3
11.8 V-rms	1N6049A OR 1.5KE27CA
90 V-rms	1N6070A OR 1.5KE200CA



$$E_{S3-S1} = V_{max} \sin\theta$$
$$E_{S2-S3} = V_{max} \sin(\theta + 120^\circ)$$
$$E_{S1-S2} = V_{max} \sin(\theta + 240^\circ)$$

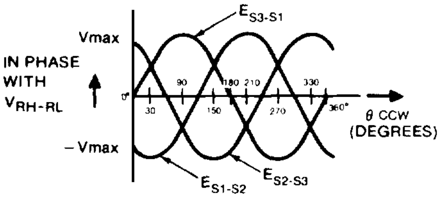
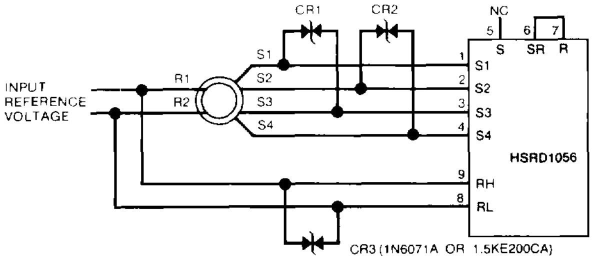


FIGURE 2 Synchro Inputs

V_{L-L} INPUT	CR1, CR2
11.8 V-rms	1N6049A OR 1.5KE27CA
26 V-rms	1N6057A OR 1.5KE56CA
90 V-rms	1N6070A OR 1.5KE200CA



$$E_{S3-S1} = V_{max} \sin\theta$$
$$E_{S2-S4} = V_{max} \cos\theta$$

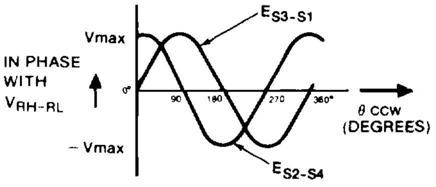


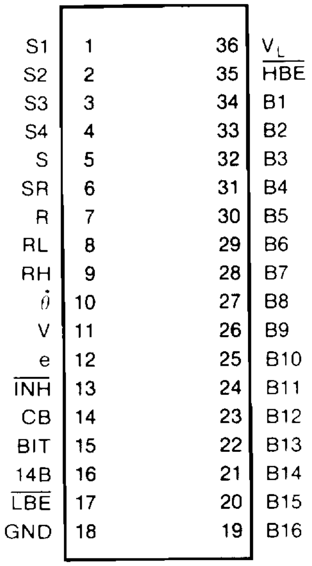
FIGURE 3 Resolver Inputs

The connections for synchro and resolver inputs are shown in figure 2 and figure 3. The input signal conditioner of the Model 1056 converter can be pin-programmed to accept either synchro or resolver inputs. In addition it uses differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format (sin θ and cos θ).

Both signal and reference inputs are true differential inputs and use precision thin film resistors for signal attenuation. If input voltages exceed the absolute maximum ratings, the thin-film resistors may be destroyed. To prevent this from happening, it is recommended that transient voltage suppressors be installed on both signal and reference lines. Synchros and resolvers are highly inductive and can generate or couple transients many times greater than their normal signal voltages and can easily exceed the absolute maximum ratings. This situation is particularly likely to occur in cases where the excitation or source voltage for the synchro (resolver) is switched on or off. Transients can also occur by other equipment being turned on or off. Figures 2 and 3 show recommended methods of connecting synchro and resolver inputs. Transient voltage suppressors given in the tables (or equivalent) must be used to assure input protection.

Pin Designations

V_L	Power Supply Voltage Logic Voltage 5 V-dc ±10%
GND	Power Supply Ground Digital Ground
B1 - B16	Parallel Output Data Bits - B1 is MSB = 180 degrees B16 is LSB = 0.0055 degree
S1, S2, S3, S4	Input Analog Signals Leave S4 unconnected for synchro-input (or connect to "V" pin 11)
S, SR, R	Synchro/Resolver Programming-pins Synchro Input - connect S to SR, leave R unconnected Resolver Input - connect R to SR, leave S unconnected
RH, RL	Reference Voltage Input
$\dot{\theta}$	Velocity Output - dc analog voltage proportional to rotational speed of the input shaft angle. Output is referenced to bias voltage (V)
V	Bias Voltage - Internally generated reference voltage serves as reference ground for all analog outputs.
e	Error Voltage - ac analog voltage proportional to instantaneous tracking error of the converter. Output is referenced to bias-voltage (V)
$\overline{\text{INH}}$	Inhibit Function - A logic "low" freezes the digital angular output. Internal loop keeps tracking the analog input. All other outputs keep following the input. For continuous operation this pin may be left unconnected. Internal active pull-up will apply V_L to the pin.
CB	Converter Busy - A 1.3 μs pulse which occurs during updating of the holding register. Output data can be transferred at the trailing edge of the CB pulse. When converter output is not changing CB is at logic "low."



S1	1	36	V_L
S2	2	35	$\overline{\text{HBE}}$
S3	3	34	B1
S4	4	33	B2
S	5	32	B3
SR	6	31	B4
R	7	30	B5
RL	8	29	B6
RH	9	28	B7
$\dot{\theta}$	10	27	B8
V	11	26	B9
e	12	25	B10
$\overline{\text{INH}}$	13	24	B11
CB	14	23	B12
BIT	15	22	B13
14B	16	21	B14
$\overline{\text{LBE}}$	17	20	B15
GND	18	19	B16

FIGURE 4 HSRD1056 Pin Assignments

BIT	Built-in Test - A Logic "high" output indicates that output is not tracking the input analog signal within ±1°.
14B	Output Resolution Control - Allows 4 times tracking speed in 14 bit-mode. Logic "low" or ground = 16-bit output Logic "high" or unconnected = 14-bit output (Bits 15 and 16 will be at Logic "low")
$\overline{\text{HBE}}$	High Byte Enable - Data bits B1 through B8 are enabled (low-impedance state of 3-state output) when $\overline{\text{HBE}}$ is set to a logic "low." When $\overline{\text{HBE}}$ is set to a logic "high," the data bits B1 through B8 are disabled (high-impedance state of 3-state output)
$\overline{\text{LBE}}$	Low Byte Enable - Data bits B9 through B16 are enabled when $\overline{\text{LBE}}$ is set to a logic "low." When $\overline{\text{LBE}}$ is set to a logic "high," the data bits B9 through B16 are disabled.
Note:	For continuous 16-bit parallel output $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ may be left open. Internal active pulldown to ground will apply logic "low" to these pins thus enabling all data bits B1 through B16.

Absolute Maximum Ratings

Signal Inputs	Twice Normal Voltage
Reference Inputs	200 V-rms
Supply Voltage (V_L)	+6.5 V-dc
Digital Inputs	−0.3 V-dc to V_L
Storage Temperature	−65° C to +135° C

When installing or removing the converter from printed circuit boards or sockets, it is recommended that the power supply and input signals be turned off. Decoupling capacitors are recommended on the power supply V_L. A 1-μF tantalum capacitor in parallel with 0.01-μF ceramic capacitor should be mounted as close to the supply pin (36) as possible.

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Output Resolution			
	16-bits (0.33 arc-minutes) 14-bits (1.32 arc-minutes)	For pin-16 (14B) = logic "0" For pin-16 (14B) = logic "1" or open circuit	Note 2
Accuracy			
	± 5.2 arc-minutes (Option S) ± 2.6 arc-minutes (Option H) ± 1.3 arc-minutes (Option V)	Accuracy applies over the full operating temperature range, ±10% frequency variation and includes hysteresis	Note 1
Reference Input			
Voltage	20 to 130 V-rms		Note 2
Frequency	700 to 3000 Hz (Option 8) 360 to 1000 Hz (Option 4) 47 to 1000 Hz (Option 6)	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Input Impedance (minimum)	250 K Ω Single Ended 500 K Ω Differential		Note 2
Common-Mode Range	±250 V peak maximum	dc plus recurrent ac peak	Note 3
Synchro/Resolver Inputs			
Input Voltages (line-to-line)	11.8 V-rms (Option 1) 26 V-rms (Option 2) 90 V-rms (Option 9)	Accuracy of the converter is maintained with ±30% variation in signal voltages	Note 1
Input Impedance (minimum)	30 K Ω (60 K Ω) minimum 75 K Ω (150 K Ω) minimum 250 K Ω (500 K Ω) minimum	Line-to-GND (differential), 11.8 V-rms L-L Models Line-to-GND (differential), 26 V-rms L-L Models Line-to-GND (differential), 90 V-rms L-L Models	Note 2
Impedance Unbalance	0.2% maximum	For all Models	Note 3
Common-Mode Range	± 25 V peak ± 55 V peak ±180 V peak	11.8 V-rms Models 26 V-rms Models 90 V-rms Models	Note 3
Common-Mode Rejection	70 dB minimum	dc to 1000 Hz	Note 3
Harmonic Distortion	10% maximum	Without degradation in accuracy specification	Note 3
Reference Synthesizer			
Phase-shift allowed between Input signals and Input reference	±45° guaranteed ±65° typical	Without any degradation of converter accuracy	Note 2
Digital Inputs		CMOS transient protected	
$\overline{\text{HBE}}$	Logic "1" Logic "0"	8 MSBs are in the high impedance state of 3-state output 8 MSBs are enabled	Note 1
$\overline{\text{LBE}}$	Logic "1" Logic "0"	8 LSBs are in the high-impedance state of 3-state output 8 LSBs are enabled	Note 1
$\overline{\text{INH}}$	Logic "1" Logic "0"	Digital output follows analog input signals Output data latched in holding register (does not interrupt converter tracking loop)	Note 1
14B	Logic "1" Logic "0"	14-bit resolution 16-bit resolution	Note 1
Voltage Levels Logic "0" Logic "1"	-0.3 V-dc to 0.8 V-dc 2.4 V-dc to 5 V-dc	For V_L = 5 V-dc	Note 2
Input Currents $\overline{\text{HBE}}$, $\overline{\text{LBE}}$	15 µA typical (30 µA max) "active" pull down to ground (GND)	When not used, may be left unconnected	Note 3
$\overline{\text{INH}}$, 14B	-15 µA typical (-30 µA max) "active" pull up to the power supply (V_L)	When not used, may be left unconnected	Note 3

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Outputs		CMOS Outputs	
Data Bits (B1-B16)	Natural Binary Angle	Positive logic	
CB	Logic "0" Logic "1" (Nominal 1.3 µs pulse for every LSB change)	Output angle not changing Output angle changing (leading edge initiates output change - see figure 5)	Note 1
BIT	Logic "0" Logic "1"	Digital output tracking analog input Fault indication (tracking error >±1° typical)	Note 1
Drive Capability		For V_L = 4.5 V-dc, over full temp range	
Data Bits (B1-B16),CB,BIT	1 Standard TTL minimum		Note 3
Logic "0" sink current Logic "1" source current	1.6 mA (min) @ 0.40 V-dc -1.6 mA (min) @ 3.0 V-dc	See Figure 10 for typical drive curves	Note 3
HI-Z Output Leakage Data Bits (B1-B16)	±10 µA maximum	Output capacitance = approx. 5 pF	Note 3
Analog Outputs	**Typical, unless specified**		
V (Bias Voltage)	1/2 (V_L-0.7) ±10%	2.15 V-dc ±10% for 5 V-dc supply	Note 3
e (unfiltered ac error)	750 mV-rms typical for 1° error	ac voltage referenced to V	Note 3
Drive Capability	± 1 mA minimum	All analog outputs	Note 3
$\dot{\theta}$ Velocity Output	**Typical, unless specified**	**dc voltage referenced to V (bias)**	
Polarity	Negative for increasing angle		Note 3
Scale Factor (Gain) @ 25° C	0.209 mV/deg/sec typical 0.835 mV/deg/sec typical 0.305 mV/deg/sec typical 1.22 mV/deg/sec typical 1.53 mV/deg/sec typical 6.11 mV/deg/sec typical	800 Hz Models/14-bit mode 800 Hz Models/16-bit mode 400 Hz Models/14-bit mode 400 Hz Models/16-bit mode 60 Hz Models/14-bit mode 60 Hz Models/16-bit mode	Note 2
Temperature Coefficient	±500 PPM/° C typical		Note 3
Power Supply Dependence	-1% per percent maximum		
Full Scale Output @ 25° C	1.5 V-dc @ 7200°/sec typical 1.5 V-dc @ 1800°/sec typical 1.1 V-dc @ 3600°/sec typical 1.1 V-dc @ 900°/sec typical 1.1 V-dc @ 720°/sec typical 1.1 V-dc @ 180°/sec typical	800 Hz Models/14-bit mode 800 Hz Models/16-bit mode 400 Hz Models/14-bit mode 400 Hz Models/16-bit mode 60 Hz Models/14-bit mode 60 Hz Models/16-bit mode	Note 2
Linearity @ 25° C	±5% of full scale maximum ±2% of full scale maximum ±1% of full scale maximum	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Temperature Coefficient	±200 PPM/° C typical		Note 3
Power Supply Dependence	0.1% per percent typical		
Output Noise Static Input	3 mV-rms typical 3 mV-rms typical 3 mV-rms typical	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Input changing at a constant maximum tracking rate	15 mV-rms typical 15 mV-rms typical 30 mV-rms typical	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Output Offset @ 25° C	± 5 mV-dc typical ±20 mV-dc maximum	All Models	Note 2
Temperature Coefficient	±30 µV/° C typical		Note 3
Power Supply Dependence	±20 µV per percent typical		
ΔGain vs. Polarity	10% maximum	All Models	Note 2
Temperature Coefficient	±200 PPM/° C typical		Note 3
Power Supply Dependence	0.1% per percent typical		
Automatic Gain Control			
Range	2 to 1	Performance of the converter is maintained with ±30% variation in signal voltages	Note 3

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Dynamic Characteristics	Typical, unless specified	Specified for power supply = +5 V-dc	
Velocity Constant (K_V)	∞	Type II servo loop	Note 3
Tracking Rate (minimum)	±7200 (1800) °/sec ±3600 (900) °/sec ± 720 (180) °/sec	For 800 Hz Models/14- (16-) bit mode For 400 Hz Models/14- (16-) bit mode For 60 Hz Models/14- (16-) bit mode	Note 1
Maximum Acceleration (typical)	1,600,000 (400,000) °/sec^2 400,000 (100,000) °/sec^2 16,000 (4,000) °/sec^2	For 800 Hz Models/14- (16-) bit mode For 400 Hz Models/14- (16-) bit mode For 60 Hz Models/14- (16-) bit mode	Note 3
Acceleration Constant (nominal)	768,000 (192,000) /sec^2 192,000 (48,000) /sec^2 7,680 (1,920) /sec^2	For 800 Hz Models/14- (16-) bit mode For 400 Hz Models/14- (16-) bit mode For 60 Hz Models/14- (16-) bit mode	Note 3
Acceleration for 1 LSB error (LSB=0.0055°/16-bit mode) (LSB=0.022° /14-bit mode)	16,875 (1,055) °/sec^2 4,219 (264) °/sec^2 169 (11) °/sec^2	For 800 Hz Models/14- (16-) bit mode For 400 Hz Models/14- (16-) bit mode For 60 Hz Models/14- (16-) bit mode	Note 3
Settling time to 1 LSB (for 179° step change)	50 (150) ms maximum 100 (300) ms " 450 (1350) ms "	For 800 Hz Models/14- (16-) bit mode For 400 Hz Models/14- (16-) bit mode For 60 Hz Models/14- (16-) bit mode	Note 2
Settling time to 1 LSB (small signal step < 1.4°)	8 (25) ms maximum 16 (50) ms " 100 (250) ms "	For 800 Hz Models/14- (16-) bit mode For 400 Hz Models/14- (16-) bit mode For 60 Hz Models/14- (16-) bit mode	Note 2
Converter Bandwidth	400 (200) Hz typical 200 (100) Hz " 40 (20) Hz "	For 800 Hz Models/14- (16-) bit mode For 400 Hz Models/14- (16-) bit mode For 60 Hz Models/14- (16-) bit mode	Note 3
Power Supply			
Voltage	5 V-dc ±10%	Without degradation in accuracy specification	Note 3
Current	30 mA typical, 45 mA maximum 10 mA typical, 20 mA maximum	800 Hz Models 400, 60 Hz Models	Note 1
Thermal Characteristics			
Junction Temperature Rise Above Case	1° C typical, 2° C maximum	For component with highest temperature rise	Note 3
Case Temperature Rise Above Ambient	2° C typical, 4° C maximum 8° C max. (800 Hz Models)	Without any heat sink	Note 3
Power Dissipation	50 mW typical, 100 mW max. 225 mW max. (800 Hz Models)	For V_L = 5 V-dc	Note 3
Physical Characteristics			
Type	36-pin Hermetic Double Dip		
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	3 Standoffs are added to the package to insulate it from the printed circuit board traces (Standoffs included in 0.21 inch height dimension)	Note 3
Weight	0.6 oz (17 g) maximum		Note 3

NOTE 1. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

NOTE 3. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

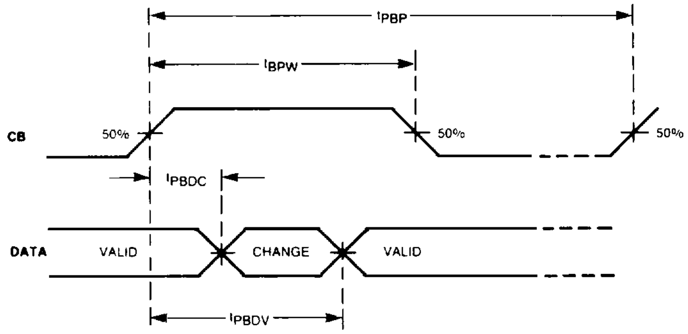
If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

Digital I/O Characteristics and Timing

R_L = 200 K Ω Input t_r t_f = 20 ns V_L = 5 V-dc C_L = 50 pF

(Specifications apply over full operating temperature range)

CHARACTERISTIC	LIMITS			UNITS	FIGURE
	MIN	TYP	MAX		
BUSY PULSE WIDTH (t_{BPW})	0.8	1.3	2.0	μs	5
BUSY PERIOD (t_{PBP})	2.0	NOTE 1	∞	μs	5
BUSY TO DATA CHANGE (t_{PBDC})	100	500	—	ns	5
BUSY TO DATA VALID (t_{PBDV})	—	600	800	ns	5
INHIBIT TO DATA STABLE (t_{PIDS})	0	—	1.0	μs	6,7
INHIBIT TO DATA UP-DATE (t_{PIDU})	100	—	—	ns	6,7
INHIBIT UPDATE PULSE WIDTH(t_{IPW})	2.0	—	—	μs	7
HIGH Z TO LOW Z (t_{PHZL})	30	150	250	ns	8
LOW Z TO HIGH Z (t_{PLZH})	30	100	200	ns	8
TRANSITION HIGH TO LOW (t_{THL}) 90%-10%	---	45	75	ns	9
TRANSITION LOW TO HIGH (t_{LHT}) TTL 10%-50% (t_{TLH}) CMOS 10%-90%	 --- ---	 60 120	 100 200	 ns ns	9



NOTE 1: **Busy Period (t_{PBP})** $= \dfrac{K \cdot 10^6}{2^N \cdot R}$ (μs)

For Reference:

Busy Frequency $= \dfrac{2^N \cdot R}{K}$ (Hz)

Rate (R) $= \dfrac{K \cdot \text{Busy Frequency}}{2^N}$

Where,

N = Converter Resolution (14 or 16)

K = 360 (For Degrees) or
 = 2π (For Radians)
 and

R = Rate (Degrees / Second) or
 = Rate (Radians / Second)

FIGURE 5 Converter Busy and Data Timing

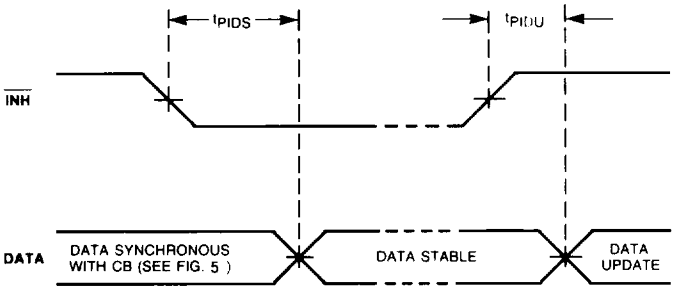


FIGURE 6 Inhibiting Output Data Update

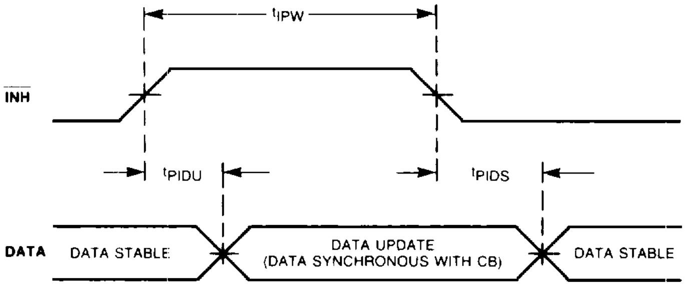


FIGURE 7 Enabling Output Data Update

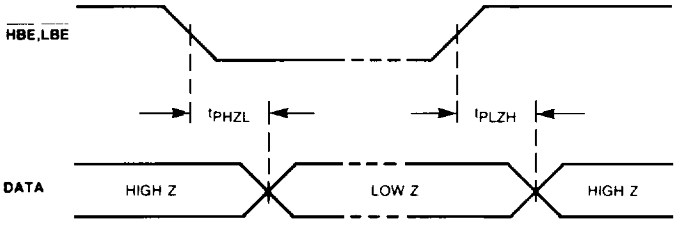


FIGURE 8 3-State Output Timing

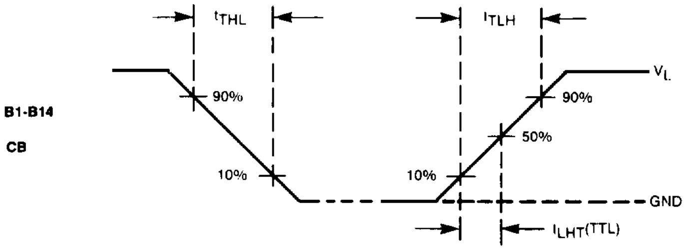


FIGURE 9 Transition Times

SINK

SOURCE

FIGURE 10 Output Drive Current (Typical @ V_L = 5V-dc, Ta = 25°C)

Data Transfer

Due to the nature of the Type II servo conversion mechanism incorporated in the 1056, the output data angle always tracks the synchro (resolver) input shaft angle within the converter's rated maximum tracking rate (angular velocity) and bandwidth. Theoretically, for every 0.0055 degree of input angle change (16-bit model) there will be a corresponding data output change of one LSB. To prevent reading data during an output change or transition, the following methods of data transfer can be used:

1) Synchronous transfer with shaft angle change.

   Use CB (Converter Busy) pulse to clock data into an external register. Use the falling edge of CB as an edge-triggered clock. (Rising edge of CB could be used but data would have an additional error of ±1 LSB.) Data changes within 800 ns after the rising edge of the CB pulse.

2) Asynchronous transfer with shaft angle change (using CB).

   Monitor the CB (Converter Busy) during a data transfer attempt. If CB is at logic "1," (the data will be void) . . . try another data transfer attempt. If CB is at logic "0" the data will be good. Note that the longest CB pulsewidth and therefore the longest wait period is 2 μsec. The CB pulse can essentially be used to gate an external data clock enable since the converter updates within the CB logic "1" duration (2 μs maximum).

3) Asynchronous transfer with shaft angle change (using $\overline{\text{INH}}$).

   The simplest method of data transfer (which is completely independent of input shaft angle change) is to use the inhibit ($\overline{\text{INH}}$) function to hold or freeze the current data output angle. Set the $\overline{\text{INH}}$ input to logic "0". . . wait a minimum of 1 μs . . . transfer the data . . . return $\overline{\text{INH}}$ to logic "1" for a minimum of 2 μs. This method of asynchronous data transfer from the 1056 is shown in Figure 11. Control functions $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ have internal pull down circuitry, permitting these pins to be left open (unconnected).

It should be noted that the $\overline{\text{INH}}$ control does not affect the conversion process . . . it only affects the transparent output latch. If the synchro (resolver) angle input changes while an inhibit is applied ($\overline{\text{INH}}$ = "0"), the internal data angle (up-down counter output) will still track the input. Fresh output data (B1-B16) will be available within 2 μs after the $\overline{\text{INH}}$ input returns to logic "1" (un-inhibit), regardless of the previous $\overline{\text{INH}}$ logic "0" duration.

Note: The CB output (Converter Busy) will always produce a pulse for every LSB of output angle change, regardless the state of the $\overline{\text{INH}}$ (inhibit) input.

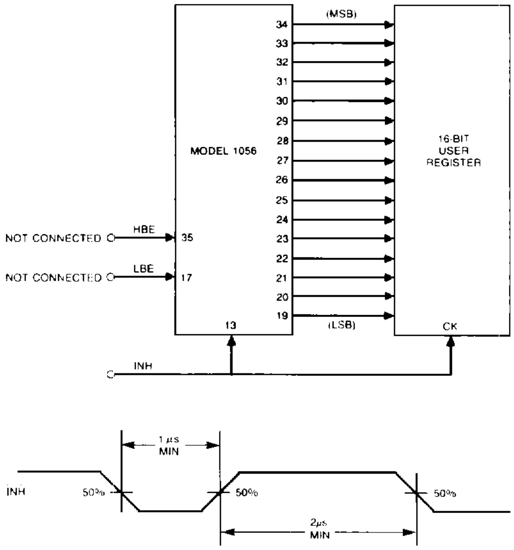


FIGURE 11 Asynchronous Data Transfer

Single-Byte Data Transfer on 16-Bit Data Bus

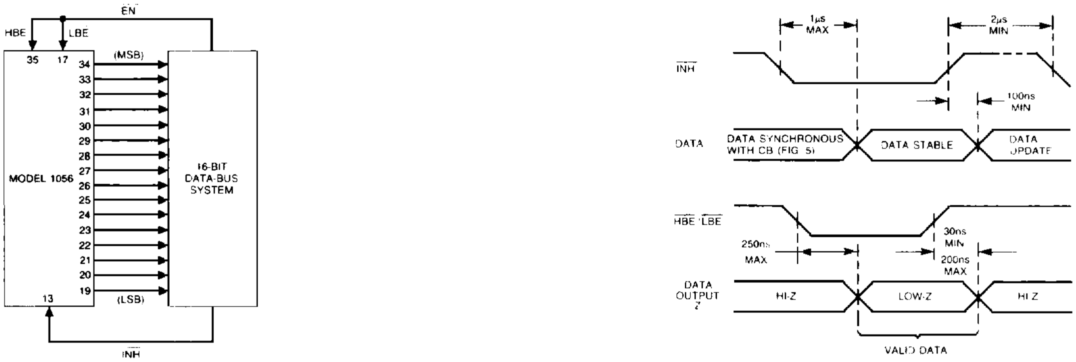


FIGURE 12 Digital Connections and Timing for Single-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from the Model 1056 to a 16-bit 3-state data-bus system is shown in Figure 12. A typical sequence of events would be as follows:

1) Apply the $\overline{\text{INH}}$ input for a minimum of 1 μs before transferring valid data.

2) Set $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ to logic "0" (3-state enables) for a minimum of 250 ns before transferring valid data.

   Note: The last device on the data-bus should be set to high impedance state no later than 30 ns after $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ are set to logic "0."

3) Transfer Data

4) Return $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ to logic "1" at least 200 ns before the next device is put on the data bus.

   Note: The data output remains in the low-Z state for a minimum of 30 ns after the rising edge of $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$, therefore data can be transferred at the rising edge of $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ . . . provided the data hold requirement of the external device is less than 30 ns.

5) Return $\overline{\text{INH}}$ to logic "1" no earlier than 100 ns before valid data is transferred. The $\overline{\text{INH}}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 2 μs to allow update of fresh accurate output data.

   Note: $\overline{\text{INH}}$ (inhibit) input function is independent from $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ (3-state enable) inputs.

Two-Byte Data Transfer on 8-Bit Data Bus

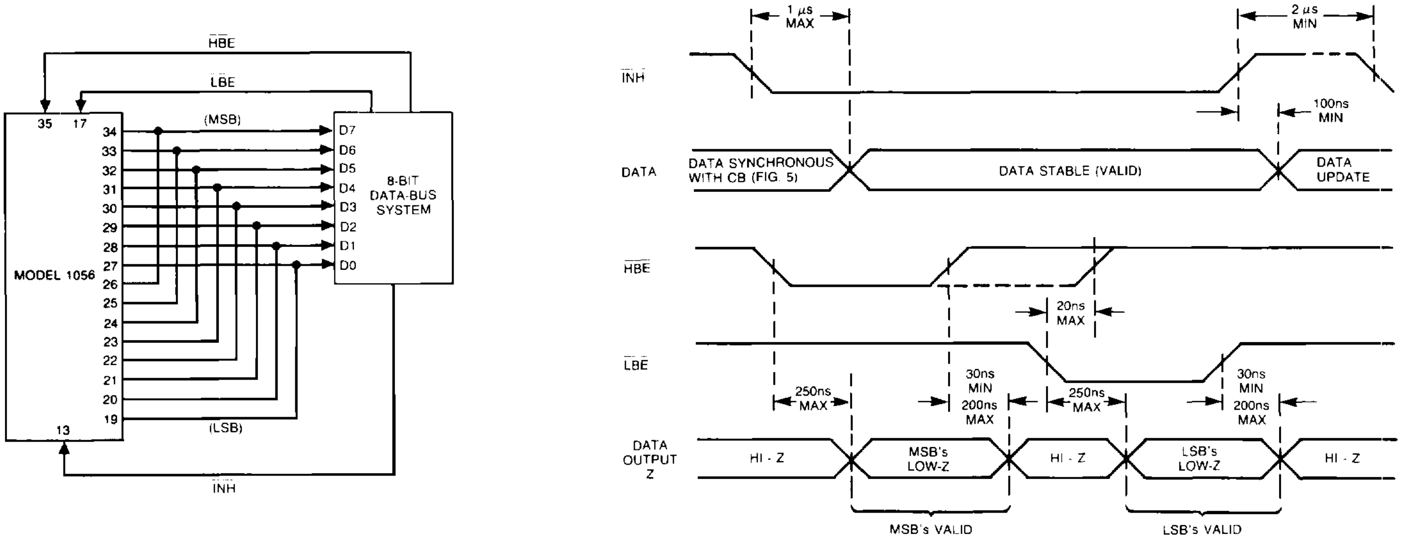


FIGURE 13 Digital Connections and Timing for Two-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from Model 1056 to an 8-bit 3-state data-bus system is shown in Figure13. A typical sequence of events would be as follows:

1) Apply the $\overline{\text{INH}}$ input for a minimum of 1 µs before transferring valid data.

2) Set $\overline{\text{HBE}}$ to logic "0" (high-byte-enable) for a minimum of 250 ns before transferring valid data (MSBs).

   Note: The last device on the data-bus should be set to high impedance state no later than 30 ns after $\overline{\text{HBE}}$ is set to logic "0."

3) Transfer MSBs.

4) Return $\overline{\text{HBE}}$ to logic "1" no later than 20 ns after $\overline{\text{LBE}}$ is set to logic "0."

5) Set $\overline{\text{LBE}}$ to logic "0" (low-byte-enable) for a minimum of 250 ns before transferring valid data (LSBs), but not more than 20 ns before $\overline{\text{HBE}}$ has returned to logic "1" (rising edge).

6) Transfer LSBs.

7) Return $\overline{\text{LBE}}$ to logic "1" at least 200 ns before the next "device" is put on the data-bus.

8) Return $\overline{\text{INH}}$ to logic "1" no earlier than 100 ns before valid data is transferred. The $\overline{\text{INH}}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 2 µs to allow update of fresh accurate output data.

Notes:

— $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ data bytes can be transferred in any sequence ($\overline{\text{HBE}}$ or $\overline{\text{LBE}}$ first). The timing requirements are the same for both $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ data byte enables.

— The data output remains in the low-Z state for a minimum of 30 ns after the rising edge of $\overline{\text{HBE}}$ and/or $\overline{\text{LBE}}$, therefore data can be transferred at the rising edge of $\overline{\text{HBE}}$ and/or $\overline{\text{LBE}}$ respectively . . . provided the data hold requirement of the external device is less than 30 ns.

— $\overline{\text{INH}}$ (inhibit) input function is independent from $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ (3-state enable) inputs.

— The CB output (Converter Busy) will always produce a pulse for every LSB of output angle change, regardless of the state of the $\overline{\text{INH}}$ (inhibit) input or $\overline{\text{HBE}}$/$\overline{\text{LBE}}$ (3-state enable) inputs.

Interfacing With a 16-Bit Microprocessor

Interface between the synchro-to-digital converter (Model 1056) and a 16-bit microprocessor is illustrated in Figure 14. To simplify the system interface to peripherals and memory devices with varying access times, the microprocessor communicates with a system via an asynchronous bus. The address decoder generates the $\overline{\text{INH}}$ chip select for the converter. When the converter returns the CB signal, the microprocessor reads the data and terminates the bus cycle. Data strobes $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ enable the converter for 16-bit word transfers. If the interface software attempts an 8-bit read (i.e., the microprocessor generates only one data strobe), then a bus error ($\overline{\text{BERR}}$) is generated. $\overline{\text{BERR}}$ terminates the bus cycle and automatically generates an exception call to the operating system. Data could be transferred from the converter using the instruction MOVE.W 1056, EA, which moves a 16-bit data word from the peripheral to an effective address — either in a register on the microprocessor chip or in a system memory location.

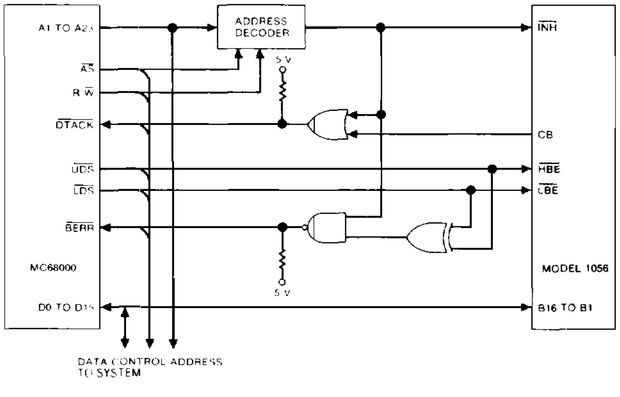


FIGURE 14 Interfacing 1056 Converter with 16-bit Microprocessor (MC68000) Via Asynchronous Bus

Analog Outputs

As a by-product of the conversion process, the Model 1056 produces various analog signals. Some of these analog signals have proven useful in various applications and are therefore brought out. The absolute value of these analog outputs is not critical to the overall conversion process. Therefore, unless otherwise specified, they are not closely controlled or characterized functions. These outputs are:

- V (pin 11), Internal analog ground (Bias)
- e (pin 12), ac error
- $\dot{\theta}$ (pin 10), Velocity output

"e," the ac error, is an ac voltage (at the output of error amplifier), which is proportional to the instantaneous error of the converter $\sin(\theta - \phi)$ . . . see theory of operation. The output "e" is also proportional to the input angular acceleration . . . the rate of change of angular velocity. This angular error as a function of acceleration is inversely proportional to the acceleration constant (K_A).

$$\text{error (degrees)} = \frac{\text{angular acceleration (degrees/sec}^2)}{K_A\,(\text{sec}^{-2})}$$

For 1 degree error, the nominal magnitude of the error voltage is 750 mV-rms. Polarity of the error is determined by demodulating (phase sensitive) this voltage with the reference voltage (RH, RL).

"$\dot{\theta}$" is a dc voltage proportional to the velocity of the digital output angle (thereby the input shaft angle). The voltage goes negative for increasing digital angle and goes positive for decreasing digital angle. At maximum tracking velocity, the output voltage is 1.1 volts-dc (1.5 volts-dc for 800 Hz model). Detailed specification for velocity functions are provided on page 7. Dynamic characteristics including open loop and closed loop transfer functions are provided below.

"V," internal analog ground, also referred to as the "bias voltage" provides a reference point for all analog functions. The typical value of the bias voltage, V, is:

$$V = 1/2\,(V_L - 0.7\text{ V-dc})$$

$$= 2.15\text{ V-dc} \pm 10\%\ (\text{for } V_L = +5\text{ V-dc})$$

All analog outputs have a minimum output drive of ±1 mA with respect to V (bias). For a power supply of +5 V-dc, the minimum output swing is ±1.1 V peak (±1.5 V peak for 800 Hz model) with respect to V (bias).

If a bipolar signal, with respect to power supply ground, is required for any analog output, a difference circuit, as shown in Figure 16, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

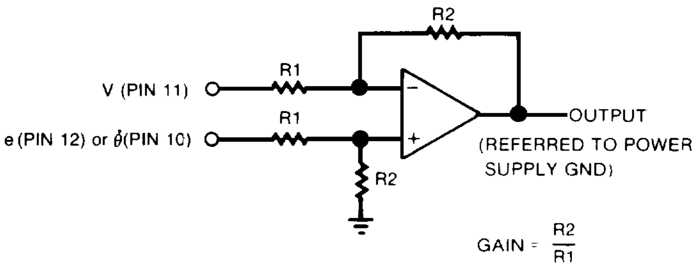


FIGURE 16 Difference Circuit for Bipolar Analog Outputs

Dynamic Performance

HSRD1056 incorporates a high gain, Type II, servo loop to provide accurate real-time synchro (resolver)-to-digital conversion. The converter is characterized for the following dynamic input angle conditions:

(1) Static Input Angle

(2) Constant Rate of Change of Input Angle Position
(Constant Velocity)

(3) Constant Rate of Change of Input Angular Velocity
(Constant Acceleration)

(4) Variable Rate of Change of Angular Velocity
(Sinusoidal Modulation)

(5) Infinite Rate of Change of Angular Velocity
(Step Input)

The 1056 accuracy specification applies for **Static (1)** and **Constant Velocity (2)** input conditions, as long as the maximum converter tracking rate is not exceeded.

For **Constant Acceleration (3)** of input angle, the digital output will lag the input by the following amount:

$$\text{Acceleration Lag (error)} = \frac{\text{Input Angle Acceleration}}{K_A}$$

The values of maximum tracking rate and acceleration constant (K_A) for different frequency options are given in the specification table (page 8). Note that the specified K_A is typical and is not a tightly controlled parameter (converter K_A is analogous to the open-loop gain of an operational amplifier).

For **Sinusoidal Shaft Angle Modulation (4),** the digital angle output will lag the input by the following amount:

$$\text{Sinusiodal Lag (error p-p)} = \frac{2 \times \pi^2 \times \text{Amp (p-p)} \times \text{Fo}^2}{K_A}$$

Where: Amp (p-p) = peak-peak angle modulation level
Fo = modulation frequency (Hz)
K_A = converter acceleration constant

The Peak Rate (Velocity) for a given sinusoidal modulation is:

Rate (degrees/sec) = π x Amp (degrees p-p) x Fo (Hz)

Dynamic Performance Continued

For **Step Inputs (5)**, the digital angle output will respond as a function of the converter's Large Signal and Small Signal transient response.

The ***Large Signal*** transient response is dependent solely on the maximum velocity (ω_{max}) and the maximum acceleration (α max) of which the converter is capable. The large signal parameters are defined in figure 17. The synchronizing time (t_{SYNC}) for large signals can be partitioned into three distinct intervals. Acceleration time (t_{ACC}) Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

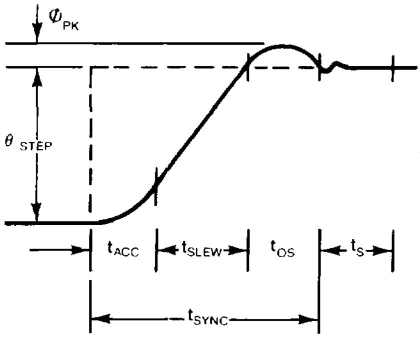
Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

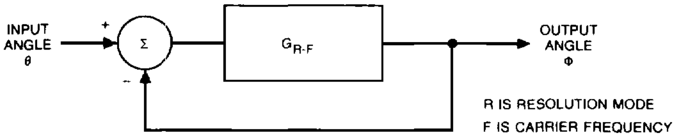
The ***Small Signal*** settling time (t_s) is specified for step inputs of less than 1.4 degrees. For small signal steps, the settling time is a function of the transient response of the converter.



$$\Phi_{PK} = \frac{\omega^2_{max}}{2\alpha_{max}}$$

$$t_{SYNC} = \frac{\theta_{STEP}}{\omega_{max}} + \frac{5}{2} \cdot \frac{\omega_{max}}{\alpha_{max}}$$

FIGURE 17 Large Signal (≥1.4°) Response Parameters



R IS RESOLUTION MODE
F IS CARRIER FREQUENCY

$$G_{14\text{-}60} = \frac{7{,}680\,(1+\frac{s}{20})}{s^2\,(1+\frac{s}{200})} \quad G_{14\text{-}400} = \frac{192{,}000\,(1+\frac{s}{100})}{s^2\,(1+\frac{s}{1000})} \quad G_{14\text{-}800} = \frac{768{,}000\,(1+\frac{s}{200})}{s^2\,(1+\frac{s}{2000})}$$

$$G_{16\text{-}60} = \frac{1.920\,(1+\frac{s}{20})}{s^2\,(1+\frac{s}{200})} \quad G_{16\text{-}400} = \frac{48{,}000\,(1+\frac{s}{100})}{s^2\,(1+\frac{s}{1000})} \quad G_{16\text{-}800} = \frac{192{,}000\,(1+\frac{s}{200})}{s^2\,(1+\frac{s}{2000})}$$

FIGURE 18 Transfer Functions for 1056

Transfer Function

The basic control loop model and transfer functions for 60-Hz, 400-Hz and 800-Hz models are shown in Figure 18. A more detailed model with corresponding transfer functions for both position and velocity outputs is shown in Figure 20. Typical values for transfer function parameters for different frequency options are shown in the table of Figure 19.

Transfer function parameters are determined by the specified frequency option and resolution mode of the converter. When a converter is operated at a frequency higher than that specified, these parameters remain the same. For some applications it may be advantageous to use a lower bandwidth converter operating at a higher carrier frequency. For example, to improve the position noise rejection, velocity output noise/ripple and velocity linearity, a 60-Hz frequency (option 6) could be used and operated at higher carrier frequencies such as 400 Hz.

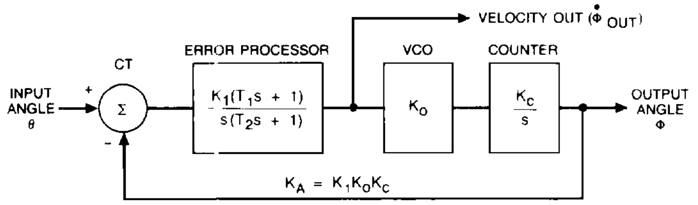
For better understanding of the dynamics of the1056, Bode plots for converter gain and output phase for 60-Hz, 400-Hz and 800-Hz options are shown in Figures 21, 22, 23 and 24.

Results of actual performance of step responses for both large and small signal inputs performed on typical converters are shown in Figure 25.

PARAMETER	UNITS	FREQUENCY OPTION					
		60 Hz		400 Hz		800 Hz	
		16 BIT	14 BIT	16 BIT	14 BIT	16 BIT	14 BIT
K_A	sec^{-2}	1,920	7,680	48,000	192,000	192,000	768,000
K_O	Counts / Volt·Sec	29,800	29,800	149,000	149,000	218,000	218,000
K_C	Radians / Count	9.587×10^{5}	3.835×10^{-4}	9.587×10^{-5}	3.835×10^{-4}	9.587×10^{-5}	3.835×10^{-4}
K_1	Volts / Radian	672	672	3360	3360	9187	9187
T_1	ms	50.0	50.0	10.0	10.0	5.0	5.0
T_2	ms	5.0	5.0	1.0	1.0	0.5	0.5
K_OK_C	Radians / Volt·Sec	2.857	11.43	14.28	57.14	20.90	83.60

FIGURE 19 Transfer Function Parameters (Typical Values)

Transfer Function Continued



POSITION GAIN (OPEN LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{K_A(T_1 s + 1)}{s^2(T_2 s + 1)}$

VELOCITY GAIN (OPEN LOOP) $\frac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \frac{K_1(T_1 s + 1)}{s(T_2 s + 1)}$

POSITION GAIN (CLOSED LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{T_2 s + 1}{\frac{T_2 s^3}{K_A} + \frac{s^2}{K_A} + T_1 s + 1}$

VELOCITY GAIN (CLOSED LOOP) $\frac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \frac{T_1 s^2 + s}{\frac{T_2 s^3}{K_1} + \frac{s^2}{K_1} + T_1 K_O K_C s + K_O K_C}$

FIGURE 20 Detailed Transfer Function Model

Bode Plots

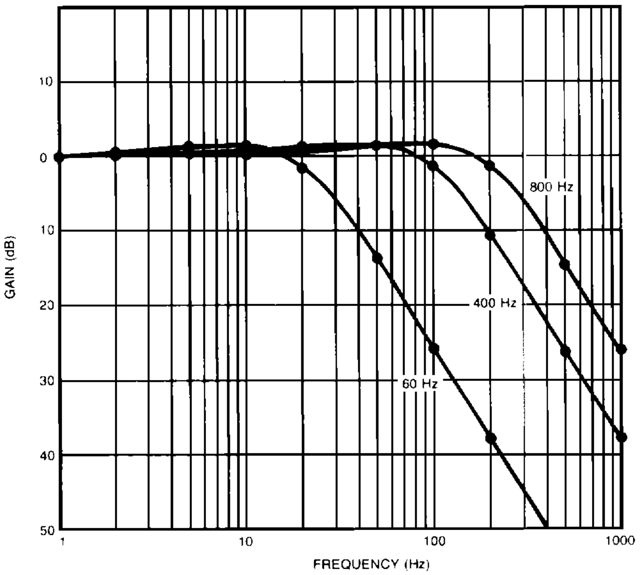


FIGURE 21 Gain Plot (16-BIT Mode)

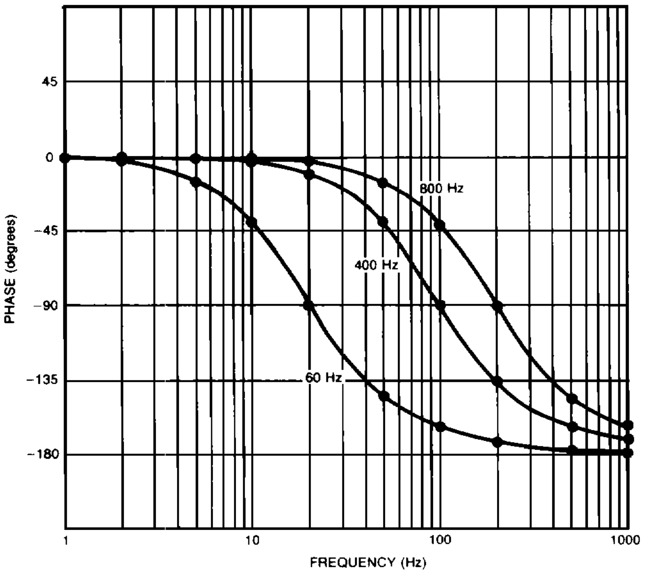


FIGURE 22 Phase Plot (16-BIT Mode)

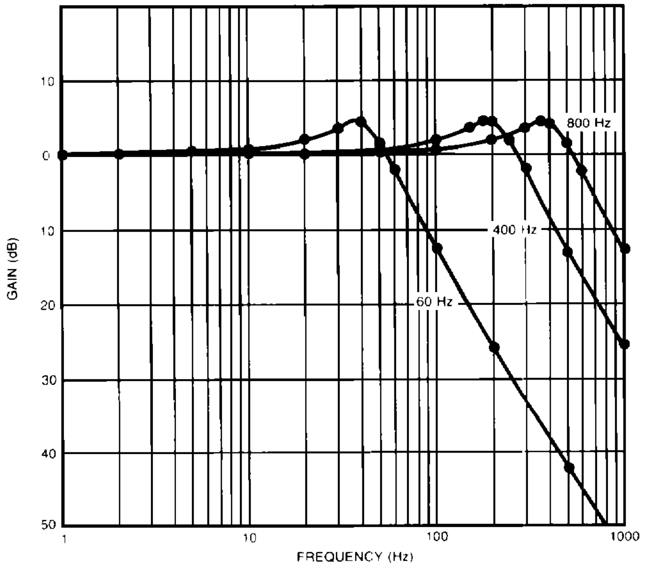


FIGURE 23 Gain Plot (14-BIT Mode)

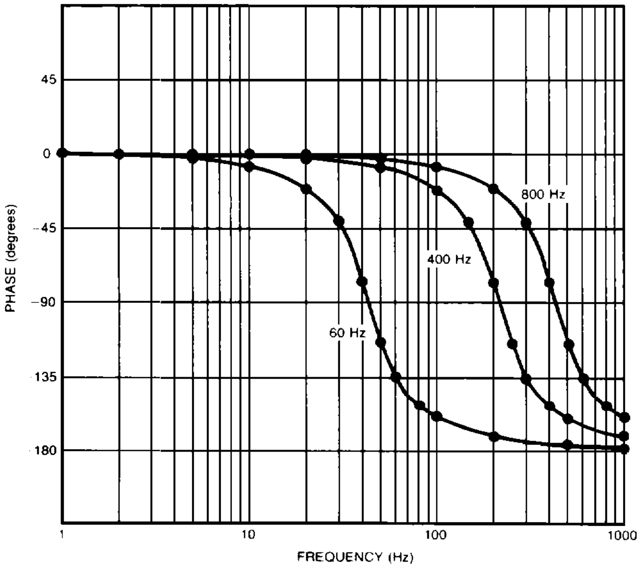
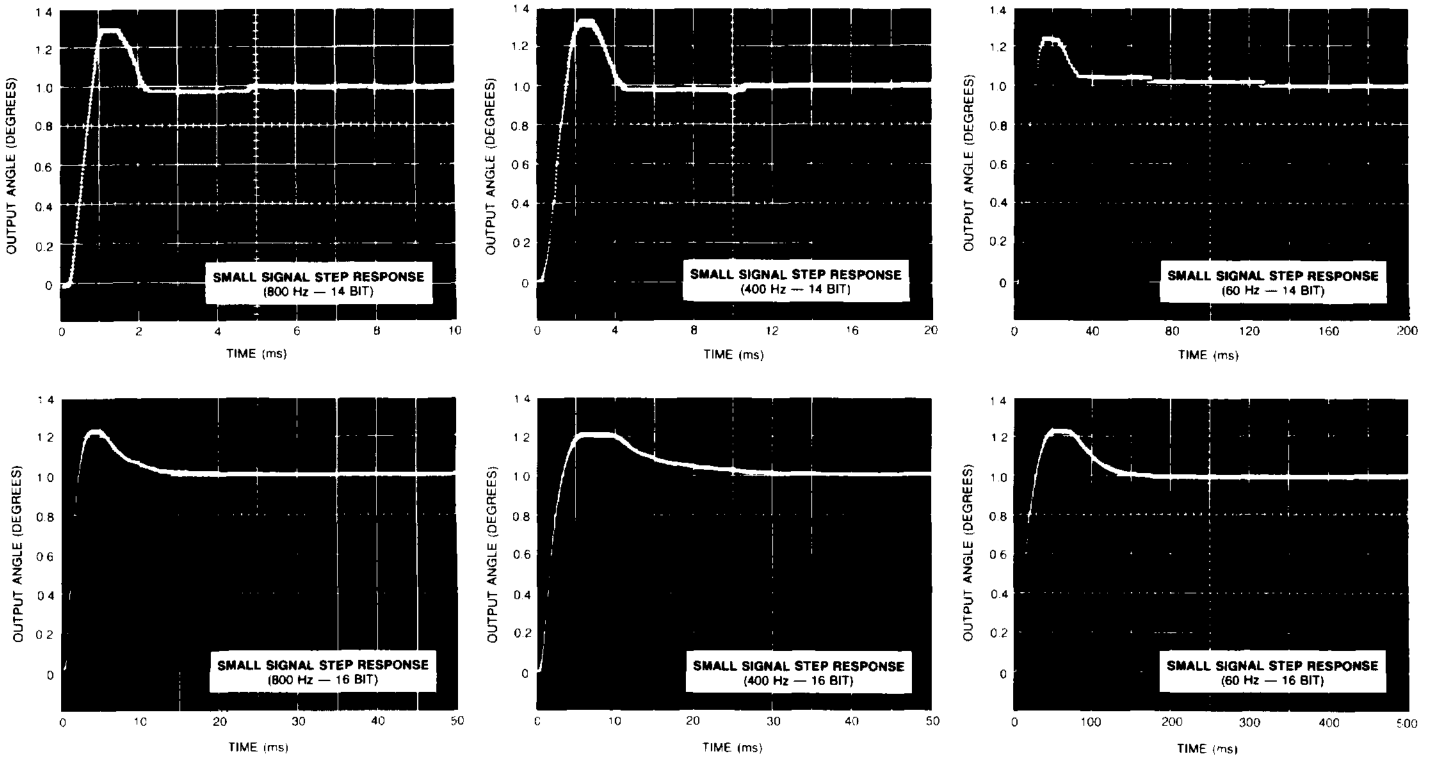


FIGURE 24 Phase Plot (14-BIT Mode)

Step Response

$V_L = +5$ V-dc, $T_a = 25°C$

Small Signal Input Step = 1.0 Degree



Large Signal Input Step = 179 Degrees

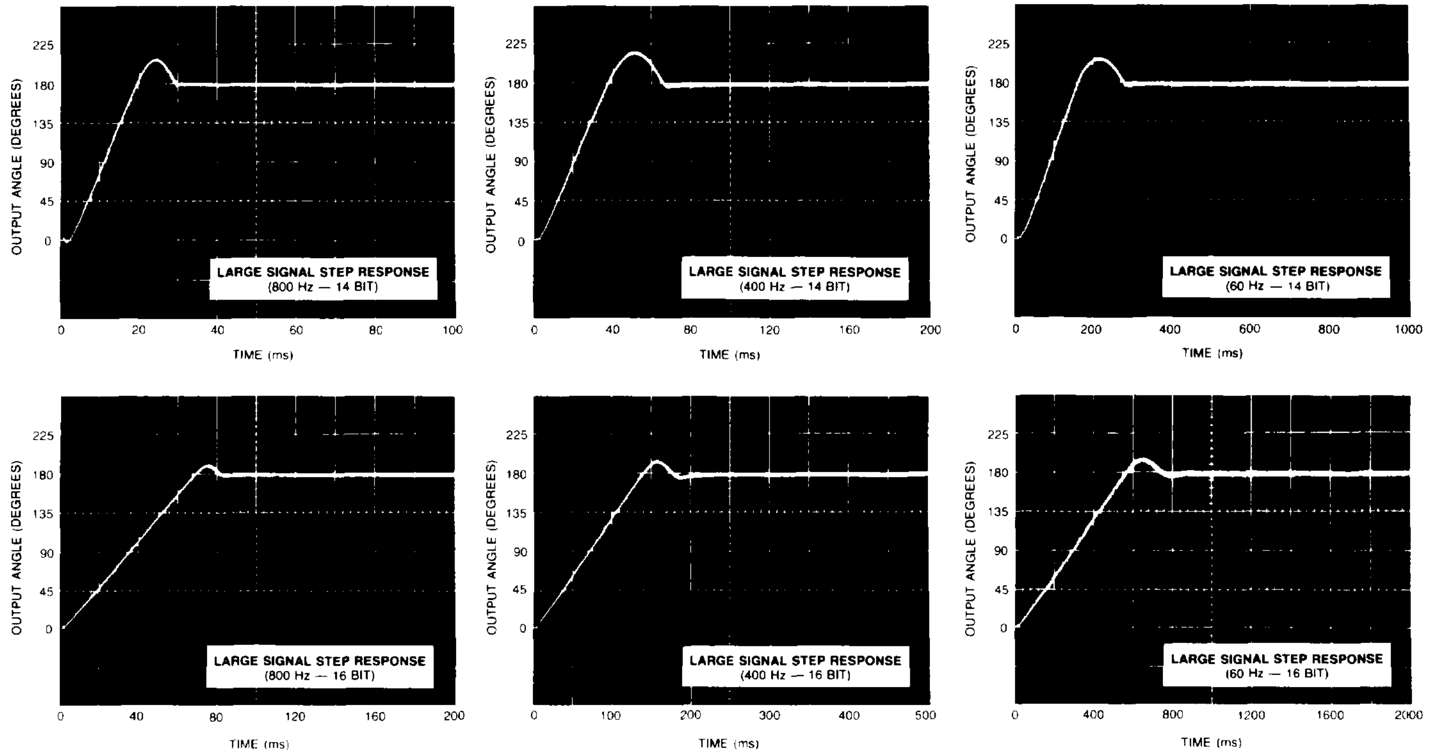
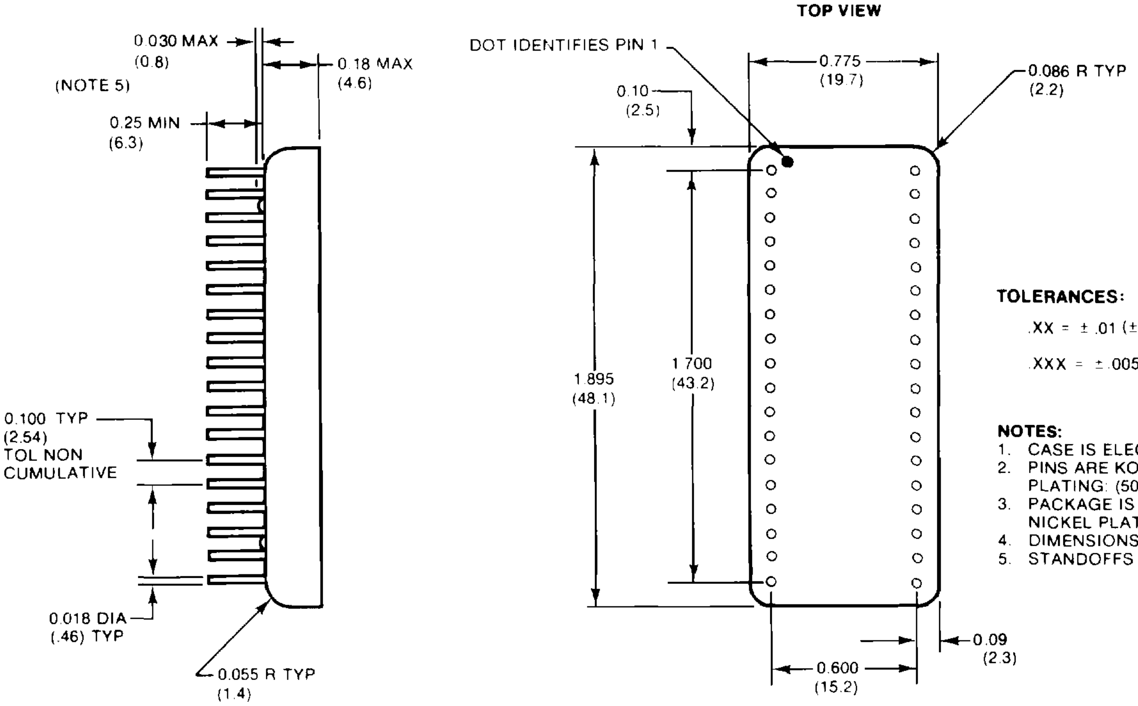


FIGURE 25 Small Signal and Large Signal Step Response



TOLERANCES:

.XX = ± .01 (±.25)

.XXX = ± .005 (±.13)

NOTES:
1. CASE IS ELECTRICALLY FLOATING
2. PINS ARE KOVAR WITH GOLD PLATING: (50µINCH MIN).
3. PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING.
4. DIMENSIONS SHOWN IN INCHES AND (MM).
5. STANDOFFS (3) CERAMIC OR GLASS

MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HSRD1056 - T F I A

Temperature Range
1 = 0° C to + 70° C
2 = −25° C to + 85° C
3 = −55° C to +125° C

Frequency
4 = 400 Hz
6 = 60 Hz
8 = 800 Hz

Accuracy
S = ±5.2 arc-minutes
H = ±2.6 arc-minutes
V = ±1.3 arc-minutes

Input Signal
1 = 11.8 V-rms
2 = 26 V-rms
9 = 90 V-rms
0 = Ext. Signal XFMRS
5 = Ext. Signal and Reference XFMRS

MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE
Contact Natel Engineering for Delivery

Other products available from NATEL

- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters with 10- to 16-bit resolutions (1000 series)
- Second generation Four Quadrant Multiplying Sin/Cos DAC (HDSC2026)
- Low cost Digital-to-Sin/Cos converter in a ceramic package (HDSC2306)
- 2-channel Digital-to-Sin/Cos converter in a single 36-pin hybrid (HDSC2036)
- 2 VA output, Digital-to-Resolver Converter in a 32-pin package (HDR2116)
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106)
- 22-bit Binary-to-BCD and BCD-to-Binary converters (SBD227 and SDB724)

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