P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
-20V	2.0Ω	-2.4V	-2.0A	—	TP2502ND
-40V	2.0Ω	-2.4V	-2.0A	TP2504N8	TP2504ND

* Same as SOT-89. For carrier tape reels specify P023 for 1,000 units or P024 for 2,000 units.
† MIL visual screening available.

Features

- ☐ Low threshold — -2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

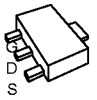
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA
(SOT-89)

Note: See package outline section for dimensions.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_A = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-1.2A	-3.3A	1.6W†	15	78†	-1.2A	-3.3A

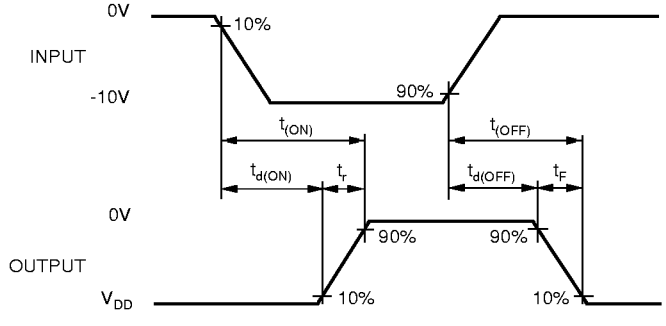
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

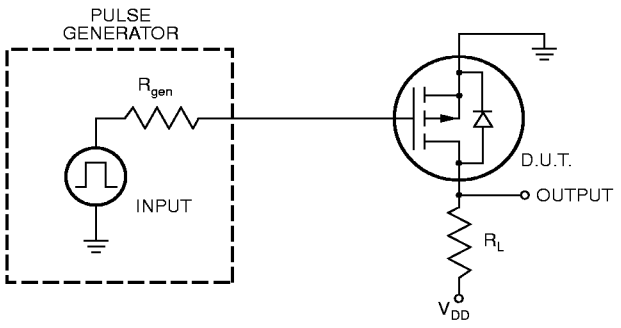
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP2502	-20			V	V_{GS} = 0, I_D = -2mA
		TP2504	-40				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D= -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			3.0	4.5	mV/°C	V_{GS} = V_{DS}, I_D= -1mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-100	µA	V_{GS} = 0, V_{DS} = Max Rating
					-10.0	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.7		A	V_{GS} = -5V, V_{DS} = -15V
			-2.0	-3.3			V_{GS} = -10V, V_{DS} = -15V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	3.5	Ω	V_{GS} = -5V, I_D = -250mA
				1.5	2.0		V_{GS} = -10V, I_D = -1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	1.2	%/°C	V_{GS} = -10V, I_D = -1A
G_{FS}	Forward Transconductance		0.3	0.65		℧	V_{DS} = -15V, I_D = -1A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = -20V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				70		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -20V, I_D = -1.0A, R_{GEN} = 25Ω
t_r	Rise Time				11		
$t_{d(OFF)}$	Turn-OFF Delay Time				15		
t_f	Fall Time				12		
V_{SD}	Diode Forward Voltage Drop			-1.3	-2.0	V	V_{GS} = 0, I_{SD} = -1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -1.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

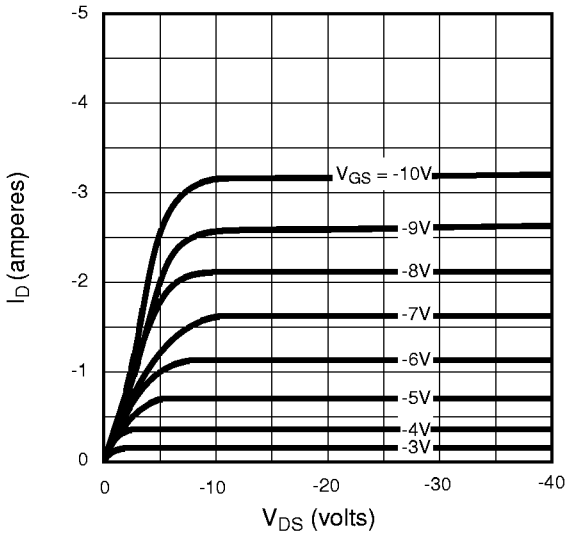
Switching Waveforms and Test Circuit



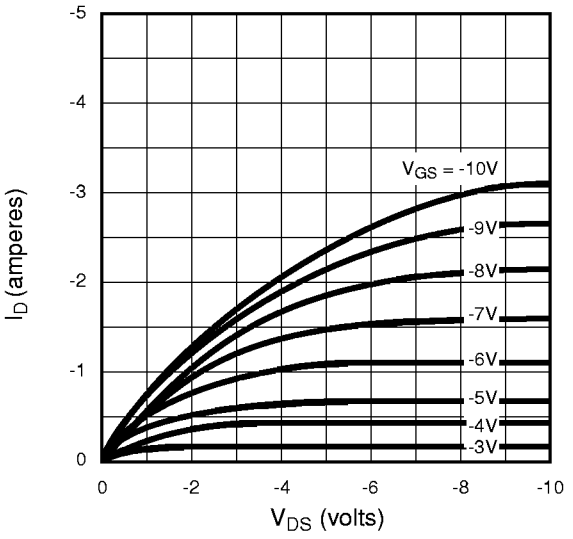


Typical Performance Curves

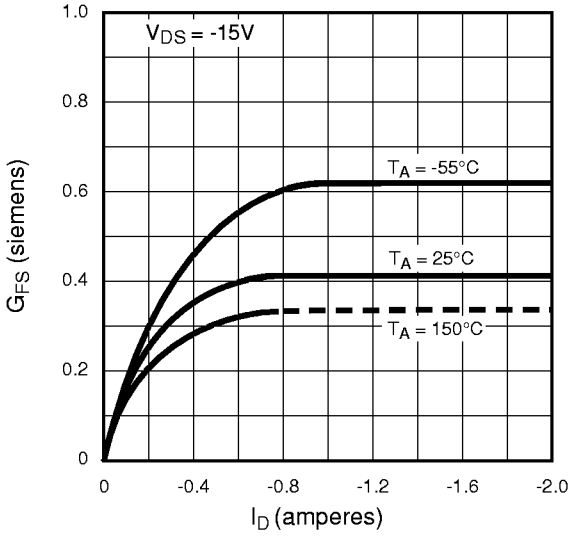
Output Characteristics



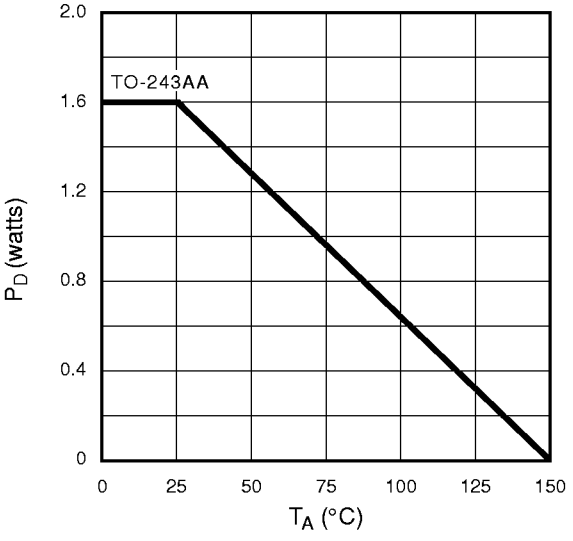
Saturation Characteristics



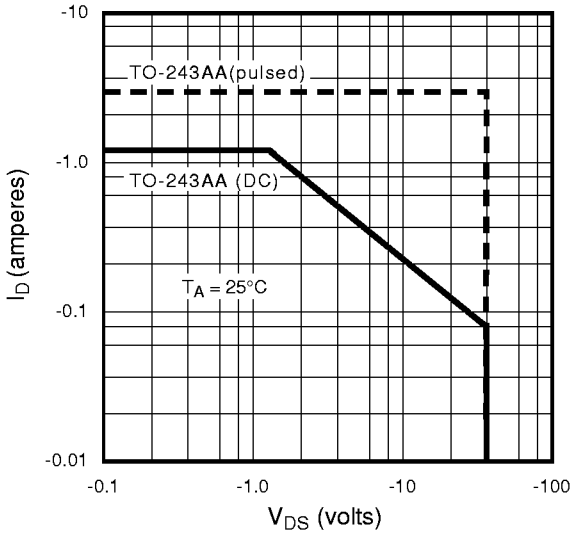
Transconductance vs. Drain Current



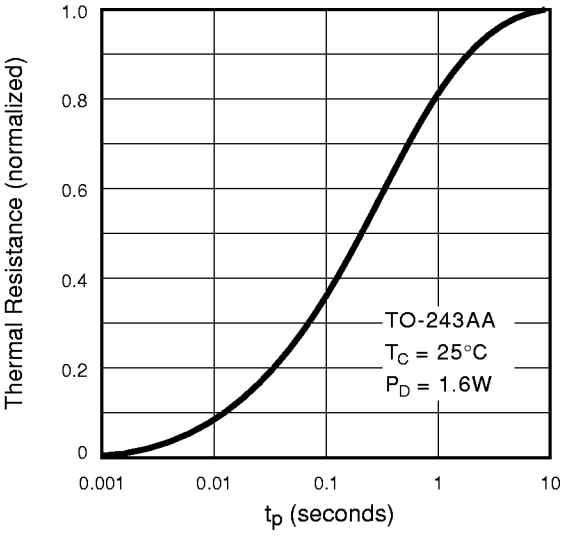
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

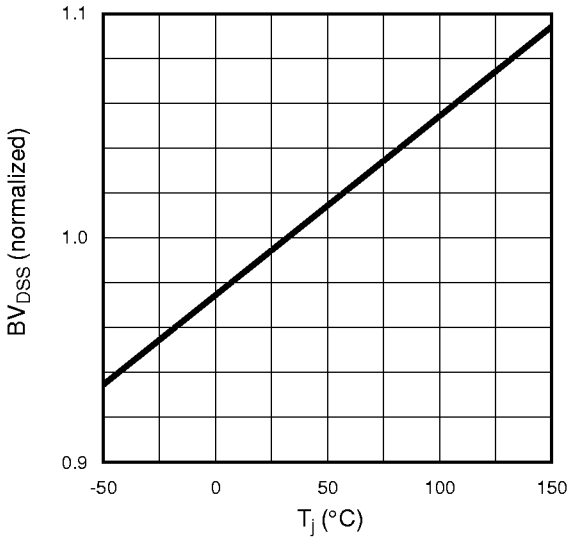


Thermal Response Characteristics

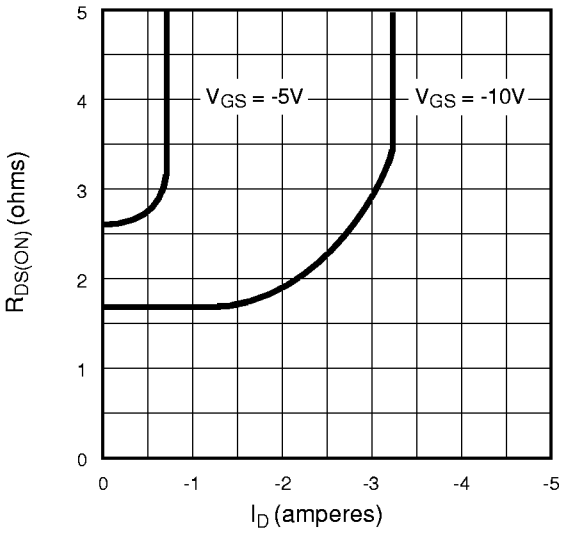


Typical Performance Curves

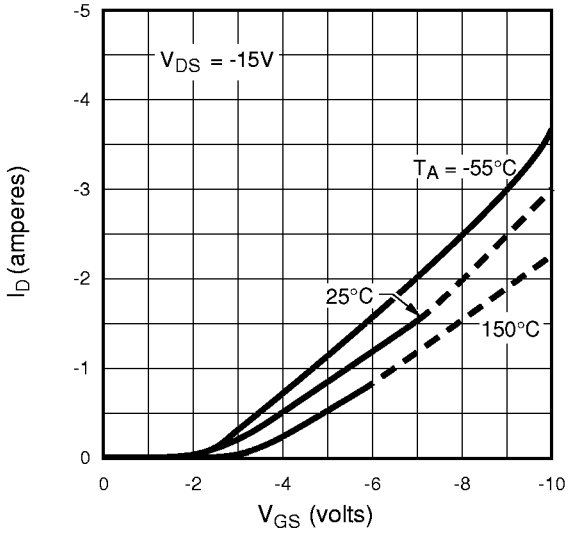
BV$_{DSS}$ Variation with Temperature



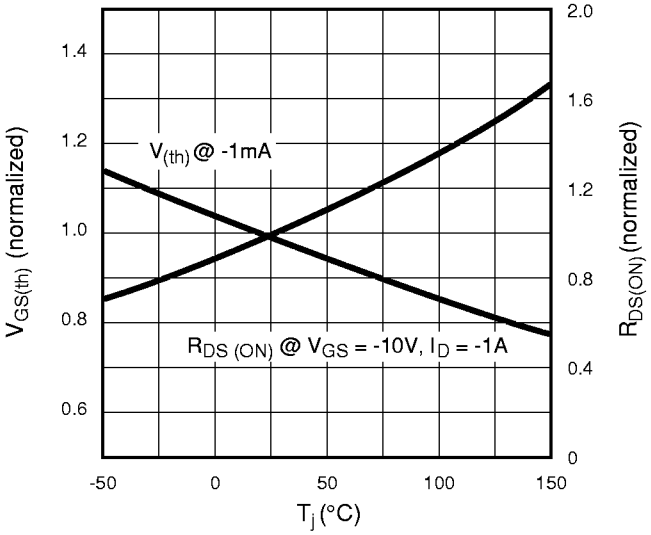
On-Resistance vs. Drain Current



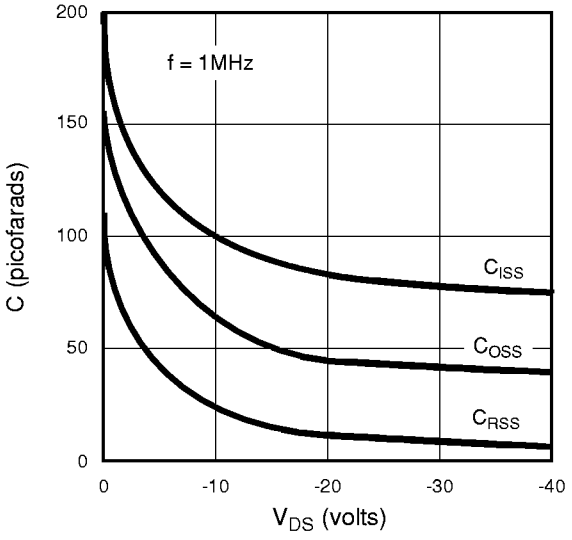
Transfer Characteristics



V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics