

82LS16 256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

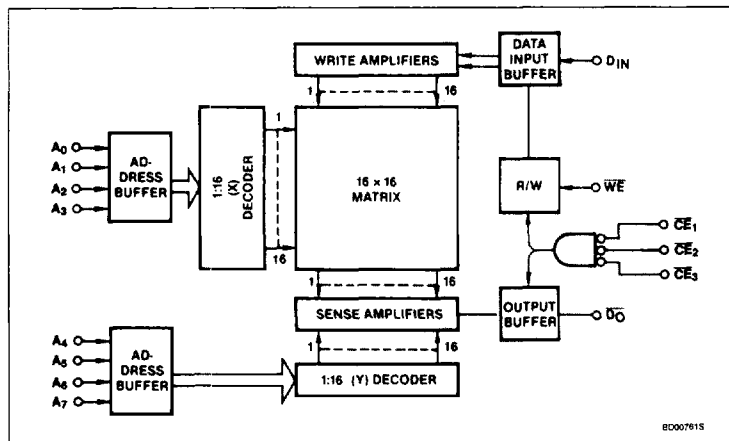
The 82LS16 is a Read/Write memory array which features 3-state outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following Write cycle.

The 82LS16 has fast Read access and Write cycle times, as well as low power requirements and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Ordering information can be found on the following page.

BLOCK DIAGRAM



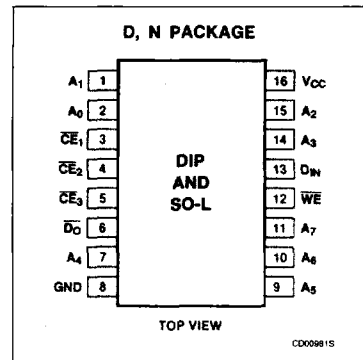
FEATURES

- Address access time: 40ns max
- Write cycle time: 25ns max
- Power dissipation: 0.99mW/bit typ
- Input loading: $-100\mu A$ max
- Output follows complement of data input during Write
- On-chip address decoding
- Three chip enable inputs
- Output: Three-state
- Schottky clamped
- TTL compatible

APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

PIN CONFIGURATION



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ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82LS16 N
Plastic Small Outline 300mil wide 16-pin	N82LS16 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OUT} Output voltage High (open collector)	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ¹	Max	
Input voltage² V _{IH} High V _{IL} Low V _{IC} Clamp ³	V _{CC} = 5.25V V _{CC} = 4.75V V _{CC} = 4.75V, I _{IN} = -12mA	2.0		0.8 -1.5	V
Output voltage² V _{OH} High V _{OL} Low ⁵	V _{CC} = 4.75V I _{OH} = -3.2mA I _{OL} = 16mA	2.6	0.35	0.45	V
Input current³ I _{IH} High I _{IL} Low	V _{CC} = 5.25V V _{IN} = 5.5V V _{IN} = 0.45V		1 -10	25 -100	μA
Output current I _{oz} Hi-Z state ⁶ I _{os} Short circuit ⁷	V _{OUT} = 5.5V V _{OUT} = 0.45V V _{CC} = 5.25V, V _O = 0V		1 -1	40 -40 -70	μA mA
Supply current⁸ I _{CC}	V _{CC} = 5.25V		50	70	mA
Capacitance C _{IN} Input C _{OUT} Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

TRUTH TABLE

MODE	CE ¹	WE	D _{IN}	D _{OUT}
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

¹"0" = All CE inputs Low; ¹"1" = One or more CE inputs High. X = Don't care.

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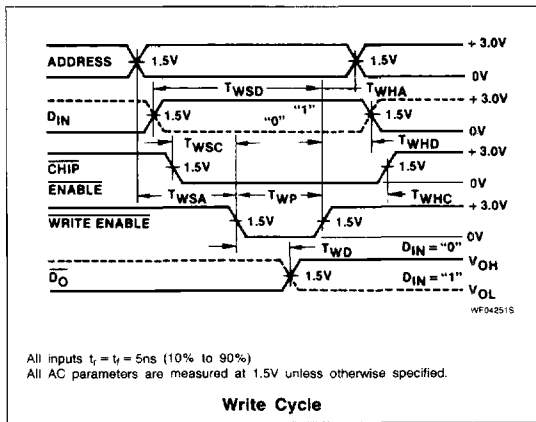
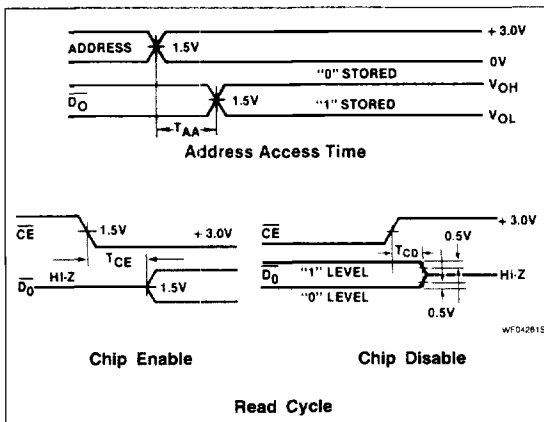
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega, R_2 = 600\Omega, C_L = 30pF, 0^\circ C \leq T_A \leq +75^\circ C, 4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ¹	Max	
Access time						
T_{AA} Address	Output	Address		30	40	ns
T_{CE} Chip enable	Output	Chip enable		15	25	
Disable time¹⁰						
T_{CD}	Output	Chip enable		15	25	ns
T_{WD} Valid time	Output	Write enable		30	40	
Set-up and hold time						
T_{WSA} Set-up time	Write enable	Address	0	-5		ns
T_{WHA} Hold time			0	-5		
T_{WSD} Set-up time	Write enable	Data in	25	15		
T_{WHD} Hold time			0	-5		
T_{WSC} Set-up time	Write enable	\overline{CE}	0	-5		
T_{WHC} Hold time			0	-5		
Pulse width⁹						
T_{WP} Write enable			25	15		ns

NOTES:

1. All typical values are at $V_{CC} = 5V, T_A = +25^\circ C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic Low stored and V_{IL} applied to $\overline{CE}_1, \overline{CE}_2$ and \overline{CE}_3 .
5. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC} .
6. Measured with V_{IH} applied to $\overline{CE}_1, \overline{CE}_2$ and \overline{CE}_3 .
7. Duration of the short-circuit should not exceed 1 second.
8. t_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega, R_2 = 750\Omega$ and $C_L = 5pF$.

TIMING DIAGRAMS



All inputs $t_r = t_f = 5ns$ (10% to 90%)
 All AC parameters are measured at 1.5V unless otherwise specified.

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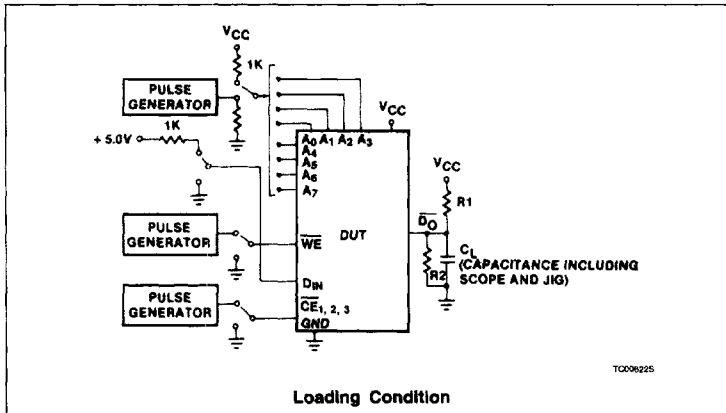
MEMORY TIMING DEFINITIONS

- T_{CE}** Delay between beginning of chip enable low (with address valid) and when data output becomes valid.
- T_{CD}** Delay between when chip enable becomes high and data output is in off state.
- T_{AA}** Delay between beginning of valid address (with chip enable low) and when data output becomes valid.

- T_{WSC}** Required delay between beginning of valid chip enable and beginning of Write enable pulse.
- T_{WHD}** Required delay between end of Write enable pulse and end of valid input data.
- T_{WP}** Width of Write enable pulse.
- T_{WSA}** Required delay between beginning of valid address and beginning of Write enable pulse.

- T_{WSD}** Required delay between beginning of valid data input and end of Write enable pulse.
- T_{WD}** Delay between beginning of Write enable pulse and when data output reflects complement of data input.
- T_{WHC}** Required delay between end of Write enable pulse and end of chip enable.
- T_{WHA}** Required delay between end of Write enable pulse and end of valid address.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

