HD153202

PLL for Timing Generator of 32 Mbps CMI Coding

Description

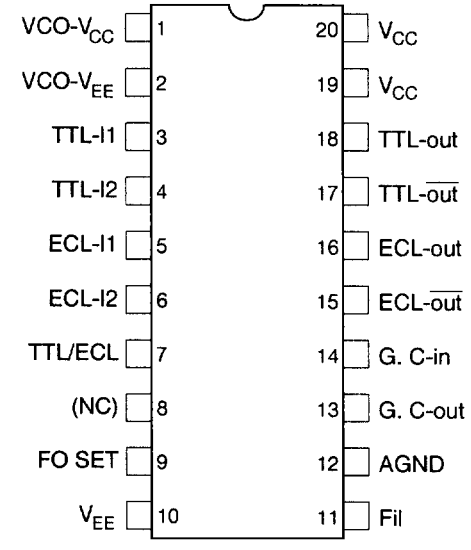
The HD153202 is a PLL (phased locked loop) IC developed for timing generation for 32 Mbps (VCO frequency of 64 MHz) CMI coding. This IC can be used with the HD153201 (CMI CODEC IC) as a chip set for building high speed low power consumption communication modules. Also, these chips may be used over the wide frequency band of 8 to 32 Mbps (16 to 64 MHz) by varying the value of an external resistance. The ratio of the input frequency at pull-in to the VCO frequency is 1:2.

Features

- A low power consumption of 175 mW (typ.)
- May be used with either ECL or TTL I/O interfaces. (However, ECL will be at pseudo ECL levels, and use of both levels at the same time is not possible.)
- The VCO oscillation frequency has a high degree of precision, and requires no adjustment.
- A fast pull-in time of 100 µs. (When the VCO oscillation frequency f_0 is 64 MHz.)
- Single voltage 5 V power supply. (When used with a TTL interface.)
- Center frequency maintained when there is no input signal.
- VCO oscillation frequency can be set by a single external resistance. (The oscillator capacitance is built in.)
- Both in phase and reverse phase VCO outputs provided.

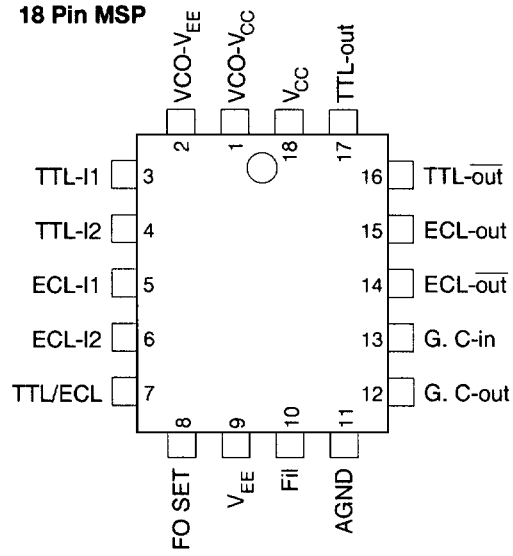
Pin Arrangement

20 Pin Plastic DIP



(Top view)

18 Pin MSP



(Top view)

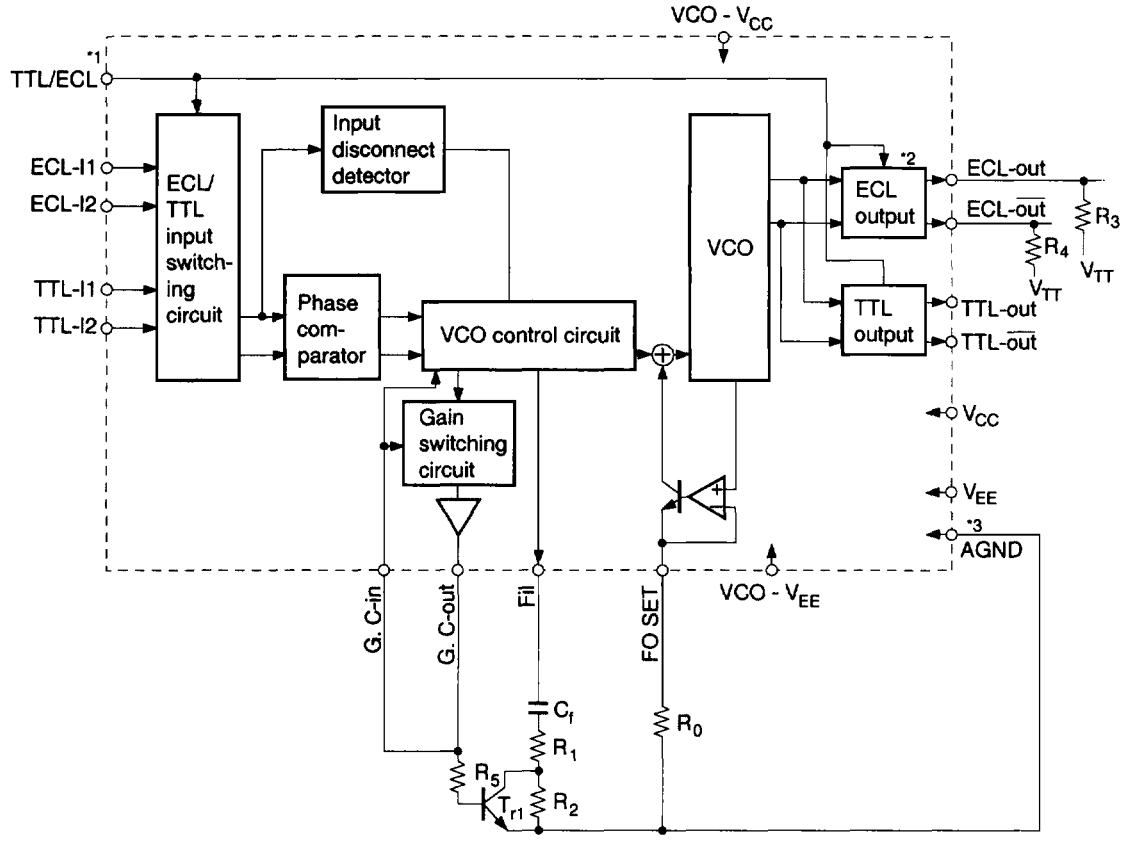
Pin Descriptions

Type	Pin Name	Pin Number DP-20	Pin Number MP-18	Function
Power supply	V_{CC}	19, 20	18	Supplies +5 V when a TTL interface is used. Connected to ground (0 V) when an ECL interface is used. In the latter case, connect directly to ground without shorting to VCO-V_{CC}. When using the DP-20 version, do not fail to connect both V_{CC} pins to the power supply.
	VCO-V_{CC}	1	1	Supplies +5 V when a TTL interface is used. Connected to ground (0 V) when an ECL interface is used. In the latter case, connect directly to ground without shorting to V_{CC}.
	V_{EE}	10	9	Connected to ground (0 V) when a TTL interface is used. Supplies –5.2 V when an ECL interface is used. Must be either directly grounded or supplied with –5.2 V without being shorted to VCO-V_{EE}.
	VCO-V_{EE}	2	2	Connected to ground (0 V) when a TTL interface is used. Supplies –5.2 V when an ECL interface is used. Must be either directly grounded or supplied with –5.2 V without being shorted to V_{EE}.
Input	AGND	12	11	The connection point for the loop filter and oscillator external resistance. Connect the loop filter between AGND and Fil, and the oscillator external resistance between AGND and FO SET. Also, connect the loop filter constant switching transistor T_r's emitter to this pin.
	TTL-I1	3	3	The TTL asynchronous signal input pin. Apply TTL level input signals. When an ECL interface is used, either leave this pin open, or pulled up or down. If pulled up or down, connect to ground or –5.2 V through a 2 to 5 kΩ resistance.
	ECL-I1	5	5	The ECL asynchronous signal input pin. Apply ECL level input signals. When a TTL interface is used, either leave this pin open, or pulled up or down. If pulled up or down, connect to either V_{CC} or 0 V through a 2 to 5 kΩ resistance.
	TTL-I2	4	4	The TTL input pin for the signal which is phase-compared to the asynchronous input signal. Apply TTL level input signals. Normally, the VCO output (TTL-out or $\overline{\text{TTL-out}}$) is applied to this pin. When an ECL interface is used, either leave this pin open, or pulled up or down. If pulled up or down, connect to ground or –5.2 V through a 2 to 5 kΩ resistance.

Pin Descriptions (cont)

Type	Pin Name	Pin Number DP-20	Pin Number MP-18	Function
Input	G. C-in	14	13	The signal input pin for switching the charge pump gain.
	ECL-I2	6	6	The ECL input pin for the signal which is phase-compared to the asynchronous input signal. Apply ECL level input signals. Normally, the VCO output (ECL-out or ECL-$\overline{\text{out}}$) is applied to this pin. When a TTL interface is used, either leave this pin open, or pulled up or down. If pulled up or down, connect to either V_{CC} or 0 V through a 2 to 5 kΩ resistance.
	TTL, ECL	7	7	The TTL/ECL I/O interface switching pin. When this pin is low, the chip will operate with a TTL interface, and when high, with an ECL interface. Setting up low or high levels should be performed with a 2 to 5 kΩ resistance, and a low level should be set by pulling down to ground (0 V), and a high level should be set by pulling up to ground (0 V).
	FO SET	9	8	The connection pin for the external resistance which sets the VCO oscillation frequency. In the HD153202, when this resistance is 2 kΩ, f0 will be 64 MHz.
	Fil	11	10	The loop filter (lug lead type) connection pin.
Output	G. C-out	13	12	The loop filter constant switching TTL level output pin. Normally connected to the base of the external transistor Tr1 through a 2 to 5 kΩ resistance.
	TTL-out	18	17	The VCO TTL output pin, and the reverse phase from TTL-$\overline{\text{out}}$. Leave open when an ECL interface is used.
	TTL-$\overline{\text{out}}$	17	16	The VCO TTL output pin, and the reverse phase from TTL-out. Leave open when an ECL interface is used.
	ECL-out	16	15	The VCO ECL output pin, and the reverse phase from ECL-$\overline{\text{out}}$. This pin is normally used terminated to V_{TT} (= –2 V) through a 50 Ω resistance. Leave open when a TTL interface is used.
	ECL-$\overline{\text{out}}$	15	14	The VCO ECL output pin, and the reverse phase from ECL-out. This pin is normally used terminated to V_{TT} (= –2 V) through a 50 Ω resistance. Leave open when a TTL interface is used.

Block Diagram

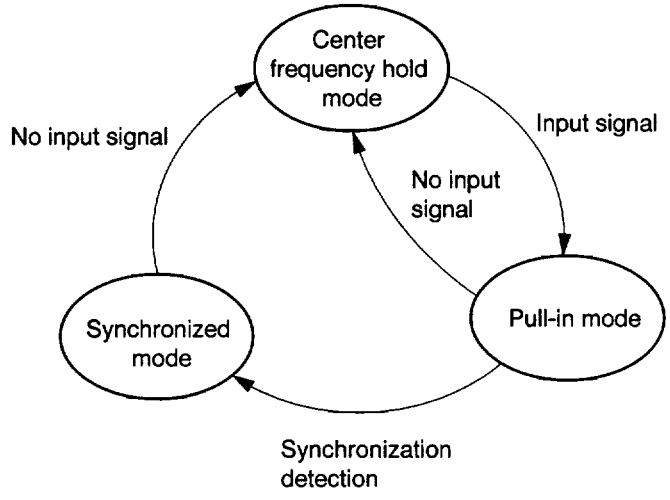


Notes: 1. Pulled down to GND (V_{EE} pin) when interfaced to TTL, pulled up to GND (V_{CC} pin) when interfaced to ECL.
2. The ECL output is from pseudo-ECL output circuits. The ECL-out and ECL-$\overline{out}$ are set to pseudo-ECL levels with individual level conversion circuits, and as a result, symmetry will be slightly distorted.
3. Do not connect the AGND pin to the board ground.

PLL State Transitions

In this PLL IC (the HD153202), PLL operation is performed by transition from center frequency hold mode to pull-in mode, and then to synchronized mode, as shown in figure 1. Therefore, if locking is lost after entering synchronized mode, it is necessary to set the input to the no input state, and after returning to center frequency hold mode, once again input the signal. The no input state is automatically recognized by internal circuitry when the input signal remains fixed for 16 counts of the VCO clock which is fed back.

An input signal should only be applied after at least 5 ms have passed following power on, when pull-in is being performed by powering up the system.



"No input signal" means that TTL-I1 or ECL-I1 is fixed in either a high or low state.

Center frequency hold mode : Maintains a free-running frequency when there is no input signal.
Pull-in mode : Rapid pull-in operation is performed at a fairly high gain.
Synchronized mode : The gain is switched to low, jitter is reduced, and synchronization is maintained.

Figure 1 PLL State Transition Diagram

Examples of External Constant Settings

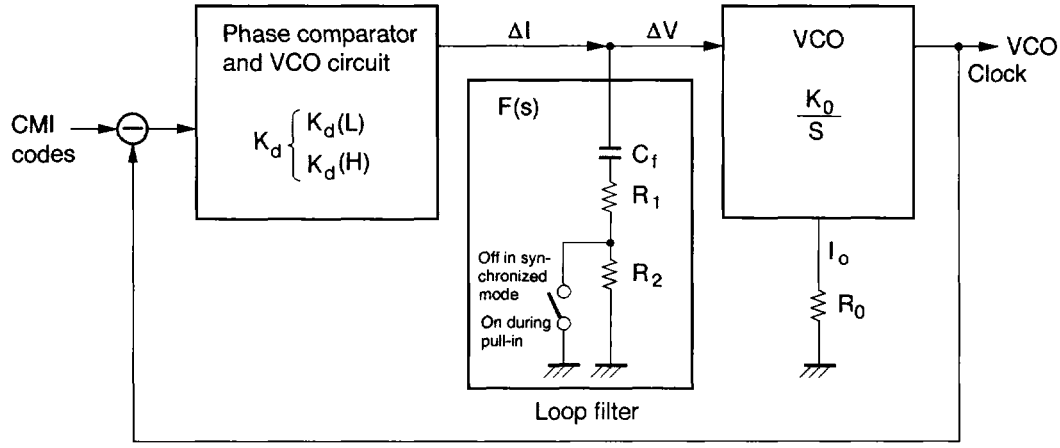
Although this device was designed for use with 64 MHz (32 Mbps) CMI code playback, it can be used over the 16 to 64 MHz range. Table 1 gives external constant examples for representative frequency bands, and the corresponding system characteristics.

R_0 is determined, as will be mentioned later, by the formula $R_0 = 1.28 \times 10^{11}/f_0$ [Hz].

Since the capture range is a narrow $4\%_{PP}$ (min) of the IC's actual ability, high precision (±1%) resistors should be used. The procedures and conditions used in determining the values of C_f, R_1, and R_2 for the 64 MHz example above will be discussed below.

Table 1

f_0	C_f	R_0	R_1	R_2	$\zeta(L)$	$B_L(L)$	$B_L(L)/f_0$
64 MHz	0.1 µF	2.0 kΩ	470 Ω	1.8 kΩ	6.2	159 kHz	$\frac{1}{402}$
32 MHz	0.1 µF	4.0 kΩ	810 Ω	2.7 kΩ	5.5	85 kHz	$\frac{1}{377}$
16 MHz	0.1 µF	8.0 kΩ	1200 Ω	4.7 kΩ	5.4	49 kHz	$\frac{1}{325}$



K_d (H): Gain of the phase comparator and VCO circuit (in pull-in mode) [µA/rad]
K_d (L): Gain of the phase comparator and VCO circuit (in synchronized mode) [µA/rad]
F (s): Loop filter transfer function

$$F(s) = R_1 \left(1 + \frac{1/(C_f R_1)}{s}\right) \quad \text{(in pull-in mode)}$$

$$F(s) = (R_1 + R_2) \left(1 + \frac{1/C_f (R_1 + R_2)}{s}\right) \quad \text{(in synchronized mode)} \quad [V/\mu A]$$

K_0: VCO gain [rad/V·sec]

Figure 2 PLL Block Diagram

Terminology

Lock range and capture range are defined below. Taking ωi as the input angular frequency and ωo as the VCO free running angular frequency, the locked state is when 2ωi = ωo.

1. Definition of the lock range

Let ω_2 be the angular frequency at which locking is lost as ωi gradually increases above ωo/2, as in figure 3, (a). Also, taking ω_4 to be the frequency at which locking is lost as ωi gradually falls below ωo/2 in figure 3 (b), the locking range ω_L can be then defined by the following formula.

$$\omega_L = \frac{(\omega_2 - \omega_4)}{\omega_0/2}$$

2. Definition of the capture range

Let ω_3 be the angular frequency at which the PLL locks as ωi, originally greater than ωo/2, gradually falls towards ωo/2 from the unlocked state, as in figure 3 (b).

Also, let ω_1 be the angular frequency at which the PLL locks as ωi, originally smaller than ωo/2, gradually rises towards ωo/2 from the unlocked state, as in figure 3 (a). The capture range ω_C can be then defined by the following formula.

$$\omega_C = \frac{(\omega_3 - \omega_1)}{\omega_0/2}$$

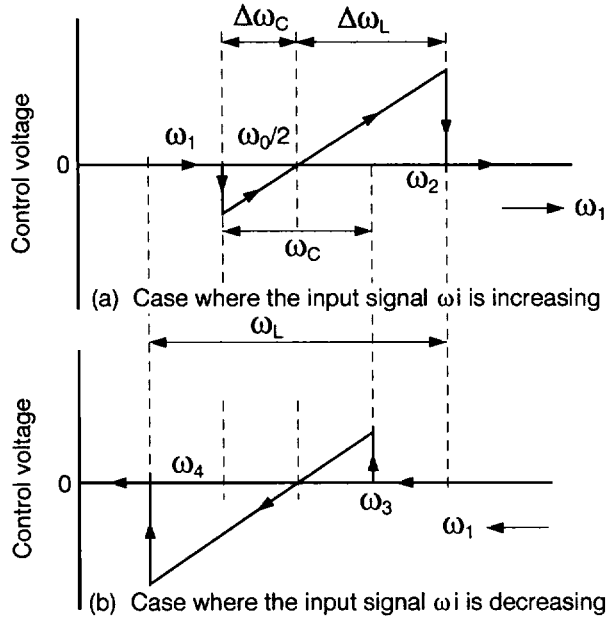


Figure 3

Absolute Maximum Characteristics (T_a = 25°C)

Item	Symbol	Rated Value	Units	Notes
Power supply voltage	V_{CC}	7.0	V	When a TTL interface is used
	V_{EE}	–7.0		When an ECL interface is used
Input voltage	V_I	–0.5 to 5.5	V	When a TTL interface is used
		0 to V_{EE}		When an ECL interface is used
Power dissipation	P_T	400	mW	
Output current	I_o	–50	mA	Applies to ECL output pins
Operating temperature	T_{opr}	0 to +75	°C	
Storage temperature	T_{stg}	–65 to +150	°C	

Electrical Characteristics

DC Characteristics 1 (TTL interface) (T_a = –20°C to +75°C)*2

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Power supply voltage	V_{CC}	4.75	5.0	5.25	V	
Power supply current	I_{CC}	—	35	50	mA	f_0 = 64 MHz, V_{CC} = 5.25 V
Input voltage*1	V_{IN}	2.2	—	—	V	V_{CC} = 4.75 V
	V_{IL}	—	—	0.7		V_{CC} = 5.25 V
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.5		V_{CC} = 4.75 V, I_{OL} = 8 mA
Output short current	I_{OS}	–20	—	–120	mA	V_{CC} = 5.25 V, V_o = 0 V

DC Characteristics 2 (ECL interface) (T_a = –20°C to +75°C)*3

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Power supply voltage	V_{EE}	–5.46	–5.2	–4.94	V	
Power supply current	I_{EE}	—	–32	–48	mA	f_0 = 64 MHz, V_{EE} = –5.46 V
Input voltage*1	V_{IH}	–1.00	—	–0.81	V	V_{EE} = –5.2 V, T_a = 25°C
	V_{IL}	–1.85	—	–1.60		
Output voltage	V_{OH}	–1.00	—	—	V	V_{EE} = –5.2 V, V_{EE} = –2 V, 50 Ω terminated, T_a = 25°C
	V_{OL}	—	—	–1.60		

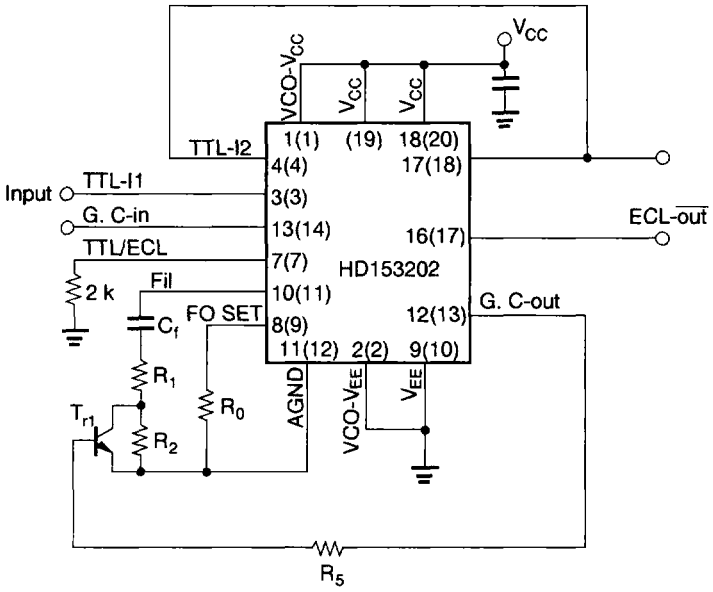
AC Characteristics (T_a = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
VCO operating frequency	f_o	—	64	—	MHz	V_{CC} = 5.0 V R_o = 2 kΩ TTL
		—	64	—	MHz	V_{EE} = –5.2 V R_o = 2 kΩ ECL
Capture range	ω_C	4	—	—	$\%_{PP}$ of f_o	f_o = 64 MHz, C_f = 0.1 µF, R_1 = 470 Ω, G. C-in = 2.7 V
Lock range	ω_L	8	—	—	$\%_{PP}$ of f_o	f_o = 64 MHz, C_f = 0.1 µF, R_2 = 4.7 kΩ, G. C-in = 0.5 V
Power supply dependency*5	$\Delta f_0/\Delta V$	—	2	—	%/V	f_o = 64 MHz*4
Temperature dependency*5	$\Delta f_0/\Delta T_a$	—	200	—	ppm/°C	f_o = 64 MHz*4

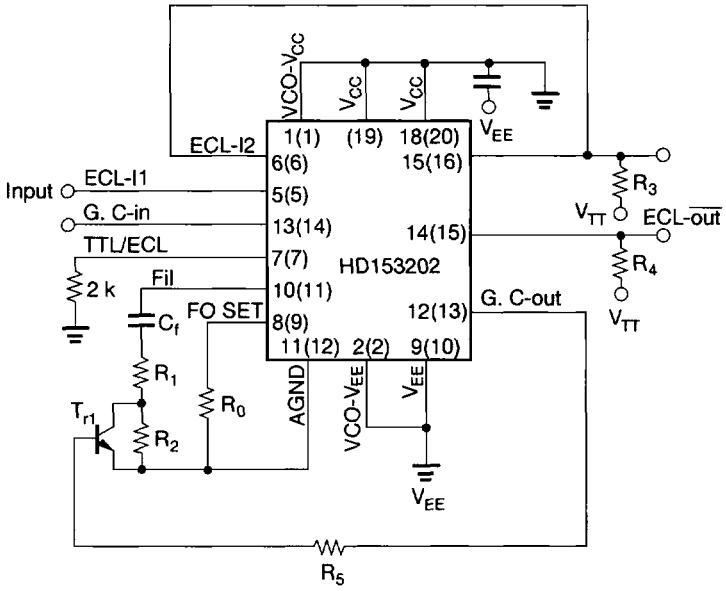
Notes: 1. The f_0-SET and Fil pins are passive component connection points, and have no input or output voltage specifications. Also, only the input levels at the G. C-in and G. C-out pins have an amplitude equivalent to TTL levels, even when an ECL interface is used.
2. With the TTL/ECL pin pulled down to ground (the V_{EE} pin) by a 2 to 5 kΩ resistance. The ECL-I1 and ECL-I2 pins are left open. (Or pulled up or down.)
3. With the TTL/ECL pin pulled up to ground (the V_{EE} pin) by a 2 to 5 kΩ resistance. The TTL-I1 and TTL-I2 pins are left open. (Or pulled up or down.)
4. This is for V_{CC} = 5.0 V for a TTL interface, or V_{EE} = –5.2 V for an ECL interface.
5. Although temperature and power supply voltages are compensated for adequately within the IC circuit itself, there are still non-linear portions remaining.

HD153202 AC Test Circuit Diagram

TTL Interface



ECL Interface



Pin numbers in parentheses are for the DP-20.

Timing Chart

This figure shows the pull-in process.

Region A: In the no input state (i.e., TTL-I1 fixed), the VCO output frequency is held at the free-running frequency f_0. Note that at this time, G. C-out will be low.

Region B: Here, a signal is input, and the circuit is performing phase pull-in. This state can be recognized by the fact that the G. C-out pin outputs a high level. The B region, up until the point where synchronization is recognized within the circuit and the G. C-out pin goes from high to low, is referred to as pull-in mode.

Region C: The PLL output is synchronized with respect to the input signal. At this time, the rising edge of the input signal and the rising edge of the PLL output which is fed back, are synchronized. (The frequency ratio will be 1:2.)

Note that this is a phase comparison method, such that the input signal frequency and the VCO frequency during pull-in take on a 1:2 ratio.

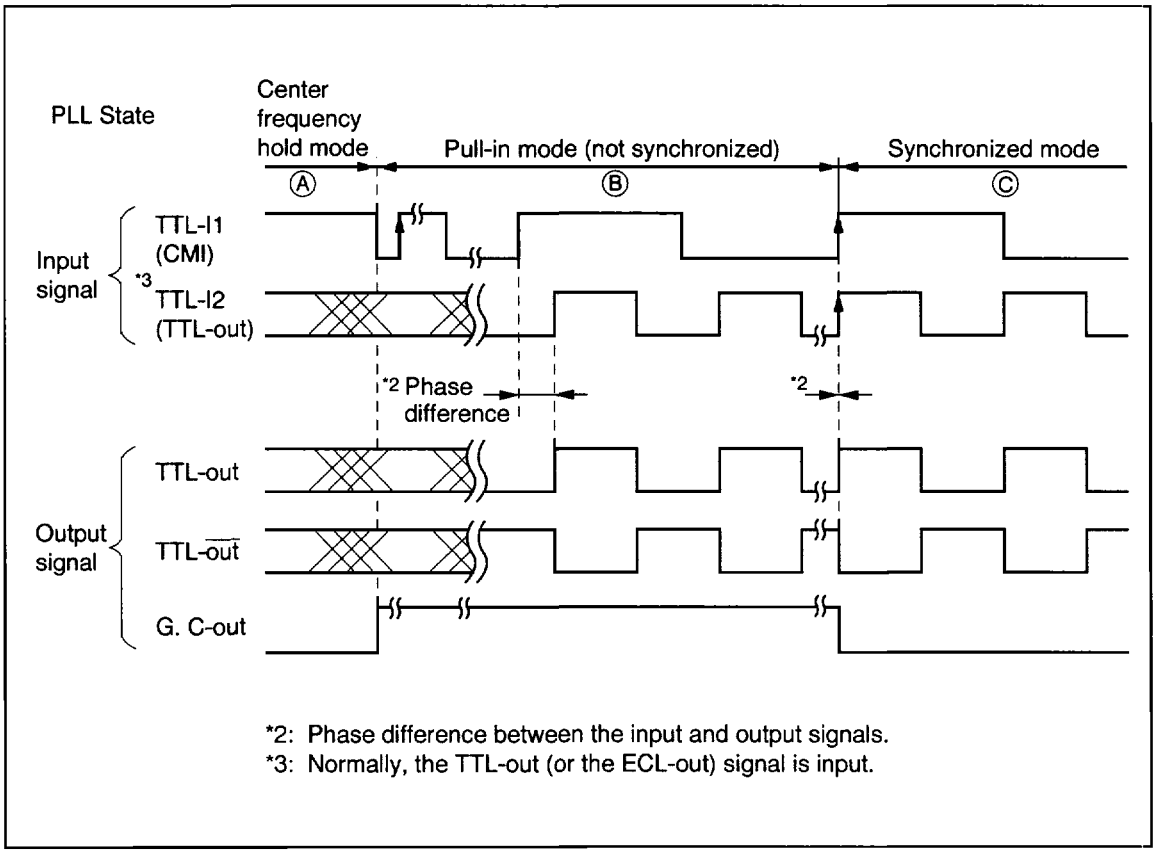
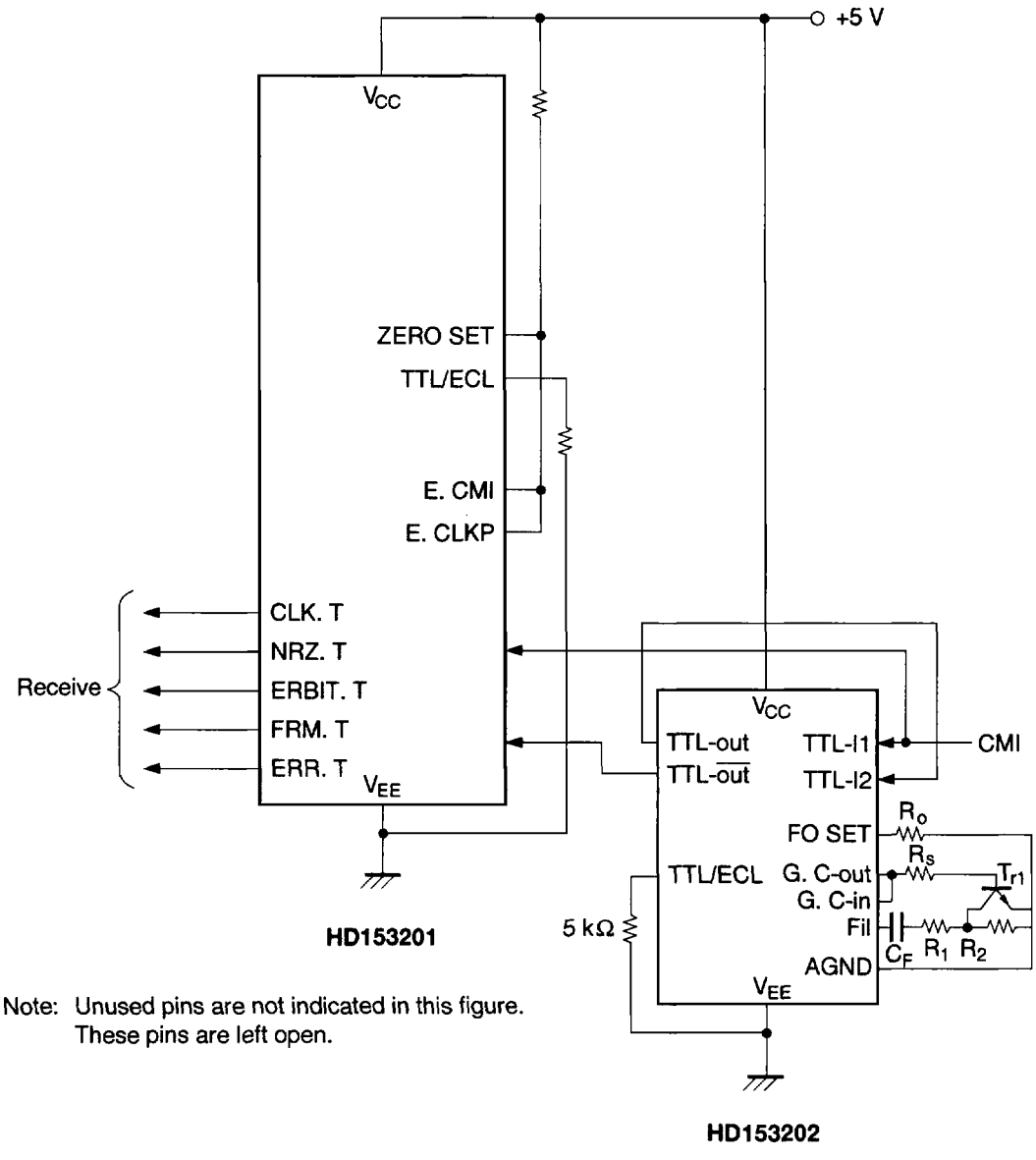


Figure 4 Timing Chart

Example of Connection to an HD153201 (TTL interface)



Note: Unused pins are not indicated in this figure.
These pins are left open.

External Components (VCO oscillation frequency f_0: 64 MHz)

Part No.	Recommended Value	Function	Notes
R_0	2 kΩ (±1%)	VCO free running frequency setting	$f_o \propto \frac{1}{R_0}$
R_1	200–700 Ω	These components make up the PLL loop filter	Refer to the section on setting the PLL constants
R_2	1.8 kΩ to 4.7 kΩ (32 Mpbs)		
C_f	0.1 µF		
R_3	50 Ω ±1%	ECL level output terminating resistance	
R_4	50 Ω ±1%		
R_5	2–5 kΩ	T_{r1} protection resistance	
T_{r1}	2SC3511	Loop filter constant switching	

Procedure for Setting External Constants (Example)

Basic Formulas for PLL Closed Loop Characteristics

The main parameters of the closed loop response characteristics in response to the input phase for a PLL of the type shown in the data sheet PLL block diagram are indicated by the formulas below. In these formulas, K_0, $K_d(H)$, and $K_d(L)$ are internal circuit constants of this IC.

This IC has two modes, the pull-in and synchronized modes, and the PLL's basic parameters have two values as shown below.

Characteristic frequency

$$\omega(H) = \sqrt{\frac{K_o \cdot K_d(H)}{C_f}} \quad (1)\ \text{(Pull-in mode)}$$

$$\omega(L) = \sqrt{\frac{K_o \cdot K_d(L)}{C_f}} \quad (2)\ \text{(Synchronized mode)}$$

Damping factor

$$\zeta(H) = \frac{C_f \cdot R_1}{2} \cdot \omega(H) \quad (3)\ \text{(Pull-in mode)}$$

$$\zeta(L) = \frac{C_f \cdot (R_1 + R_2)}{2} \cdot \omega(L) \quad (4)\ \text{(Synchronized mode)}$$

Noise band

$$B_L(H) = \frac{K_d(H) \cdot K_0 \cdot R_1 + \dfrac{1}{R_1 \cdot C_f}}{4} \quad (5)\ \text{(Pull-in mode)}$$

$$B_L(L) = \frac{K_d(L) \cdot K_0 \cdot (R_1 + R_2) + \dfrac{1}{(R_1 + R_2) \cdot C_f}}{4} \quad (6)\ \text{(Synchronized mode)}$$

Loop gain

$$K_L(H) = K_d(H) \cdot K_0 \cdot R_1 \quad (7)\ \text{(Pull-in mode)}$$

$$K_L(L) = K_d(L) \cdot K_0 \cdot (R_1 + R_2) \quad (8)\ \text{(Synchronized mode)}$$

Design Center Values of Parameters Determined by IC Internal Circuits

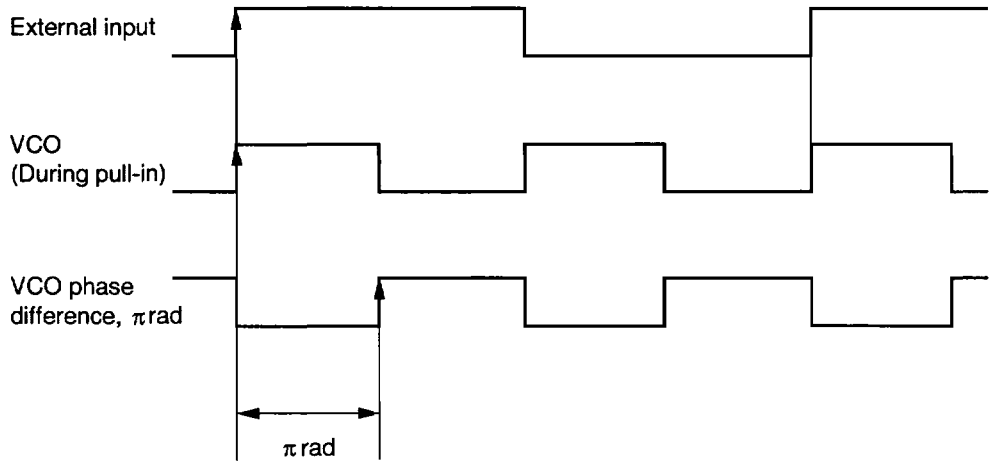
The design center values for K_0, K_d(H), and K_d(L) are as shown in the table 2 below.

Table 2

	Relational Expression	64 MHz	32 MHz	16 MHz	Units
R_0	$\frac{1.28 \times 10^8}{f_0}$	2.0	4.0	8.0	kΩ
K_d (L)*1	$\frac{4 \times 10^4}{\pi \cdot R_0}$	$\frac{20}{\pi}$*2	$\frac{10}{\pi}$	$\frac{5}{\pi}$	μA/rad
K_d (H)*1	$50 \cdot K_d$ (L)	$\frac{1000}{\pi}$	$\frac{500}{\pi}$	$\frac{250}{\pi}$	μA/rad
K_0*3	$2\pi \frac{286}{\sqrt{R_0}} \times 10^6$	$12.8\pi \times 10^6$	$9.0\pi \times 10^6$	$6.4\pi \times 10^6$	rad/V · sec

Notes: 1. (H) indicates pull-in mode, (L) indicates synchronized mode.

2. This is a phase comparator gain which becomes an output current of 20 μA in response to an input phase difference of π (rad).
   The phase difference is seen in the phase difference of the VCO waveform. (The frequency of the externally input signal is 1/2 that of the VCO.)



3. The design center value for the VCO conversion gain is 6.4 MHz/V.
   It takes 2·π (rad/sec·Hz) to convert K_0 to a phase output.

   $$6.4 \times 10^6 \times 2\pi = 12.8\pi \times 10^6 \text{ [rad/sec·V]}$$

   For other frequencies, the design is inversely proportional to $\sqrt{R_0}$.

Calculation Procedures (for the values in the data sheet)

The external constants for an application example of f_0 = 64 MHz are calculated by the following procedure.

Design conditions	Data transfer rate (Input signal frequency)	f_{IN} = 32 Mbps
	Free running frequency	f_0 = 64 MHz ($f_0 = 2 \times f_{IN}$)
	Capture range	$\omega_C \geq 4\%$ ($\Delta f/f_0 = 2\%$)
	Pull-in time	$T_P \leq 100$ µs ($\Delta f/f_0 = 2\%$)
	Damping factor	$\zeta(L) \geq 5$
	Noise band	$B_L(L)$ Confirm by calculation (This is a trade off between T_P and $B_L(L)$.)

1. Determination of R_0

This IC is for use in CMI code playback, and the VCO free running frequency f_0 is set at twice the input frequency f_{IN}. R_0 is calculated from the formula below.

$$R_0 = \frac{1.28 \times 10^8}{f_0} = \frac{1.28 \times 10^8}{64 \times 10^6} = 2.0\ [k\Omega] \quad (9)$$

2. Determination of R_1

The PLL closed loop band (angular frequency $\Delta\omega$) is generally up to the neighborhood of the value of the loop gain $K_L(H)$ (pull-in mode). Since the capture range is determined by the narrow side of the closed loop band, which is determined by the actual ability of the IC's phase comparator plus VCO, it is necessary to set the closed loop band to be relatively wide.

$$K_L(H) = K_d(H) \cdot K_0 \cdot R_1 > 2\pi \cdot \Delta f = 2\pi f_0 \cdot \frac{\omega_C}{2}$$

From this:

$$R_1 > \frac{2\pi f_0 \cdot \frac{\omega_C}{2}}{K_d(H) \cdot K_0} = \frac{2\pi \times 64 \times 10^6 \times 0.02}{\frac{1 \times 10^{-3} \times 12.8\pi \times 10^6}{\pi}} \quad (10)$$

$$= 628\ [\Omega]$$

However, there is an IC internal series impedance which is about 200 Ω. Therefore:

$$R_1 \geq 628 - 200 = 428 \rightarrow R_1 = 470\ [\Omega] \quad (11)$$

(When chosen from the 12 series.)

3. Determination of C_f

To reduce the pull in time, it is necessary for C_f to fulfill conditions 1 and 2 below.

1 It should have a capacitance such that it can be charged adequately rapidly by the output current of the phase comparator.

2 It should have a capacitance such that the response characteristic of the closed loop is adequately quick in pull-in mode.

Furthermore, it should have as large a value as possible with that range.

a. Since the center design value of the VCO conversion gain is 6.4 MHz/V [= $K_0/2\pi$] for $|\Delta f|/f_0$ = 2%, the voltage conversion capacity of C_f becomes:

$$\Delta V = \frac{f_0 \times \Delta f/f_0}{K_0} = \frac{64 \times 10^6 \times 0.02}{6.4 \times 10^6} \quad (12)$$

$$= 0.2\ [V]$$

Also, from the value for $K_d(H)$ in table 2, the output current of the phase comparator is a maximum of 1 mA (in pull-in mode) when the input phase difference is π [rad.].

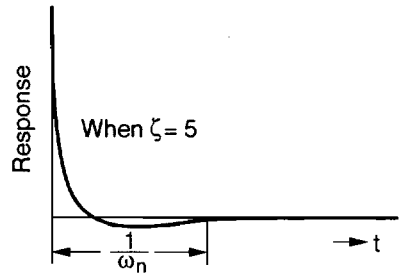
Accordingly, it is necessary for C_f to fulfill the following condition.

$$C_f \ll \frac{K_d(H) \cdot T_P}{\Delta V} = \frac{1 \times 10^{-3} \times 100 \times 10^{-6}}{0.2} \quad (13)$$

$$= 0.5\ [\mu F]$$

b. Although the response characteristic to a phase step input in the closed loop is generally as shown in the figure to the right, as will be mentioned later, since ω is taken on the larger side, the closed loop response time in the figure (PLL block diagram) is on the order of $1/\omega_n$, and it is necessary to set $1/\omega_n \ll$ TP.

$$\frac{1}{\omega_n(H)} = \sqrt{\frac{C_f}{K_0 \cdot K_d(H)}} \ll T_P \quad (14)$$



Given formula (12), and since the a priori condition is that T_P be 100 μs, the following condition holds.

$$C_f \ll K_0 \cdot K_d(H) \times (100\ \mu s)^2 \quad (15)$$

$$\ll 12.8\,\pi \times 10^6 \cdot \frac{1000 \times 10^{-6}}{\pi} \cdot (100 \times 10^{-6})^2$$

$$\ll 128\ \mu F$$

This will automatically be fulfilled when the condition of formula (13) is fulfilled.

In this example, taking a margin of a factor of 4 or 5, gives:

$$C_f = 0.1\ [\mu F] \quad (16)$$

(We are also experimenting with the same value at 32 and 16 MHz.)

In these conditions (R_1 = 470 Ω, and C_2 = 0.1 μF), the actual pull-in time will be between 70 and 90 μs.

4. Determination of R_2

The synchronized mode damping factor is taken on the larger side ($\zeta \geq 5$) in optical transmission applications.

$$\zeta(L) = \frac{C_f \cdot (R_1 + R_2)}{2} \sqrt{\frac{K_d(L) \cdot K_0}{C_f}} \geq 5 \quad (17)$$

$$(R_1 + R_2) = \frac{2 \times \zeta(L)}{\sqrt{K_d(L) \cdot K_0 \cdot C_f}} \quad (18)$$

$$= \frac{2 \times 5}{\sqrt{\frac{20 \times 10^{-6}}{\pi} \cdot 12.8\,\pi \times 10^6 \times 0.1 \times 10^{-6}}}$$

$$= 2000$$

Since R_1 is about 470 Ω plus 200 Ω, an R_2 of between 1.5 and 2 kΩ is selected.

$$R_2 = 1.8\ k\Omega \quad (19)$$

5. Confirmation of the noise band $B_L(L)$

With the constants set according to the above procedure, the synchronized mode noise band $B_L(L)$ will be as follows.

$$B_L(L) = \frac{K_d(L) \cdot K_0 \cdot (R_1 + R_2) + \dfrac{1}{(R_1 + R_2) \cdot C_f}}{4} \tag{20}$$

$$= \frac{\dfrac{20 \times 10^{-6}}{\pi} \cdot 12.8\,\pi \times 10^6 \times (470 + 200 + 1800) + \dfrac{1}{(470 + 200 + 1800) \cdot 0.1 \times 10^{-6}}}{4}$$

$$= 159 \text{ kHz}$$

$$\frac{B_L(L)}{f_0} = \frac{159 \times 10^3}{64 \times 10^6} = 0.0025 = \frac{1}{400} \tag{21}$$