1.0 Introduction

AMI Semiconductor's wireless product portfolio includes the AMIS-50050 spread spectrum baseband controller. AMI Semiconductor's AMIS-5005x products simplify the design of direct sequence spread spectrum radios. They contain all the baseband circuitry needed to implement a radio, thus providing an economical solution to the extensive digital hardware requirements of high performance spread spectrum radios. The AMIS-50050 is a low power device optimal for portable battery powered applications. It utilizes a 3.3V power supply and interfaces to a 3V microprocessor and logic.

2.0 Key Features

- Low power with user controlled 'shutdown' modes
- 3.3V (+/-10 percent)
- Narrow band and spread spectrum operation, independently selectable for transmit and receive
- Performs all baseband functions required for implementation of direct sequence spread spectrum and can be used in any radio frequency band
- User programmable transmission protocol with pass through or packetization formatting
- Generic microprocessor interface
- Full or half duplex operation
- High process gain (up to 2047chips/bit) with data rates from 100bps to 4Mbps
- Independent transmit and receive PN code generators
- Gold code and 11 -chip Barker code options
- Programmable preamble lengths for faster acquisition when there has been recent transmission or reception
- Byte-wide transmit and receive FIFOs
- 16 or 32 bit CRC error checking
- 8 or 16 bit receiver addressing
- Optional data scrambling
- Support for: binary phase shift keying (BPSK); differential binary phase shift keying (DBPSK); quadrature phase shift keying (QPSK); differential quadrature phase shift keying (DQPSK)
- Continuous tracking feature for transferring multiple packets of data at high data rates without reacquiring synchronized packet

The AMIS-50050 is a low power device optimal for portable battery powered applications. It utilizes a 3.3V power supply and interfaces to a 3V microprocessor and logic.

The AMIS-50050 IC consists of a microprocessor interface and a full duplex transmit/receive message processor circuit. Included in the AMIS-50050 message transmit processor circuits are the data scrambler, packet generator, CRC generator, pseudonoise (PN) code generator, and modulation mode formatter. The AMIS-50050 message processor receive circuits include the receive PN code generator, receive synchronization and tau-dither tracking loop, integrate and dump control, data descrambler, packet decoder, CRC checker, demodulator, and signal strength indicator. Each transmit and receive PN code generator consists of two 11-bit PN generators, allowing selection of an 'A' code, a "B" code, or a "Gold code" combination of the "A" and "B" codes. AMI Semiconductor's AMIS-50050 uses separate transmit and receive 64MHz VCOs, which allow fully independent transmit and receive operations.

AMI Semiconductor's wireless ICs interface to a generic microprocessor bus for programming and data transfer and to an IF modulator/demodulator and RF radio for the transmission medium. 8530 SCC operation and HDLC protocol are emulated for the message packetization and error checking. No packetization can be selected for data to be transmitted as received from the host.

The AMIS-50050 is a high performance part, capable of chipping rates up to 64Mchips/second in transmit and receive modes. This results in a maximum data rate of 2Mbps using QPSK or DQPSK modulation and a PN code length of 63. A maximum data rate of 1Mbps is achieved using BPSK or DBPSK modulation and a PN code length of 63. At lower chipping rates the ICs are capable of generating code lengths up to 2047 chips. The lowest possible chipping rate is 300Hz. The flexibility of the design allows an optimal combination of transmitted power, system process gain, system bandwidth and bit rate in order to achieve a reliable communication channel with minimum interference to other adjacent channels or co-channel users.

3.0 Block Diagram

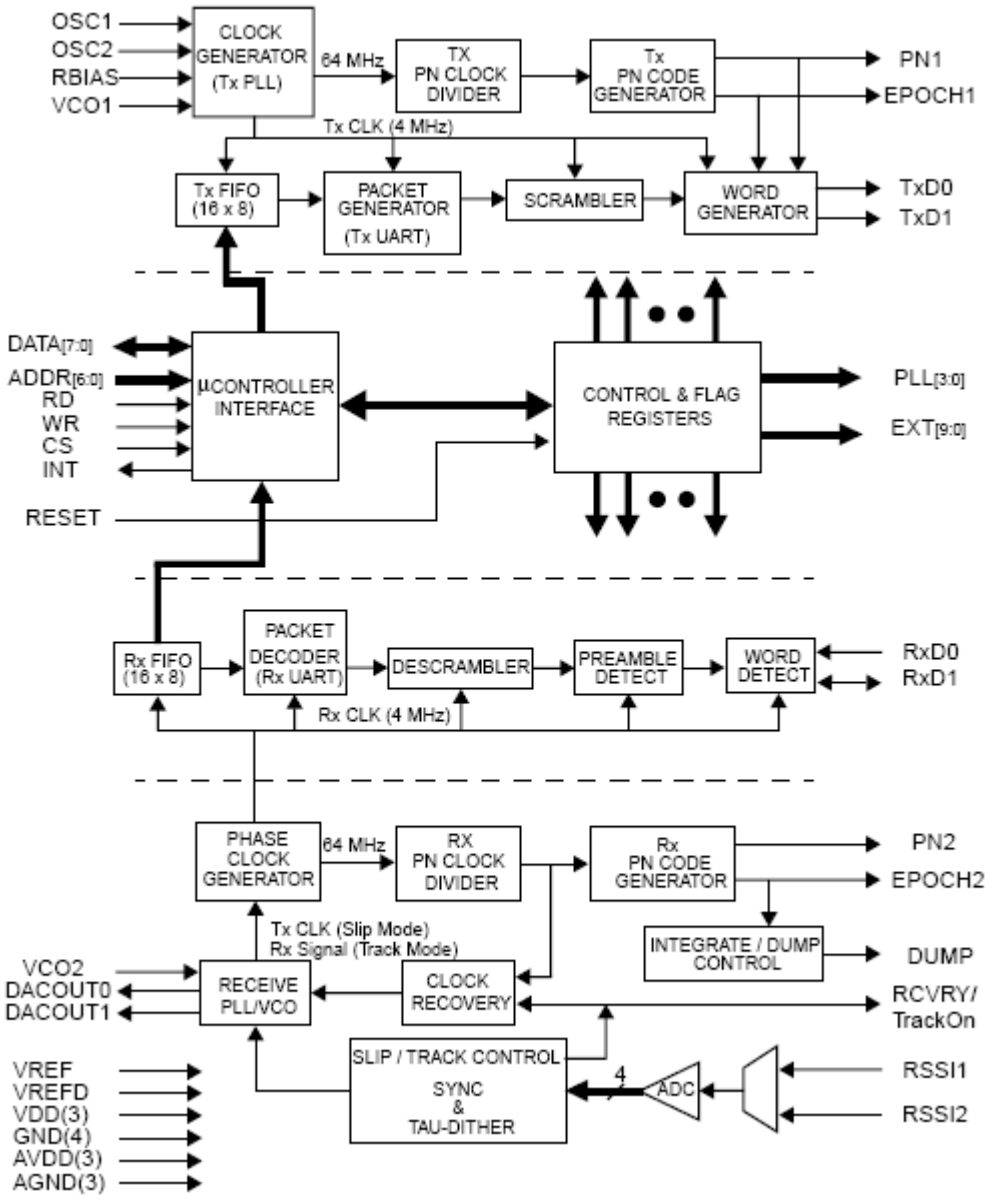

Figure 1: AMIS-50050 Block Diagram

4.0 Package Availability

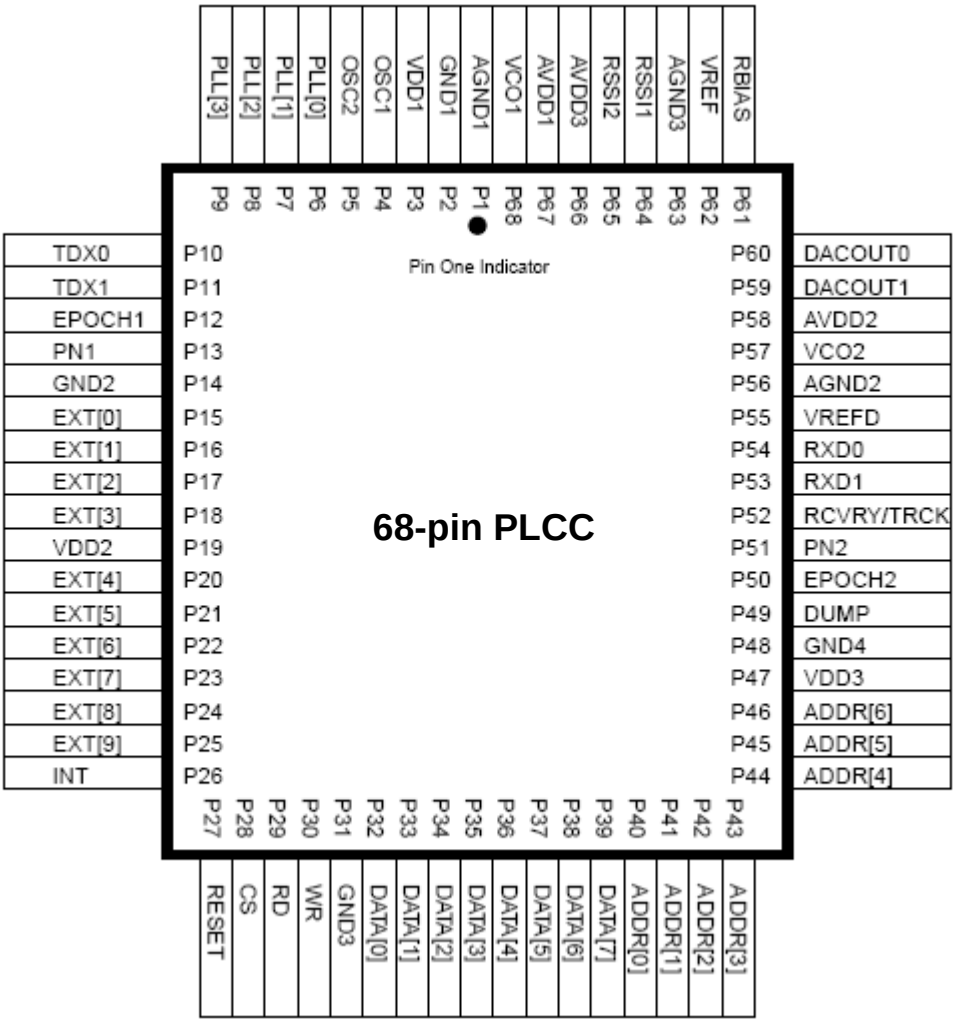

Figure 2: 68-pin PLCC Package Pin Assignments

Table 1: 68-pin PLCC Package

68-pin PLCC		
Height	**Body Size**	**Lead Spacing**
5.08mm	25 x 25mm	1.27mm

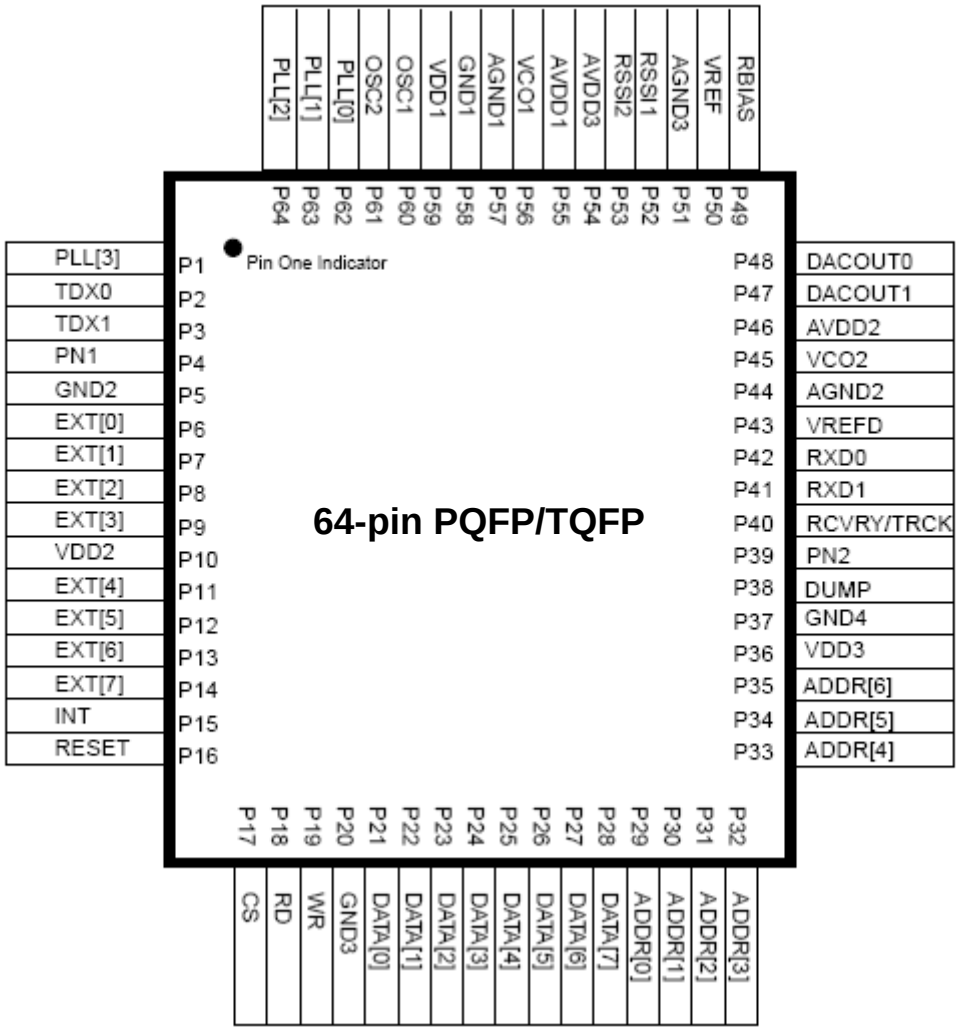

Figure 3: 64-pin PQFP/TQFP Package Pin Assignments

Table 2: 64-pin PQFP/TQFP Package

64 Lead PQFP		
Height	**Body Size**	**Lead Spacing**
3.0mm	14 x 14mm	0.80mm
68 Lead TQFP		
Height	**Body Size**	**Lead Spacing**
1.2mm	10 x 10mm	0.50mm

Table 3: Pin Descriptions

Pin Name	Type	Functional Description
AGND1	Analog GND	
GND1	Ground	
VDD1	Vdd	
OSC1	Input	Crystal oscillator or external reference input, this input is divided by OSCDIV to generate the reference clock for the transmit PLL
OSC2	Padosc	Xtal osc output
PLL[3:0]	Output	Off-chip PLL programming; Bit0, Enable1, Bit1; Sclk, Bit2, Enable0, Bit3, Sdata
TXD0	Output	Transmit data “I” output
TXD1	Output	Transmit data “Q” output, or QAM output clock
EPOCH1	Output	Transmit PN generator Epoch signal, (68 pin PLCC package only)
PN1	Output	Transmit PN generator output, can be internally disabled (PMR Bit 4)
GND2	Ground	
EXT[3:0]	Output	External control port (lower bits), user defined functions for radio control
VDD2	Vdd	
EXT[7:4]	Output	External control port (upper bits), user defined functions for radio control
EXT[9:8]	Output	External control port (upper bits), user defined functions for radio control (68 pin PLCC package only)
INT	Output	Active high – initiates an interrupt to the microprocessor
RESET	Input	Active low – sets all registers to standby states
CS	Input	Active low – selects the chip for reading and writing via the µP interface
RD	Input	Active low – initiates a read operation via the µP interface
WR	Input	Active low – initiates a write operation via the µP interface
GND3	Ground	
DATA[7:0]	BIDirection	µP interface data bus
ADDR[6:0]	Input	µP interface address bus
VDD3	Vdd	
GND4	Ground	
DUMP	Output	Integrate and dump control logic output
EPOCH2	Output	Receive PN Generator Epoch signal (68 pin PLCC package only)
PN2	Output	Receive PN generator output
RCVRY	BIDirection	Clock recovery input for narrow band mode, track-on (active high) output for spread spectrum mode – indicates to external circuitry that the PN code is locked and tracking the received PN code
TEST	Input	Pin for manufacturing test only – should be tied to ground for normal operation
RXD1	Analog I/O	Receive data input “Q” or QAM mode output clock to external shift register
RXD0	Analog In	Receive data input “I”
VREFD	Analog In	Reference voltage for integrate and dump comparators and switches
AGND2	Analog GND	
VCO2	Analog Input	Receive VCO control voltage output
AVDD2	Analog VDD	
DACOUT1	Analog Output	Receive DAC output during TRACK operation – Note: DACOUT0 and DACOUT1 are provided in the event that separate gain control is necessary for SLIP and TRACK operation
DACOUT0	Analog Output	Receive PLL DAC output during SLIP operation
RBIAS	Analog Input	Current reference for DACs and analog buffers – nominal resistor value of 20kΩ to AGND3
VREF	Analog Input	Reference voltage for ADC and DACs – value is mid-scale between VDD and GND
AGND3	Analog GND	
RSSI1	Analog Input	Analog input to the ADC – received signal strength indicator from the RF receiver, range is zero to VREF (full scale on the internal ADC)
RSSI2	Analog Input	Analog input to the ADC – received signal strength indicator from the RF receiver, range is zero to VREF (full scale on the internal ADC) This input is not usable in “SLIP” mode.
AVDD3	Analog VDD	
AVDD1	Analog VDD	
VCO1	Analog I/O	Transmit VCO voltage control output

5.0 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter	Min.	Max.	Units
VDD/AVDD	-0.3	6.0	V
Input pin voltage, all pins	-0.3	VDD+0.3	V
Input pin current, all pins	-10	10	mA
Storage temperature	-55	125	°C
Lead temperature		300	°C for 10 seconds

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Operational Range

Table 5: Operational Range

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD/AVDD	Supply voltage	3	3.3	3.6	V
Ta	Operating temperature	-40		85	°C

5.3 DC Electrical Operating Characteristics

Table 6: DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
Vil	Input low voltage			0.25VDD	V
Vih	Input high voltage		0.7VDD		V
Vol	Output low voltage	Iol = 2mA		0.4	V
Voh	Output high voltage	Ioh = -1mA	2.4		V
Iil	Input leakage	Vi = 0V to VDD/AVDD		+/-10	µA
Ioz	Output leakage	I/O = Hi impedance Vo = 0V to VDD/AVDD	300	+/-10	µA
OSCI Vil*	Input low voltage			0.1LVDD	V
OSCI Vih*	Input high voltage		0.9VDD		V

Note: * These levels are needed on the OSCI input if it is being driven by an external clock.

5.4 AC Characteristics

Table 7: AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
DAC LSB	DAC current source, least significant bit		10.3		µA
DAC Zero	DAC current with 0 input			100	nA
DAC FS (1)	DAC current source, with HEX F input	+/-100	+/-155	+/-200	µA
DAC DIFF LIN	DAC differential non-linearity		+/-0.1		LSB
ADC STEP (2)	ADC first step		130		mV
ADC LSB	ADC least significant bit		103		mV
ADC FS	ADC full scale		1.56		V
ADC DIFF LIN	ACD differential non-linearity		+/-0.3		LSB
VCO GAIN	VCO gain		45		MHz/V
RXDRES	RXD0/1 resistance		74		Ω
VCO GAIN	Comparator input low voltage			1.5	V
RXDRES	Comparator input high voltage	1.8			V

Note: Specified typical values are from characterization at 25°C, 3.3V AVDD, VDD. FS means full scale.
(1) Source and sink
(2) ADC STEP1 includes offset. Successive steps defined by ADC/LSB value.

5.5 IDD Characteristics

Table 8: IDD Characteristics

Symbol	Conditions	Max.	Units
ISLEEP	Sleep mode	50	µA
ITXS	TX standby	21	mA
IRXS	RX standby	38	mA
IALL	Full duplex	70	mA
IPIN	Full duplex with PN1 disabled	68	mA
ITXON1	TX on, RX VCO off	41	mA
ITXON2	TX on, RX VCO on	58	mA
IRXON	RX on	58	mA

Notes: All IDD tests are done at AVDD = VDD = 3.6V, 1Mbps BPSK, 64MHz chipping, internal transmit PN code mixing A and B Gold codes, 50pF load using indicated condition.

6.0 Microcontroller Interface Read/Write Timing

6.1 Read Timing Characteristics

Table 9: Read Timing Characteristics

Symbol	Parameter	Min.	Max.	Units
Tcsd	Read chip select low to valid data out		60	nS
Trd	Read low to valid data out		60	nS
Tcsdz	Chip select high to data bus disable		25	nS
Trdz	Read high to data bus disable		25	nS
Tcsur	Read chip select setup	0		nS
Tchr	Read chip select hold	10		nS
Tadrsur	Read address setup	10		nS

Note: See Figure 4: Read Timing Diagram

6.2 Write Timing Characteristics

Table 10: Write Timing Characteristics

Symbol	Parameter	Max.	Units
Tcsuw	Write chip select setup	0	nS
Tchw	Write chip select hold	10	nS
Tadrsuw	Write address setup	10	nS
Tadrh	Write address hold	10	nS
Tdsu	Write data setup time	15	nS
Tdh	Write data hold	10	nS

Note: See Figure 5: Write Timing Diagram

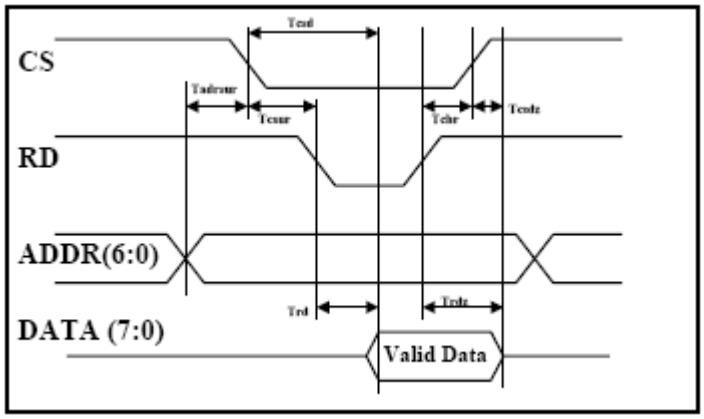

Figure 4: Microcontroller Read Timing

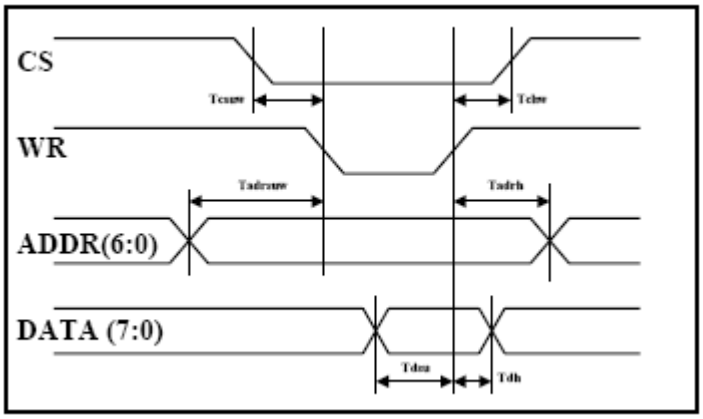

Figure 5: Microcontroller Write Timing

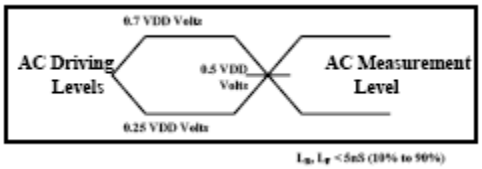

Figure 6: Input Test Waveforms and Measurement Levels

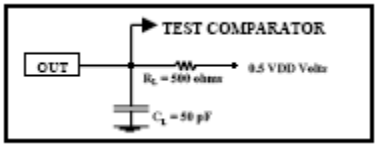

Figure 7: Output Test Load

7.0 AMIS-50050 Ordering Codes

Table 11: Ordering Codes

Device Number	Package
08906-002-XTP (or –XTD)	68 Lead PLCC
08906-003-XTP (or –XTD)	64 Lead PQFP
08906-004-XTP (or –XTD)	64 Lead TQFP
08906-808-XTP (or –XTD)	64 Lead TQFP (green/RoHS)

XTP – Tape & Reel
XTD – Tube/Tray

8.0 Company or Product Inquiries

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