TS 8368

BIPOLAR HIGH-SPEED 8-BIT FLASH A/D CONVERTER

2

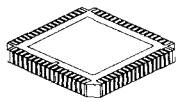
DESCRIPTION

The TS 8368 is a monolithic bipolar 8-bit parallel flash analog-to-digital converter designed for applications requiring very high-speed conversion.

The TS 8368 uses 256 parallel comparators to digitize fast moving analog input signals without the need of external sample-and-hold circuits or input buffers. The analog input is designed for 0 to − 2 V operation. Midpoint reference tap is provided for linearity adjustment or transfer function modification. An analog return pin can be driven with a buffered analog input to enhance dynamic performance. The output datas includes an overflow bit and data ready output signal. Control pins allow the user to select among binary, inverted binary, two's complement and Inverted two's complement coding.

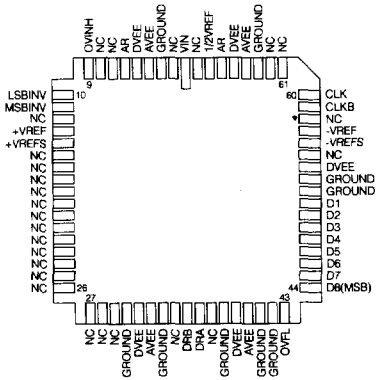
With encode rates up to 330 MHz, the TS 8368 is specified to operate from commercial to military temperature range, up to analog input frequency of 100 MHz, making it useful for a variety of applications and environments.

The TS 8368 is packaged in hermetic 68-pin LCCC configuration and also in die form.



LCCC 68
(Leadless Ceramic Chip Carrier)

PIN CONNECTIONS
(Top view)
LCCC - 68 pins



Note : In TCS device pin 30 and 31 are not connected. For details, see «*pin description*».

MAIN FEATURES

- 8-bits resolution.
- 330 MHz sampling rate.
- 250 MHz analog bandwidth.
- Low power : 1.95 W.
- Single − 5.2 V power supply.
- − 55°C / + 125°C specified.
- ECL 10 K compatible.
- Overflow bit & bit invert functions.
- Data ready output.
- Very low input capacitance : 18 pF
- No sample & hold required.
- Pin to pin compatible with AD9028.

APPLICATIONS

- Military systems.
- Radar pulse analysis.
- Video digitizing.
- Image processing.
- Medical imaging.
- High energy physics.
- X-Ray and ultrasound imaging.
- Communication/signal intelligence.

ABSOLUTE MAXIMUM RATINGS (see Note 1)

Symbol	Parameter	Value	Unit
A_R	Positive supply voltage (see Note 2)	−0.3 to +5.5	V
AV_{EE}, DV_{EE}	Negative supply voltage (see Note 2)	−6 to +0.3	V
$+V_{REF}$, $+V_{REFS}$	Upper reference voltage	−2.1 to +0.1	V
$-V_{REF}$, $-V_{REFS}$	Lower reference voltage		
1/2 V_{REF}	Midscale reference voltage		
V_{IN}	Analog input voltage		
$+V_{REF}$ to $-V_{REF}$	Reference voltage range	2.2	V
CLK, CLKB	Clock input voltages	V_{EE} to 0	V
DV_{EE} to AV_{EE}	Maximum difference between negative supplies	±0.5	V
I_D	Digital output current	20	mA
I (1/2 V_{REF})	Midscale reference current	4	mA
T_j	Junction temperature	+175	°C
T_{stg}	Storage temperature	−65 to +150	°C
T_{case}	Operating temperature range	−55 to +125	°C
T_{leads}	Lead temperature (soldering 10 s)	+260	°C
LSB_{INV}, MSB_{INV}, OV_{INH}	Digital input voltages	V_{EE} to 0	V

Note 1 : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions.
Long exposure to maximum rating may affect device reliability.

Note 2 : With respect to AGND = DGND.

USER WARNING

The power supplies must be applied before all the other signals to damage from occuring on the devices.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

$AV_{EE} = DV_{EE} = -5.2\,V$; $AR = +4\,V$; $R_L = 100\,\Omega$ to $-2\,V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	TS 8368B Min.	TS 8368B Typ.	TS 8368B Max.	TS 8368A Min.	TS 8368A Typ.	TS 8368A Max.	Unit
RESOLUTION				8			8		Bits
DIGITAL INPUTS AND OUTPUTS									
Logic compatibility				ECL 10K			ECL 10K		
Clock inputs									
• Logic «0» voltage	full	IV			−1.5			−1.5	V
• Logic «1» voltage	full	IV	−1.1			−1.1			V
Output data									
• Logic «0» voltage (see Note 1)	full	II, D			−1.5			−1.5	V
• Logic «1» voltage (see Note 2)	full	II, D	−1.1			−1.1			V
MAXIMUM CLOCK FREQUENCY		III	300	330		300	330		MHz
ANALOG INPUT									
Voltage range	*full*	V		2			2		V
Input capacitance		IV		20			20		pF
Input resistance		V		100			100		kΩ
Analog bandwidth (see Note 3)		V		250			250		MHz
REFERENCE INPUT									
Differential reference voltage	full	II, D		2	2.1		2	2.1	V
Reference ladder resistance		I, D	80	110	140	80	110	140	Ω
	full	II	65		165	65		165	Ω
POWER REQUIREMENTS									
Positive supply voltage		I, D	0	4	5	0	4	5	V
	full	II	0	4	5	0	4	5	V
Positive supply current		I, D		15	23		15	23	mA
(AR = +4 V)	full	II			25			25	mA
Negative supply voltage		I, D	−5.7	−5.2	−4.7	−5.7	−5.2	−4.7	V
	full	II	−5.7	−5.2	−4.7	−5.7	−5.2	−4.7	V
Negative supply current		I, D		360	450		360	450	mA
(V_{EE} = −5.2 V)	full	II			500			500	mA
Nominal power dissipation (see Note 4)		V		1.95			1.95		W
Reference ladder dissipation		V		30			30		mW
THERMAL RESISTANCE									
Junction-to-ambient (see Note 5)		V		33			33		°C/W
Junction-to-case		V		1.2			1.2		°C/W
ACCURACY (see Note 6)									
Differential nonlinearity		I, D		0.45	0.65		0.60	0.8	LSB
	full	II			0.80			0.9	LSB
Integral nonlinearity		I, D		0.45	0.65		0.60	0.8	LSB
	full	II			0.80			0.9	LSB
Monotonicity and no missing codes	full	IV	Guaranteed over specified temperature range			Guaranteed over specified temperature range			

SPECIFICATIONS (Continued)

Electrical operating characteristics

$AV_{EE} = DV_{EE} = -5.2\,V$; $AR = +4\,V$; $R_L = 100\,\Omega$ to $-2\,V$; $T_C = 25°C$ (unless otherwise specified)

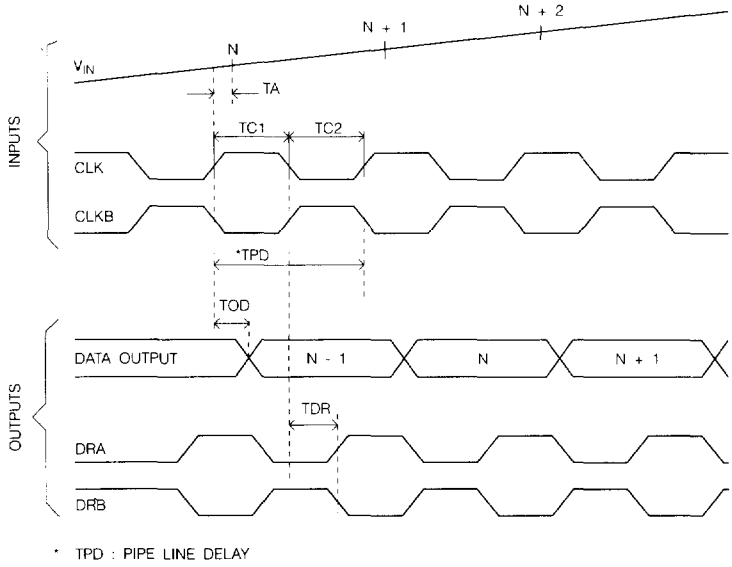
Parameter	Test level	TS 8368B Min.	TS 8368B Typ.	TS 8368B Max.	TS 8368A Min.	TS 8368A Typ.	TS 8368A Max.	Unit
DYNAMIC CHARACTERISTICS								
Signal to noise ratio (SNR)								
$F_S = 300\,MHz$ $F_{in} = 1\,MHz$	III	44.5	46.3		44.5	46.3		dB
$F_S = 250\,MHz$ $F_{in} = 10\,MHz$	III	43.9	45.7		43.9	45.7		dB
$F_S = 250\,MHz$ $F_{in} = 50\,MHz$	III	36.7	37.8		36.7	37.8		dB
$F_S = 300\,MHz$ $F_{in} = 100\,MHz$	III	31.9	33.6		31.9	33.6		dB
$F_S = 10\,MHz$ $F_{in} = 1.5\,MHz$	D				43.9	45		dB
Total harmonic distorsion (THD)								
$F_S = 300\,MHz$ $F_{in} = 1\,MHz$	III	48	53		48	53		dB
$F_S = 250\,MHz$ $F_{in} = 10\,MHz$	III	45.5	51		45.5	51		dB
$F_S = 250\,MHz$ $F_{in} = 50\,MHz$	III	36.7	40		36.7	40		dB
$F_S = 300\,MHz$ $F_{in} = 100\,MHz$	III	35.0	37.5		35.0	37.5		dB
$F_S = 10\,MHz$ $F_{in} = 1.5\,MHz$	D				47	53		dB
Effective number of bits								
$F_S = 300\,MHz$ $F_{in} = 1\,MHz$	III	7.1	7.4		7.1	7.4		Bits
$F_S = 250\,MHz$ $F_{in} = 10\,MHz$	III	7.0	7.3		7.0	7.3		Bits
$F_S = 250\,MHz$ $F_{in} = 50\,MHz$	III	5.8	6.0		5.8	6.0		Bits
$F_S = 300\,MHz$ $F_{in} = 100\,MHz$	III	5.0	5.3		5.0	5.3		Bits
$F_S = 10\,MHz$ $F_{in} = 1.5\,MHz$	D				7.0	7.2		Bits

Note 1 : With $I_{OUT} = 2\,mA$.
Note 2 : With $I_{OUT} = 12\,mA$.
Note 3 : See definition of terms.
Note 4 : With $AR = 4\,V - AV_{EE} = DV_{EE} = -5.2\,V$ $F_S = 10\,MHz$ $F_{in} = 1.5\,MHz$.
Note 5 : 33°C/W on glass expoxy board or 18°C/W on ceramic board.
Note 6 : Histogram based on sampling of 1.5 MHz sinusoidal analog signal with and encode rate of 10 MHz.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested.
II	100 % production tested at +25°C, and sample tested at specified temperature
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at $T_{amb} = +25°C$ (based on A version only).

TIMING DIAGRAM



* TPD : PIPE LINE DELAY

Figure 1

SWITCHING PERFORMANCES (see Notes 1 and 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
TC1	Minimum clock pulse width (high)		1.5		ns
TC2	Minimum clock pulse width (low)		1.5		ns
TA	Aperture delay		0.4		ns
	Aperture uncertainty (see Note 1)		3		ps
TOD	Ouput delay		3.5		ns
TDR	Data ready output delay		3.5		ns
	Output rise time (see Note 3)		2		ns
	Output fall time (see Note 3)		2		ns

Note 1 : See definitions of terms.

Note 2 : $AV_{EE} = DV_{EE} = -5.2\,V$; $AR = +4\,V$; $+V_{REF} = 0\,V$; $-V_{REF} = -2\,V$.

Note 3 : Ouputs terminated through 100 Ω to $-2\,V$. $C_{load} < 10\,pF$.
Clock command rise/fall time should be less than 1.5 ns for normal operation.

FUNCTIONAL BLOCK DIAGRAM

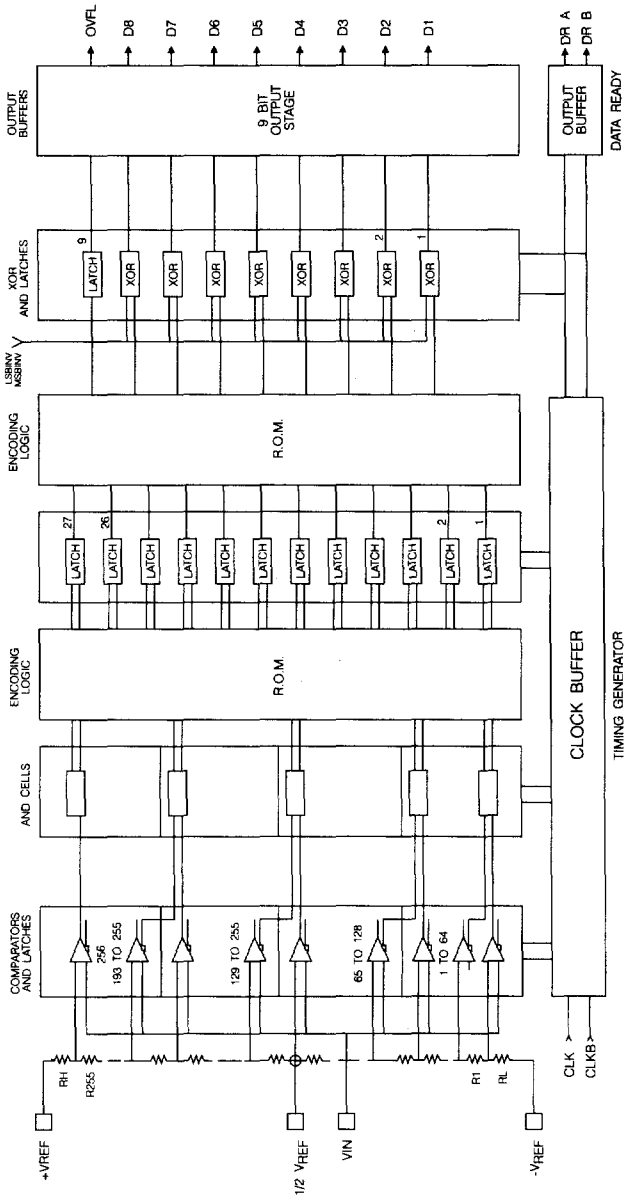


Figure 2

PIN DESCRIPTION

Pin	Name	Function
3, 33, 38, 63	A_{GND}	Ground connection, analog section
4, 32, 40, 64	AV_{EE}	Negative supply voltage, analog section
6, 66	AR	Analog return, normally grounded
60	CLK	Non inverted input of clock command
59	CLKB	Inverted input of clock command
51, 50, 49, 48, 47, 46, 45, 44	D1-D8	Digital data output (ECL)
41, 42, 52, 53	DGND	Ground connection, digital section
5, 39, 54, 65	DV_{EE}	Negative supply voltage, digital section
36	DRA	Data ready output signal (ECL)
35	DRB	Inverted data ready output signal (ECL)
43	O_{VFL}	Overflow data output signal (ECL)
10	LSB_{INV}	LSB invert input command (D1-D7) (see Note 1)
11	MSB_{INV}	MSB invert input command (D8) (see Note 2)
9	O_{VINH}	Overflow inhibit input command (see Note 3)
1	V_{IN}	Analog input, normally between 0 and − 2 V
57	$-V_{REF}$	Negative reference voltage
56	$-V_{REFS}$	Negative reference voltage sense
67	1/2 V_{REF}	Midscale V_{REF}, normally floating
13	$+V_{REF}$	Positive voltage reference
14	$+V_{REFS}$	Positive reference voltage sense
2, 7, 8, 12, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 34, 37, 55, 58	NC	Not connected

Note 1 : When grounded, low-order output bits are inverted. No inversion when tied at V_{EE} or floating.

Note 2 : When grounded, MSB is inverted. No inversion when tied at V_{EE} or floating.

Note 3 : When connected to ground, the overflow bit is inhibited and the nonreturn to-zero operation is actived. When tied to V_{EE} (or floating), overflow bit O_{VFL} = HIGH and output bits = LOW when the analog input voltage exceed + V_{REFS}.

TRUTH TABLE

MSB_{INV}	LSB_{INV}	Output coding
L	L	True binary
H	H	Inverted binary
H	L	Two's complement
L	H	Inverted two's complement

THEORY OF OPERATION

The block diagram (see page 6) shows a conventional flash converter structure having one comparator per state. This architecture enables very high-speed operation, without external sample and hold.

The analog input signal is fed to all comparators, and is compared to a set of 256 reference levels (8 bits + overflow), derived from a resistor ladder network. Midpoint tap (1/2 V_{REF}) of the reference ladder is provided for linearity adjustment or transfer function modification. When not being used, a decoupling capacitor of 100 nF connected to AGND is recommended to minimize high frequency noise injection.

A set of 256 AND latches following the comparator array indicates the appropriate quantization level of the analog input signal. Two encoder stages (R.O.M.) followed by master-slave latches provide synchronized output data in binary code.

High-speed output ECL buffers using active pulldown current sources, makes it possible to drive high capacitive loads (up to 10 pF) at maximum data rate without the need of external buffers.
A Data Ready circuit delivers output strobe signals, which track internal propagation delay, and facilitate in output data acquisition.

APPLICATIONS

Functional description

The TS 8368 operates for input analog signals varying between $\pm V_{REF}$ reference voltages, (Nominally $+V_{REF} = 0$ V, $-V_{REF} = -2$ V), applied accross internal resistor ladder.
Maximum differential Reference voltage is 2.1V, so external reference generator circuit must limit the voltage to this value, to avoid permanent damage caused to the TS 8368 by excessive current densities.
The offset errors caused by input $\pm V_{REF}$ access resistances, can be cancelled using voltage sense lines ($\pm V_{REFS}$ control pins). (Maximum sense current : 500 μA).

The typical input capacitance of the TS 8368 is 20 pF, which needs simple buffering requirements, or can be directly driven by most 50 Ω signal sources.
When Analog Return (AR) supply pin is grounded, the input capacitance is dependent on the analog input voltage, which causes distorsion.
If the (AR) supply pin is connected to a positive dc supply voltage, (between 0 V (Ground) and +5 V), input capacitance variation is lowered, and dynamic performances of the TS 8368 are improved.

Differential input ECL clock signals are recommended for the TS 8368, to reduce jitter and thus improve output noise floor.
Fast clock transition times (< 500 ps, 300 ps recommended), are required when digitizing high-frequency input waveforms.

The differential Data Ready (DRA, DRB), signals track the internal propagation delay of output Data (typically 3.5 ns).
This enables easy external clock generation for output data acquisition over full temperature range.
Internal output ECL buffers were designed for driving heavy capacitive loads (up to 10 pF) at maximum data rates.

Output data format can be determined by two control pins :
LSB_{INV}, which allows to invert the seven least significant bits.
MSB_{INV}, which allows the most significant bit to be inverted.
Selection among True/Inverted Binary and True/Inverted Two's Complement output coding is handled by proper setting of LSB_{INV} and MSB_{INV} control pins. (See TS 8368 Truth Table).

The OVINH (Overflow Inhibit) control pin handles output RZ (Return to Zero), or NRZ (Non Return to Zero) feature in overflow conditions.
When OVINH is connected to V_{EE} or allowed to float, and $V_{IN} > +V_{REFS}$ sense voltage, overflow bit turns to ECL logic 1, and output bits to ECL logic 0.
For Normal operation, (i.e. True Binary, Return to Zero), the LSB_{INV}, MSB_{INV} and OV_{INH} control pins are to be connected to V_{EE} (or allowed to float).

Timing

Output Data change on rising edge of clok signal, (Comparators in latch mode), after Tod (Typ = 3.5 ns) output propagation delay. (Pipeline delay is one clock cycle).
Output Data should be latched on rising edge of Data Ready signal (DRA), corresponding to falling edge of Clock input command.

Application board layout and power supplies recommendations

Multilayer printed circuit board is recommended, because it enables compact implementation, and allows easy desing of low impedance continuous Supply and Ground planes.
Digital input/output signal paths length should be matched and kept short, to avoid propagation delay mismatches, and minimize output bits time skew, and reflections.
So long as propagation delay along the line is shorter than digital signal rise or fall time, the reflection has little effect on the waveform.
If long interconnection lengths cannot be avoided, proper desing of transmission line impedance with adapted ECL termination loads has to be observed.
It is important to retain separate supply planes for Analog and Digital V_{EE}. Proper Supply decoupling by high resonant frequency chip capacitor near the circuit, and high quality tantalum capacitor at each power supply incoming, is especially recommended.

Packaging

The top of the LCCC 68 Package (Heat spreader) is internally connected to V_{EE} (Device substrate).
A seal ring is internally connected to ground, which reduces internal coupling and thus improves output noise floor.
Sockets may be used for prototype evaluation, but should be avoided after-wards, because of possible limitations of TS 8368 dynamic performance.

TYPICAL EVALUATION CIRCUIT

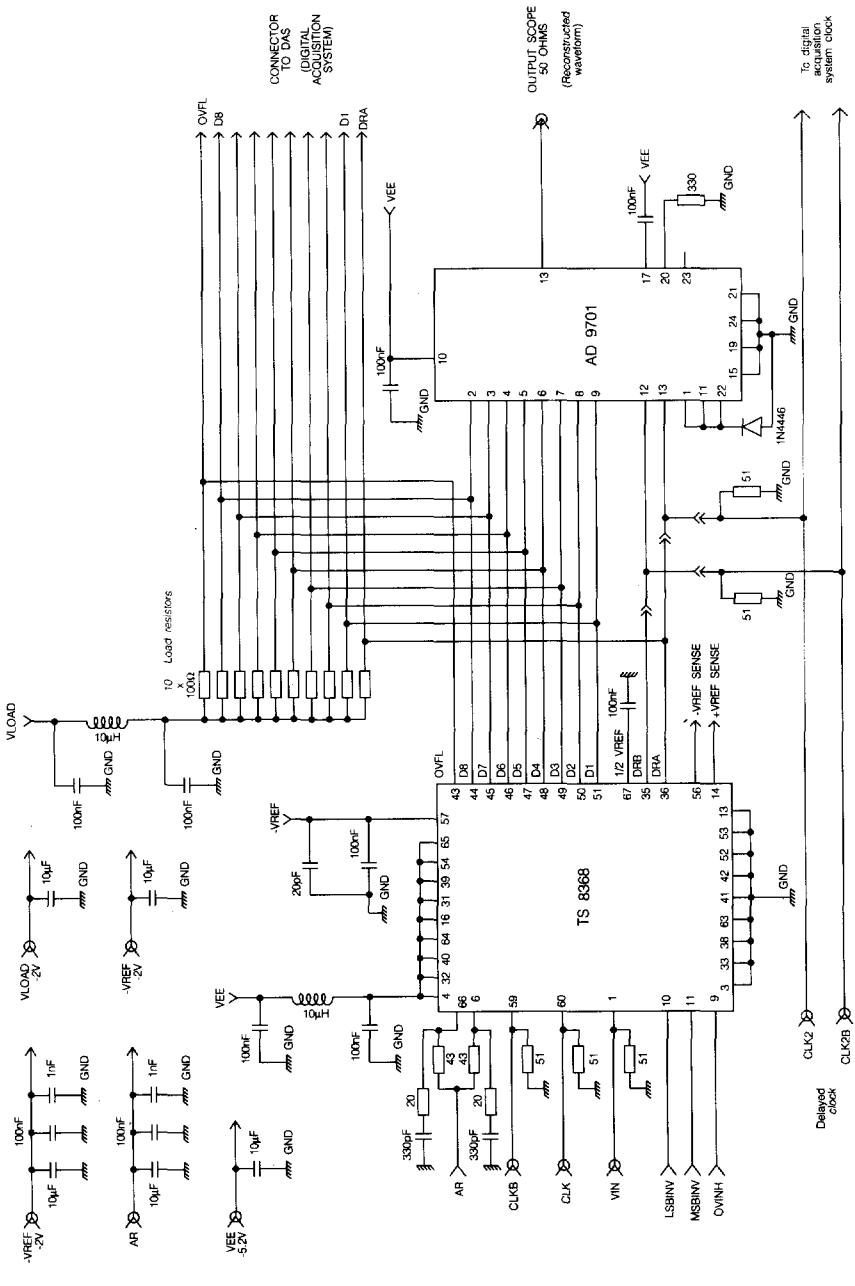


Figure 3

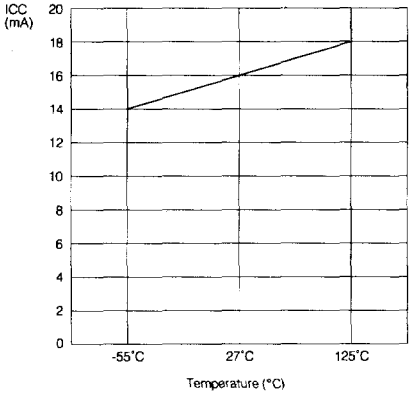


Figure 4 : I_{CC} vs. temperature.

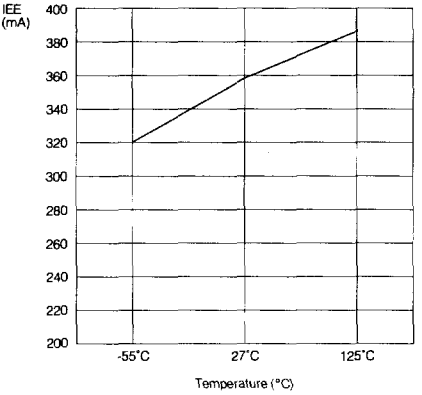


Figure 5 : I_{EE} vs. temperature.

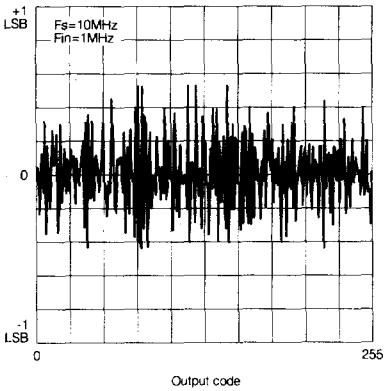


Figure 6 : Differential non linearity.

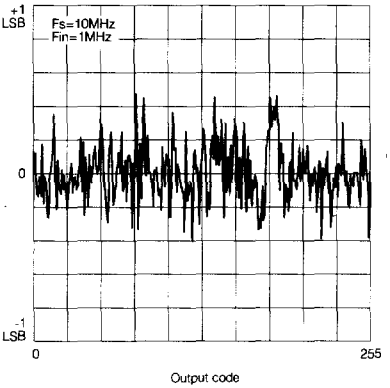


Figure 7 : Integral non linearity.

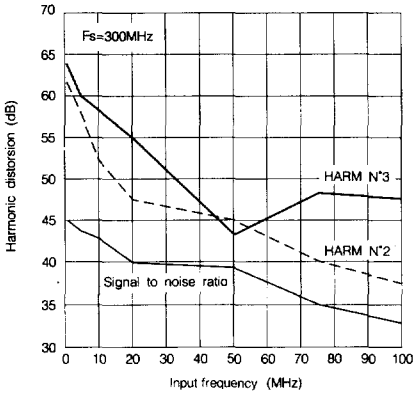


Figure 8 : SNR, distorsion 2nd and 3rd harmonics vs. input frequency.

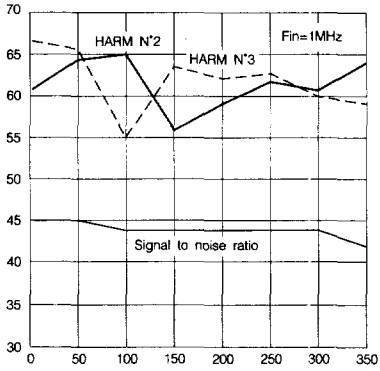


Figure 9 : SNR, distorsion 2nd and 3rd harmonics vs. sampling rate.

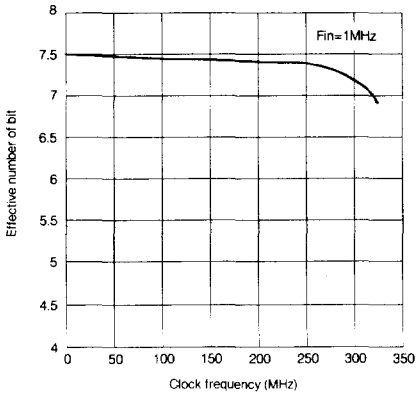


Figure 10 : Number of effective bits vs. sampling rate.

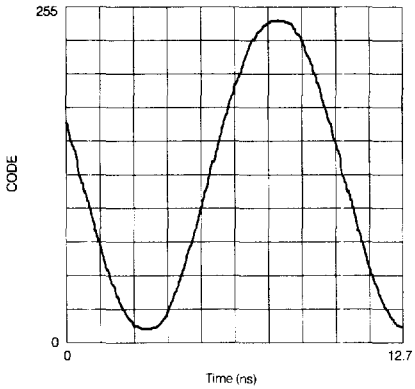


Figure 11 : Reconstructed waveform 200 MHz sampling rate, 100 MHz input frequency.

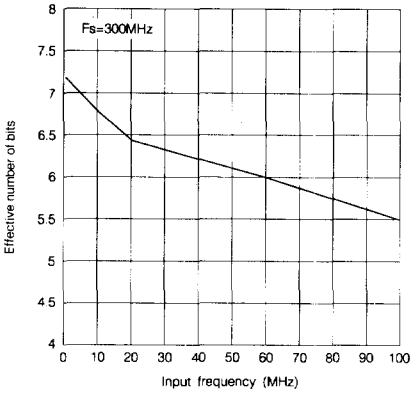


Figure 12 : Number of effective bits vs. input frequency.

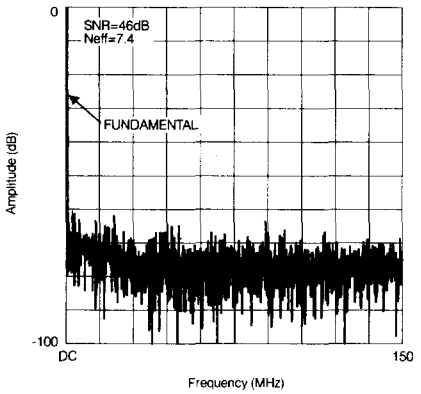


Figure 13 : FFT of TS 8368 output at 300 MHz sampling rate, 1 MHz input frequency.

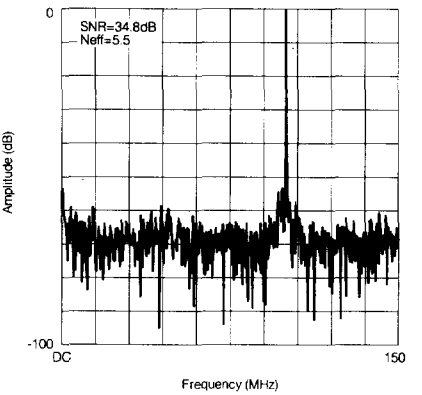


Figure 14 : FFT of TS 8368 output at 300 MHz sampling rate, 100 MHz input frequency.

DEFINITION OF TERMS

Signal-to-noise ratio (SNR)

Determined by FFT analysis,

$$SNR = 10 . \log \left[\frac{P(F_{IN})}{P_n}\right] = 10 . \log \left[\frac{A^2(F_{IN})}{\Sigma A^2(j)\, j \neq F_{in}}\right]$$

with :

- *P (FIN) spectral power of the input frequency* F_{IN}.
- P_n noise power, which is defined as the sum of the powers of all spectral components, except F_{IN}.
- A (j) amplitude of the spectral component of frequency j.

Total harmonic distorsion (THD)

Determined by FFT analysis,

$$THD = 10 . \log \left[\frac{P(F_{IN})}{P_{hm}}\right] = 10 . \log \left[\frac{A^2(F_{IN})}{\Sigma A^2(k.F_{IN})}\right] \text{ with } k \geqslant 2$$

with : P_{hm} harmonic noise power, which is defined as the sum of the powers of au harmonics of F_{IN}.

Number of effective bits (N_{eff})

Determined by FFT analysis,

$$N_{eff} = \frac{SNR - 1.76}{6.02}$$

Gain error (G_e)

$$G_e = \frac{G - G_O}{G_O}$$

with :

- G_O slope of theoretical straight line of the ADC transfer function.
- G slope of the real best-fit straight line.

Integral nonlinearity (INL)

Measured after trimming the offset and gain errors to zero.

The integral nonlinearity for an output code i, INL(i), is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.

The ADC integral nonlinearity INL is the maximum value of all |INL(i)|.

Differential nonlinearity (DNL)

Measured after trimming the offset and gain errors to zero.

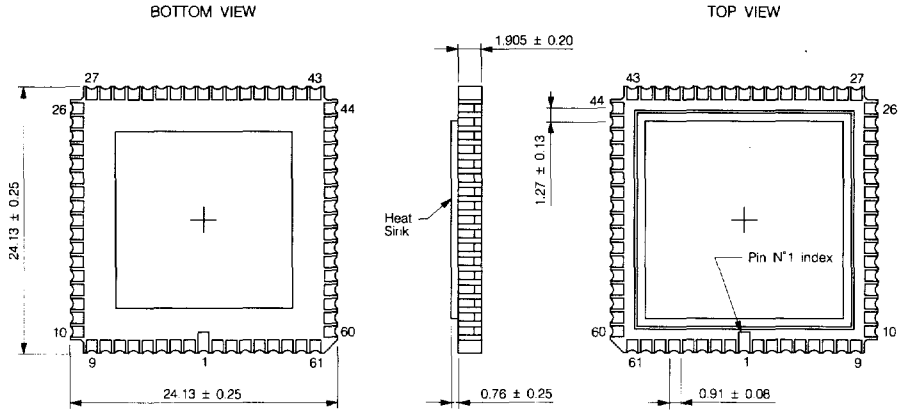
The differential nonlinearity for an output code i, DNL(i), is the difference between the measured step size of code i and the ideal ISB step size.

The ADC differential nonlinearity DNL is the maximum value of all |DNL(i)|.

OUTLINE DIMENSIONS

Leadless Ceramic Chip Carrier (LCCC) - Suffix E

Dimensions in mm



DIE MECHANICAL INFORMATION : JTS 8368

Pad layout : V594

Pad size : 0.120 x 0.120 mm

Die size : 4.180 x 5.080 mm

Die thickness : 380 μm

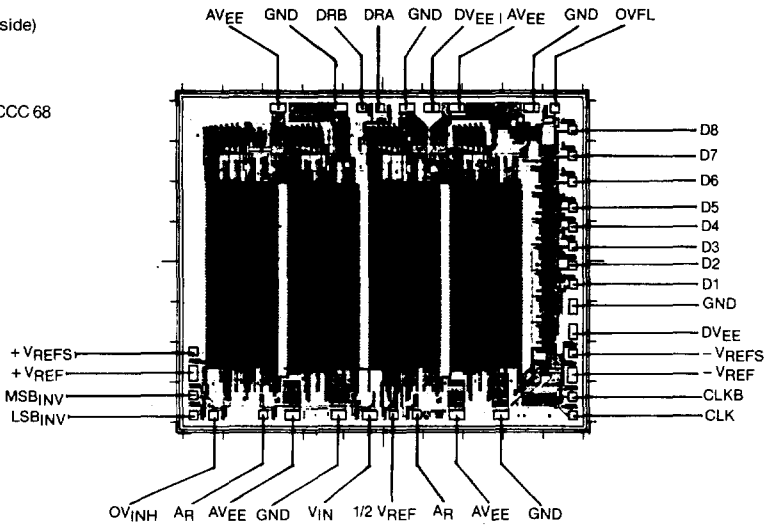
Metallization : Si (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

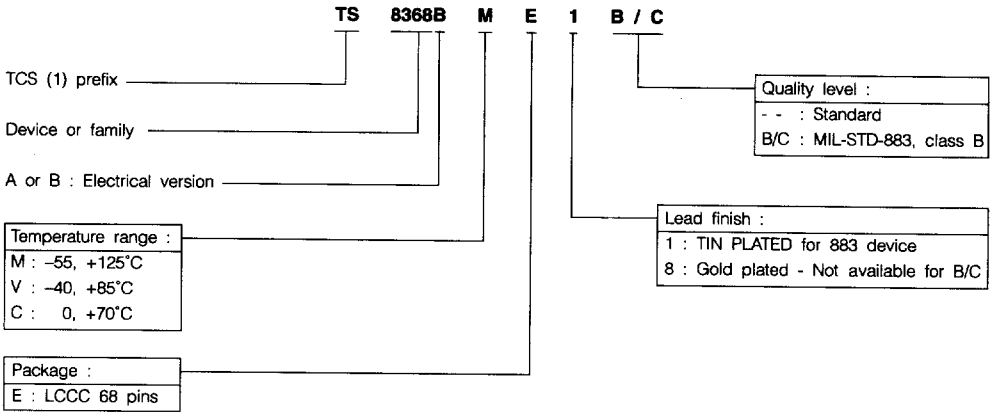
Qualification lot package : LCCC 68

Back side potential : AV_{EE}

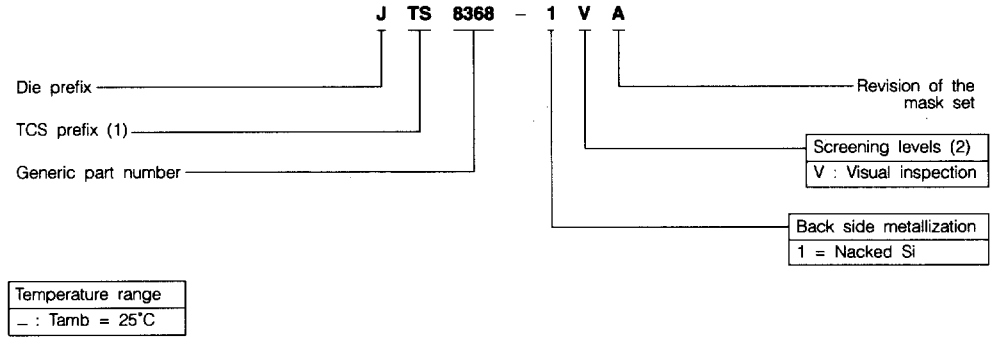


ORDERING INFORMATION

Packaged device



Die form



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : For availability of the different available versions contact your TCS sales office.