Medical Series CompactFlash® Card

FEATURES

- Storage Capacities:
  - 128MB, 256MB, 512MB,1GB, 2GB, 4GB and 8GB
- Environment conditions:
  - Operating temperature: -40°C to 85°C
  - Storage temperature: -55°C to 125°C
- CompactFlash® Compatibility
  - CFA standard 2.1 compliant
  - 3.3V or 5.0V single power supply
  - 50 pin connector with Type-I form factor (3.3mm thickness)
  - 256 Bytes of attribute memory
- Power consumption
  - 5V operation

    Active mode:

    Write operation: 28 mA (Typ.), 30 mA (Max.)

    Read operation: 23 mA (Typ.), 30 mA (Max.)

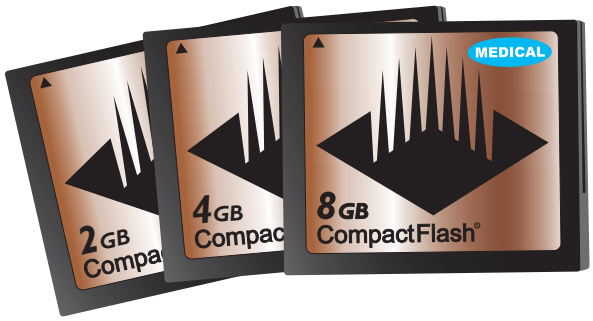
    Sleep mode: 2.0mA (max.)
  - 3.3V operation

    Active mode:

    Write operation: 28 mA (Typ.), 30 mA (Max.)

    Read operation: 23 mA (Typ.), 30 mA (Max.)

    Sleep mode: 2.0mA (max.
- RoHS compliant
- Interface modes
  - PC card memory mode
  - PC card I/O mode
  - True IDE mode
- Less than 1 Error in 10^{14} bits read
- MTBF > 4,000,000 hours
- High shock & vibration tolerance
- W/E Endurance: 4,000,000 write/erase cycles
- High performance
  - Interface Transfer speed in PIO mode 4 or Multi Word DMA mode 2 cycle timing; up to 16.7 MB/second (PIO mode 3 & 4 are available in IDE mode only).
  - Typical write: 5.0 MBytes/s in ATA PIO mode 4
  - Typical read: 7.0 MBytes/s in ATA PIO mode 4
  - On card ECC up to 6 Bytes per 512 Byte data



- Dimensions:
  - Type I card : 36.4mm(L) x 42.8mm(W) x 3.3mm(H)
- Highly resistant to data corruption due to power loss or card removal

DESCRIPTION

The W7NCF-H-M1 series CompactFlash® family is designed for high reliability and robust operation. This product not only offers a strictly controlled and locked bill of materials but also the robust operation which is desired in many medical applications. The product's reliability backbone is established by using a 32 bit RISC based controller along with the best SLC (single level cell) NAND flash memory devices. Utilizing proprietary techniques, our card offers both firmware and hardware features which mitigate problems relating to power disturbances and interruptions. Implemented is the industry leading ECC protection which is capable of correcting 6 bytes in every 512 byte sector. This leading ECC protection combined with patented static wear leveling technology provides the highest read/write endurance possible.

sector

ENVIRONMENTAL CHARACTERIZATION

Item	Performance
Temperature Cycle	JEDEC - JESD STD A104 Temp condition N (-40°C to 85 °C) and soak mode 3; 200 cycles
Humidity	MIL-STD 810F, Method 507.4, Paragraph 4.5.2 - 10 day test per figure 507.4-1, 10 day test
Vibration	MIL-STD 810F, Method 514.5, procedure 1, category 24, 1 hour per axis
Shock	MIL-STD 810F, Method 516.5, procedure1, non-operational, 40g, SRS functional shock for ground equipment, three (3) shock per axis (positive or negative). JEDEC- JESD22-B, 104-A, test condition B,1500 g pulse, 0.5 msec
Altitude	MIL-STD 810F, Method 500.4, procedure II, modified to 80,000 ft and non operation 1 hr test duration at altitude

PRODUCT RELIABILITY

Item	Value
MTBF (@ 25°C)	> 4,000,000 Hours
Data reliability	< 1 Non-Recoverable Error in 10^{14} Bits Read
Endurance	> 4,000,000 write/erase cycles

PRODUCT PERFORMANCE

Item	Performance (PIO mode 4 true IDE)
Read Transfer Rate (Typical)	7MB/s
Write Transfer Rate (Typical)	5MB/s
Burst Transfer Rate	up to 16.7MB/s
Controller Overhead (Command to DRQ)	1ms typical, 5ms (max)

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input LOW Voltage	-0.3	+0.8	V	
V_{IH}	Input HIGH Voltage	2.0	VCC+0.3	V	
V_{OL}	Output LOW Voltage		0.45	V	at 4mA
V_{OH}	Output HIGH Voltage	2.4		V	at 4mA
I_{CC}	Operating Current, $V_{CC\_R=5.0V}$				
	Sleep Mode		0.2	mA	
	Operating, 20 MHz		30	mA	
I_{CC}	Operating Current, $V_{CC\_R=3.3V}$				
	Sleep Mode		0.2	mA	
	Operating, 20 MHz		30	mA	
I_{LI}	Input Leakage Current		±10	µA	
I_{LO}	Output Leakage Current		±10	µA	

Attribute Memory Read and Write AC Characteristics

V_{CC} = 5V ± 0.5V, 3.3 V ±0.3V

Symbol	Parameter	Min	Max	Units
t_{cR}	Read Cycle Time	250		ns
$t_{a(A)}$	Address Access Time		250	ns
$t_{a(CE)}$	Card Enable Access Time		250	ns
$t_{a(OE)}$	Output Enable Access Time		125	ns
$t_{dis(CE)}$	Output Disable time from CE		100	ns
$t_{dis(OE)}$	Output Disable time from OE		100	ns
$t_{en(CE)}$	Output Enable time from CE	5		ns
$t_{en(OE)}$	Output Enable time from OE	5		ns
$t_{V(A)}$	Data valid time from address change	0		ns
$t_{su(A)}$	Address Setup Time	30		ns
$t_{h(A)}$	Address Hold Time	20		ns
$t_{su(CE)}$	Card Enable Setup Time	2		ns
$t_{h(CE)}$	Card Enable Hold Time	20		ns
t_{cW}	Write Cycle Time	250		ns
$t_{w(WE)}$	Write Pulse TIme	150		ns
$t_{su(A-WEH)}$	Address setup time for WE	180		ns
$t_{su(CE-WEH)}$	Card Enable setup time for WE	180		ns
$t_{su(D-WEH)}$	Data setup time for WE	80		ns
$t_{h(D)}$	Data hold time	30		ns
$t_{dis(WE)}$	Output disable time from WE			ns
$t_{en(WE)}$	Output enable time from WE	5	100	ns
$t_{su(OE-WE)}$	Output Enable setup time for WE	10		ns
$t_{h(OE-WE)}$	Output Enable hold time from WE	10		ns

Common Memory Read and Write AC Charateristics

Symbol	Parameter	Min	Max	Units
t_{cR}	Read Cycle Time	150		ns
$t_{a(A)}$	Address Access Time		150	ns
$t_{a(CE)}$	Card Enable Access Time		150	ns
$t_{a(OE)}$	Output Enable Access Time		75	ns
$t_{dis(CE)}$	Output Disable time from CE		75	ns
$t_{dis(OE)}$	Output Disable time from OE		75	ns
$t_{en(CE)}$	Output Enable time from CE	5		ns
$t_{en(OE)}$	Output Enable time from OE	5		ns
$t_{V(A)}$	Data valid time from address change	0		ns
$t_{su(A)}$	Address Setup Time	20		ns
$t_{h(A)}$	Address Hold Time	20		ns
$t_{su(CE)}$	Card Enable Setup Time	0		ns
$t_{h(CE)}$	Card Enable Hold Time	20		ns
t_{cW}	Write Cycle Time	150		ns
$t_{w(WE)}$	Write Pulse TIme	80		ns
$t_{su(A-WEH)}$	Address setup time for WE	100		ns
$t_{su(CE-WEH)}$	Card Enable setup time for WE	100		ns
$t_{su(D-WEH)}$	Data setup time for WE	50		ns
$t_{h(D)}$	Data hold time	20		ns
$t_{rec(WE)}$		20		
$t_{dis(WE)}$	Output disable time from WE			ns
$t_{en(WE)}$	Output enable time from WE	5	75	ns
$t_{su(OE-WE)}$	Output Enable setup time for WE	10		ns
$t_{h(OE-WE)}$	Output Enable hold time from WE	10		ns

I/O Access Read and Write AC Characteristic

Symbol	Parameter	Min	Max	Units
$t_{d(IORD)}$	Data Delay after IORD		100	ns
$t_{h(IORD)}$	Data Hold following IORD	0		ns
$t_{w(IORD)}$	IORD pulse width	165		ns
$t_{suA(IORD)}$	Address setup time for IORD	70		ns
$t_{hA(IORD)}$	Address hold time for IORD	20		ns
$t_{suCE(IORD)}$	Card Enable setup time for IORD	5		ns
$t_{hCE(IORD)}$	Card Enable hold time from IORD	20		ns
$t_{suREG(IORD)}$	REG setup time for IORD	5		ns
$t_{hREG(IORD)}$	REG Hold time from IORD	0		ns
$t_{dfINP(IORD)}$	INPACK delay falling from IORD	0	45	ns
$t_{drINP(IORD)}$	INPACK delay rising from IORD		45	ns
$t_{dfIO16(IORD)}$	IOIS16 delay falling from address		35	ns
$t_{drIO16(IORD)}$	IOIS16 delay rising from address		35	ns
$t_{su(IOWR)}$	Data setup time for IOWR	60		ns
$t_{h(IOWR)}$	Data hold time from IOWR	30		ns
$t_{w(IOWR)}$	IOWR pulse width	165		ns
$t_{suA(IOWR)}$	Address setup time for IOWR	70		ns
$t_{hA(IOWR)}$	Address hold time from IOWR	20		ns
$t_{suCE(IOWR)}$	Card Enable setup time fro IOWR	5		ns
$t_{hCE(IOWR)}$	Card Enable hold time from IOWR	20		ns
$t_{suREG(IOWR)}$	REG setup time for IOWR	5		ns
$t_{hREG(IOWR)}$	REG hold tme from IOWR	0		ns

True-IDE Mode I/O Access Read and Write AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{cR}	Cycle time	120		ns
t_{suA}	Address setup time for IORD/IOWR	25		ns
t_{hA}	Address hold time from IORD/IOWR	10		ns
t_{w}	IORD/IORW pulse width	70		ns
t_{rec}	IORD/IORW recovery time	25		ns
$t_{suD(IORD)}$	Data setup time for IORD	20		ns
$t_{hD(IORD)}$	Data hold time for IORD	5		ns
$t_{dis(IORD)}$	Output disable time from IORD		30	ns
$t_{suD(IOWR)}$	Data setup time for IOWR	20		ns
$t_{hD(IOWR)}$	Data hold following IOWR	10		ns

Pin Assignments & Pin Type

PC Card Memory Mode			
Pin Number	Signal Name	Pin Type	In, Out Type
1	GND		Ground
2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U
8	A10	I	IZ1
9	-OE	I	IU3
10	A09	I	I1Z
11	A08	I	I1Z
12	A07	I	I1Z
13	V_{CC}		Power
14	A06	I	I1Z
15	A05	I	I1Z
16	A04	I	I1Z
17	A03	I	I1Z
18	A02	I	I1Z
19	A01	I	I1Z
20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3
24	WP	O	OT3
25	-CD2	O	Ground
26	-CD1	O	Ground
27	D11[1]	I/O	I1Z, OZ3
28	D12[1]	I/O	I1Z, OZ3
29	D13[1]	I/O	I1Z, OZ3
30	D14[1]	I/O	I1Z, OZ3
31	D15[1]	I/O	I1Z, OZ3
32	-CE2[1]	I	I3U
33	-VS1	O	Ground
34	-IORD	I	I3U
35	-IOWR	I	I3U
36	-WE	I	I3U
37	RDY	O	OT1
38	V_{CC}		Power
39	-CSEL[4]	I	I2Z
40	-VS2	O	OPEN
41	RESET	I	I2Z
42	-WAIT	O	OT1
43	-INPACK	O	OT1
44	-REG	I	I3U
45	BVD[2]	O	OT1
46	BVD[1]	O	OT1
47	DO8[1]	I/O	I1Z, OZ3
48	DO9[1]	I/O	I1Z, OZ3
49	D10[1]	I/O	I1Z, OZ3
50	GND		Ground

PC Card I/O Mode			
Pin Number	Signal Name	Pin Type	In, Out Type
1	GND		Ground
2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U
8	A10	I	IZ1
9	-OE	I	IU3
10	A09	I	I1Z
11	A08	I	I1Z
12	A07	I	I1Z
13	V_{CC}		Power
14	A06	I	I1Z
15	A05	I	I1Z
16	A04	I	I1Z
17	A03	I	I1Z
18	A02	I	I1Z
19	A01	I	I1Z
20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3
24	-IOIS16	O	OT3
25	-CD2	O	Ground
26	-CD1	O	Ground
27	D11[1]	I/O	I1Z, OZ3
28	D12[1]	I/O	I1Z, OZ3
29	D13[1]	I/O	I1Z, OZ3
30	D14[1]	I/O	I1Z, OZ3
31	D15[1]	I/O	I1Z, OZ3
32	-CE2[1]	I	I3U
33	-VS1	O	Ground
34	-IORD	I	I3U
35	-IOWR	I	I3U
36	-WE	I	I3U
37	IREQ	O	OT1
38	V_{CC}		Power
39	-CSEL[4]	I	I2Z
40	-VS2	O	OPEN
41	RESET	I	I2Z
42	-WAIT	O	OT1
43	-INPACK	O	OT1
44	-REG	I	I3U
45	-SPKR	I/O	OT1
46	-STSCHG	I/O	OT1
47	DO8[1]	I/O	I1Z, OZ3
48	DO9[1]	I/O	I1Z, OZ3
49	D10[1]	I/O	I1Z, OZ3
50	GND		Ground

True IDE Mode			
Pin Number	Signal Name	Pin Type	In, Out Type
1	GND		Ground
2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3
7	-CS0	I	I3U
8	A10[2]	I	IZ1
9	-ATA SEL	I	IU3
10	A09[2]	I	I1Z
11	A08[2]	I	I1Z
12	A07[2]	I	I1Z
13	V_{CC}		Power
14	A06[2]	I	I1Z
15	A05[2]	I	I1Z
16	A04[2]	I	I1Z
17	A03[2]	I	I1Z
18	A02	I	I1Z
19	A01	I	I1Z
20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3
24	-IOIS16	O	ON3
25	-CD2	O	Ground
26	-CD1	O	Ground
27	D11[1]	I/O	I1Z, OZ3
28	D12[1]	I/O	I1Z, OZ3
29	D13[1]	I/O	I1Z, OZ3
30	D14[1]	I/O	I1Z, OZ3
31	D15[1]	I/O	I1Z, OZ3
32	-CS1[1]	I	I3Z
33	-VS1	O	Ground
34	-IORD	I	I3Z
35	-IOWR	I	I3Z
36	-WE[3]	I	I3U
37	IREQ	O	OZ1
38	V_{CC}		Power
39	-CSEL	I	I2U
40	-VS2	O	OPEN
41	RESET	I	I2Z
42	-IORDY	O	ON1
43	DMARQ	O	OZ1
44	-DMACK[5]	I	I3U
45	-DASP	I/O	I1U, ON1
46	PDIAG	I/O	I1U, ON1
47	DO8[1]	I/O	I1Z, OZ3
48	DO9[1]	I/O	I1Z, OZ3
49	D10[1]	I/O	I1Z, OZ3
50	GND		Ground

Note: [1] These signals are required only for 16-bit access and are not required when installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.

[2]: Should be grounded by the host system.

[3]: Should be tied to V_{CC} by the host system.

[4]: The -CSEL signal is ignored by the card in PC Card moudes. However, because it is not pulled up on the card in thses modes, it should not be left floating by the host in PC card modes. In these modes, the pin should be connected by th host to PC card A25 or grounded by the host.

[5]: If DMA operations are not used, the signal should be held high or tied to V_{CC} by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore the signal, including a floating condition.

Signal Description

Signal Name	Dir.	Pin	Description
A10-A0 (PC Card Memory Mode)	I	8, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash® Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash® Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
A10-A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode)		18, 19, 20	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
-STSCHG (PC Card I/O Mde) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states , while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio out put from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/ Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26, 25	These Card Detect pins are connected to ground on the CompactFlash® Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash® Storage Card or CF+ Card is fully inserted into its socket.
-CD1, CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Signal Description (con'd)

Signal Name	Dir.	Pin	Description
D15 - D00 (PC Card Memory Mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller . D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)	-	1, 50	Ground
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
-INPACK (PC Card Memory Mode)	O	43	This signal is the same for all modes.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash® Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash® Storage Card or CF+ Card and the CPU.
DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK-, i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re asserting DMARQ if there is more data to transfer. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash® Storage Card or CF+ Card when the card is configured to use the I/O interface.
-IORD (Tru IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

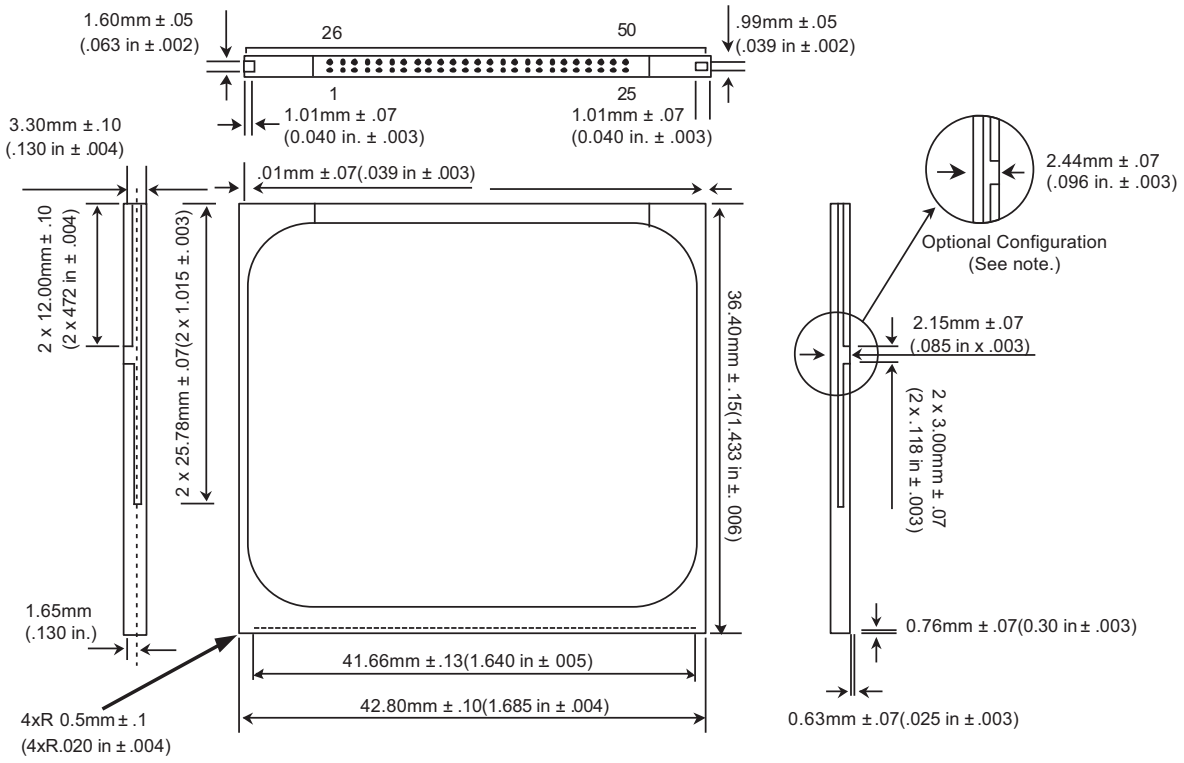
Signal Description (con'd)

Signal Name	Dir.	Pin	Description
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash® Storage Card or CF+ Card controller registers when the CompactFlash® Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash® Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash® Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash® Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash® Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
-IREQ (PC Card I/O Mode)			I/O Operation – After the CompactFlash® Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ			In True IDE Mode signal is the active high Interrupt Request to the host.
Signal Name	Dir.	Pin	Description
-REG (PC Card Memory Mode) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.

Signal Description (con'd)

Signal Name	Dir.	Pin	Description
RESET (PC Card Memory Mode)	I	41	The CompactFlash® Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash® Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	-	13, 38	+5 V, +3.3 V power.
VCC (Pc Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode)	O	33, 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash® Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.
-WAIT (PC Card Memory Mode)	O	42	The -WAIT signal is driven low by the CompactFlash® Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode)			In True IDE Mode, this output signal may be used as IORDY.
-WE (PC Card Memory Moce)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash® Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	Memory Mode – The CompactFlash® Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Model)			I/O Operation – When the CompactFlash® Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

PACKAGE DIMENSIONS



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0 in specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

Part Numbering Guide

W 7N CF xxx H x 0 x x x x x M1 x

WEDC:

Flash Card, SLC - NAND:

CompactFlash®:

Memory Capacity:
128 = 128M Byte
256 = 256M Byte
512 = 512M Byte
01G = 1G Byte
02G = 2G Byte
04G = 4G Byte
08G = 8G Byte

Controller manufacturer
H = H-Series

Controller/Firmware Revision Number:
1, 2, 3...

Labels or Custom Labeling:
0 = labels front and back
1 = label on back only

Temperature:
C = Commercial (0°C - 70°C)
I = Industrial (-40°C - +85°C)

Memory Mfg.:
S = Samsung

Memory Vendor Revsison:
Blank = Initial release
A = Susequent release etc.

Memory Device Information:

2 = 512Mbit single die package	7 = 8Gb dual die package
3 = 1Gb single die package	8 = 8Gb single die package
4 = 2Gb single die package	9 = 16Gb quad die package
5 = 4Gb dual die package	A = 16Gb dual die package
6 = 4Gb single die package	B = 16Gb single die package

Option:
B = Standard CF card configuration
A = Standard CF with conformal coating
C = Standard card with DMA disabled
D = Standard card with DMA disabled and conformal coating
E = Fixed disk option (for compatibility with some embedded software)
F = Fixed disk with conformal coating
H = Fixed with DMA disable
J = Fixed disk with DMA disable and conformal coating

Market Series:
M1 = Medical Series 1

G = for RoHS:

* For help selecting the proper and most current part number for your application please contact your local sales representative.

Document Title

128MB to 8GB Medical Series CompactFlash®

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	February 2007	Concept
Rev 1	1.0 Reviewed by enginerieng 1.1 Moved from concept to advanced	March 2007	Advanced
Rev 2	2.0 Added 1GB density to storage capacites	March 2007	Advanced