# TMC2311

## CMOS Fast Cosine Transform Processor

12 Bits, 15 Million Pixels Per Second

The TMC2311, a high-speed algorithm specific processor, computes the one or two dimensional forward discrete cosine transform (DCT) of an 8 or 8x8 point array of contiguous 9-bit data or the inverse DCT of 12-bit data. Output precision in all cases is 12 bits. It complies with the CCITT Specialists' Group on Visual Telephony (SG XV) accuracy specification for inverse DCT. With its internal coefficient ROM, data transpose RAM, address generators, and sequencer, the TMC2311 accepts high level instructions from a host processor and raw 8x8 blocked data from an external memory and returns transformed data to a second external memory. The TMC2311 also includes a defeatable adder-subtractor for linear predictive coding and differential pulse code modulation. The pipelined TMC2311 can transform continuous 8x8 pixel data blocks at a rate of one per 4.48µs.

Operating under a system clock of up to 30MHz, the TMC2311 accepts each incoming data block in row-major ("line-by-line") format at two clock cycles per pixel. Output data are written in column-major format, i.e., down the left-most column of the block, then down the next column to the right, etc., also at two clock cycles per pixel. In the inverse DCT mode, the chip accepts column-major data and return row-major data. Thus, a pair of TMC2311 chips can transform an image and return it to its original spatial domain, with or without any intervening operation, such as compression, transmission and re-expansion.

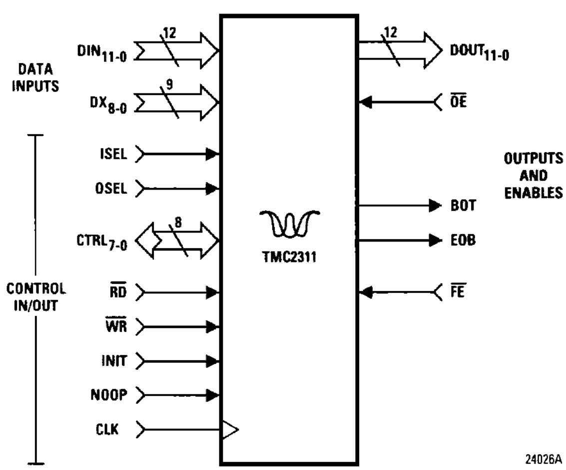
Built with TRW's one-micron double level metal OMICRON-C™ low-power CMOS process, the TMC2311 is available in a 68-lead plastic chip carrier.

## Features

- Stand Alone Execution Of 8-Point Forward Or Inverse Cosine Tranform
- Continuous 8x8-Point 2-D DCTs Every 4.48µs Including Memory Transpose And Data Loading/Unloading
- On-Chip Cosine Coefficient ROM
- On-Chip Data Transpose Memory With Direct Transpose Mode
- Auxiliary Adder With Optional Clipped Outputs For Linear Predictive Coding And Differential Pulse Code Modulation
- Two's Complement 12-Bit Data I/O Format
- Two's Complement 9-Bit Add/Subtract Input
- Full CCITT SGXV Compatibility
- All Inputs And Outputs TTL Compatible
- 68 Pin Plastic Chip Carrier

F

## Logic Symbol



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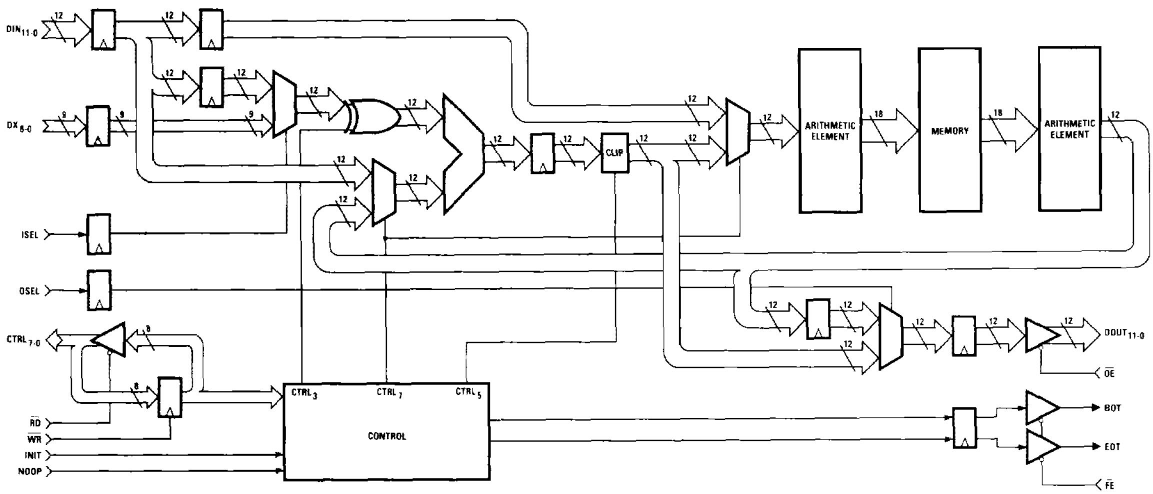
## Applications

- Image Processing, Graphics
- Pulse And Image Compression
- Video Teleconferencing
- Linear Predictive Coding
- Differential Pulse Code Modulation
- Electronic Publishing
- Medical Imaging And Archiving

## Associated Products

- TMC2312 — Quantizer/Huffman Encoder
- TMC2313 — Huffman Decoder/Dequantizer
- TMC2220 — 4x32 Correlator
- TMC2250 — 2-D 3x3 FIR Filter
- TMC2272 — Colorspace Converter

**Figure 1. Functional Block Diagram**




## Functional Description

The TMC2311 comprises five internal blocks: a controller, two arithmetic elements, a data transpose memory and an auxiliary adder circuit (*Figure 1*). Each arithmetic element (AE) can compute an 8-point 1-dimensional DCT in 16 clock cycles. When the device is configured to perform 2-dimensional transforms, the first AE computes the DCT of each consecutive row of 8 pixels. The results of each 8x1 DCT are written into the intermediate memory. After eight 1-dimensional transforms are computed, the device computes the DCT of each consecutive 8-pixel column, while (if so instructed) computing the DCTs of the rows of the next block of data. The auxiliary adder/subtractor can be used with a forward and inverse transform in linear predictive coding applications. The adder can also be used alone to perform differential pulse code modulation without the cosine transform. In all modes and configurations the device operates on continuous data at a rate of up to 15 Megapels/second and can perform a complete 8x8 DCT every 128 clock cycles.

### Control

The control block includes the chip's preprogrammed controller, sequencer, and microcode generator. The host system needs only to load a single 8-bit control word on $C_{7-0}$ and then strobe the INIT pin. The chip will proceed automatically through the chosen operation without further supervision.

### Arithmetic Element #1

Comprising a multiplier and two adder/subtractors, bypassable processor AE1 performs a series of one-dimensional 8-point forward or inverse DCTs on the incoming data, writing its 8-point transform results into the transpose memory.

### Data Transpose Memory

This two-port 64-word RAM collects each group of eight consecutive 8-point transformed data sets from AE1 and then passes them to AE2 while collecting the next group, thereby acting as a large pipeline buffer. When enabled, the DTM accepts each 64-point data block in row-major sequence and returns the same data in column-major order, effecting a "corner turn." Bypassing this block leaves the data sequence unchanged.

### Arithmetic Element #2

Identical to AE1, bypassable data processor AE2 performs eight 8- point one-dimensional transforms on each 64-point block of data. Each transform pulls one data point from each of the eight transforms done by AE1, completing the 8x8 two-dimensional transform. For one-dimensional transforms, either AE can be bypassed.

### Auxiliary Adder

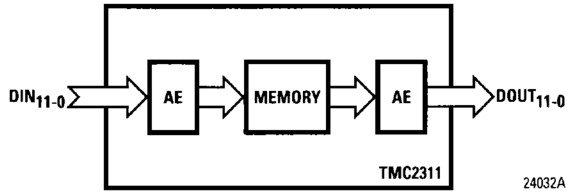
The remaining circuitry in *Figure 1* can be employed as either a presubtractor or a post-adder. (See *Applications Discussions* of *Linear Predictive Coding*, *Differential Pulse Code Modulation*, and *Interframe Coding*.) As instructed by $CTRL_3$ (INVERT), $CTRL_7$ (XSEL), ISEL, and OSEL, this adder combines the 9-bit two's complement data entering on port $DX_{8-0}$ with either the incoming or emerging data stream.

### Operating Modes

The TMC2311's five operating modes are selected by control pins $CTRL_{2-0}$. The device can be configured in the following ways:

The device will perform a two-dimensional transform if $CTRL_{2-0}$ = 000 or 001. AE1 performs a one-dimensional DCT (IDCT if $CTRL_3$ = 1) on each of eight 8-pixel rows of data supplied row-by-row to $DIN_{11-0}$. Results from each block of eight transforms are fed via the Transpose Memory to AE2, which performs a one-dimensional DCT (IDCT) on each of the eight 8-pixel columns of data, in turn (*Figure 2*).

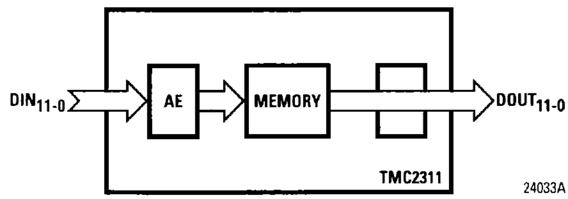
**Figure 2. 2-D Transform (With Transpose)**




The device can also perform one-dimensional DCTs (IDCTs) with or without memory transpose.

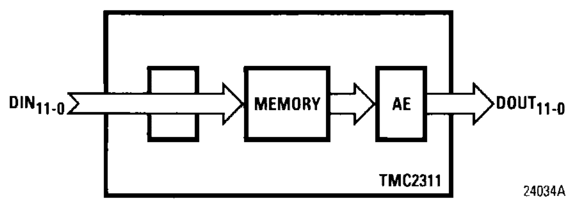
When $CTRL_{2-0}$ = 010, the chip will transform eight 8-point rows of incoming data, then transpose the results without transforming the columns (*Figure 3*).

**Figure 3. 1-D Transform With 8x8 Transpose**




When $CTRL_{2-0}$ = 011, the device accepts eight 8-point rows of data and transposes them before AE2 performs one-dimensional DCTs (IDCTs) of the columns (*Figure 4*).

**Figure 4. 8x8 Transpose With 1-D Transform**




The device can also perform one-dimensional transforms without transposes. When $CTRL_{2-0}$ = 100 or 101, AE1 performs a one-dimensional DCT or IDCT on each incoming 8-point row of data (*Figure 5*).

**Figure 5. 1-D Transform (Without Transpose)**

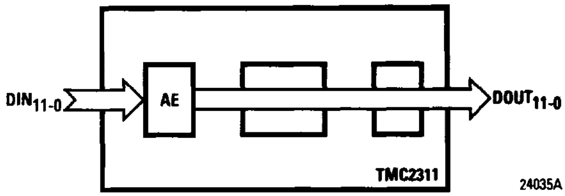
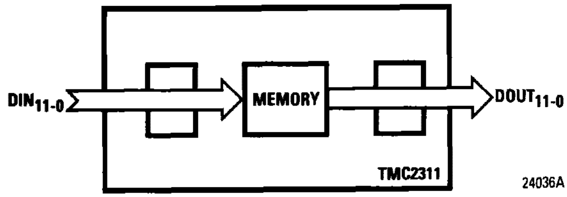



**Figure 6. Memory Transpose (Without Transform)**




Finally, the device will perform the memory transpose with no DCT when $CTRL_{2-0}$ = 110 or 111 (*Figure 6*).

*Table 1* summarizes the operation of controls $CTRL_7$, $CTRL_3$, ISEL, and OSEL, which "fine tune" the mode selection by programming the presubtractor/postadder and the transform direction. (Where a full two- dimensional FCT or IFCT is needed, $CTRL_{2-0}$ must be set to 011. $CTRL_7$=1 then enables presubtraction and OSEL=1 enables postaddition, as desired by the user.)

**Table 1. Operating Mode Configurations**

| Application | Function | Device Configuration | | | |
|---|---|---|---|---|---|
| | | $CTRL_7$ | $CTRL_3$ | ISEL | OSEL |
| 2D DCT | 2D FCT | 0 | 0 | X | 0 |
| 2D IDCT | 2D IFCT | 0 | 1 | X | 0 |
| Interframe Compress | 2D FCT, Presubtract | 1 | 0 | 0 | 0 |
| Interframe Decompress | 2D IFCT, Post Add | 0 | 1 | 0 | 1 |
| LPC | 2D FCT, Presubtract | 1 | 0 | 0 | 0 |
| ILPC | 2D IFCT, Post Add | 0 | 1 | 0 | 1 |
| LPC Directly Out | DOUT=DIN-DX | 1 | 0 | 0 | 1 |
| ILPC Directly Out | DOUT=DIN+DX | 1 | 1 | 0 | 1 |
| DPCM Directly Out | DOUT(k)=DIN(k)-DIN(k-1) | 1 | 0 | 1 | 1 |
| IDPCM Directly Out | DOUT(k)=DIN(k)+DIN(k-1) | 1 | 1 | 1 | 1 |
| DPCM w/ Transpose | DOUT(k)=DIN(k)-DIN(k-1) | 1 | 0 | 1 | 0 |
| IDPCM w/ Transpose | DOUT(k)=DIN(k)+DIN(k-1) | 1 | 1 | 1 | 0 |

Notes: LPC/ILPC Linear Predictive Coding (Forward/Inverse)
DPCM/IDPCM Differential Pulse Code Modulation (Forward/Inverse)

## Signal Definitions

### Control

**INIT** Single pass "start" command. INIT=0 resets the internal logic and output flags and updates the $CTRL_{7-0}$ parameters. INIT is registered and must be LOW for at least 3 clock cycles. INIT returning HIGH starts the transform. The first data point is loaded two cycles later.

**NOOP** Input clock disable. NOOP=1 freezes operation of the device on the next CLK rising edge. Operation commences from where it stopped one cycle after NOOP returns LOW.

**$\overline{WR}$** Control word preload command. $\overline{WR}$=0 loads CTRL7-0 parameters into the device's preload register. The next INIT rising edge transfers the preloaded parameters into the chip's working registers.

**$\overline{RD}$** Control word (READ) command. $\overline{RD}$=0 allows the preloaded parameters $CTRL_{7-0}$ to be read.

**$CTRL_{2-0}$** MODE Control. Defines the internal configuration (mode) of the device, selecting either 2-dimensional or 1-dimensional transforms and/or the access to the internal Transpose Memory (*Figures 2* through *6*.)

| $CTRL_{2-0}$ | Operation |
|---|---|
| 000 | 2–D Transform |
| 001 | 2–D Transform |
| 010 | 1–D Transform, Transpose |
| 011 | Transpose, 1–D Transform |
| 100 | 1–D Transform |
| 101 | 1–D Transform |
| 110 | Transpose |
| 111 | Transpose |

**$CTRL_3$** Inverse Transform Enable (INV). INV=0 selects a forward DCT. If INV=1, the device will compute the Inverse DCT. INV also inverts the data to one side of the auxiliary adder. When and only when INV=0, data from the multiplexer which selects the DX port or delayed DIN port will be inverted.

**$CTRL_4$** Automatic Reinitialization (AUTOINIT). AI=0 allows continuous operation of device. When AI=1, the device will halt at the end of the specified transform.

**$CTRL_5$** Arithmetic Limit (CLIP). CLIP=1 saturates data outputs to 9 bits. CLIP is useful when presubtraction or postaddition is used with the DCT or IDCT.

**$CTRL_6$** Flag Control (FC). FC determines when the output flags, BOT and EOB, appear. When FC=0, both flags are output with the corresponding data result. When FC=1, the flags appear two clock cycles earlier.

**$CTRL_7$** Auxiliary Adder Select (XSEL). XSEL controls two multiplexers within the auxiliary adder circuitry. The first mux feeds the non-inverted input to the adder either the DIN port (XSEL=1) or outputs from the core of the device (XSEL=0). The second mux selects the data entering the core of the device from either the input port (XSEL=0) or adder output (XSEL=1). See *Applications, Operating Mode Configurations*.

**ISEL** Input Data Select. ISEL=0 connects the inverted (optional) input of the auxiliary adder to the DX port. When ISEL=1, the DIN port is connected, via a one data cycle delay. Output from this mux to the adder is inverted when INV=0. See *Applications, Operating Mode Configurations*.

**OSEL** Output Data Select. When OSEL=0, data results from the device core pass to the final output register. When OSEL=1, results from the adder pass to the final output register. See *Applications, Operating Mode Configurations*.

**$\overline{OE}$** Asynchronous active LOW OUTPUT ENABLE for data output port, $DOUT_{11-0}$. When $\overline{OE}$=1, every output is forced into a high-impedance state.

**$\overline{FE}$** Active LOW asynchronous output FLAG ENABLE. When $\overline{FE}$=1, BOT and EOB are forced into a high-impedance state.

### Data Inputs

$DIN_{11-0}$ Data INput Port (12-bit two's complement format). DIN is the input port for both FORWARD and INVERSE transforms. DIN11 is the MSB. For two dimensional forward transforms, data precision is limited to 9 bits, $DIN_{8-0}$, and must be sign-extended into the remaining MSBs. Data exceeding the lower 9-bit range may cause an internal overflow. For INVERSE transforms, the entire 12-bit input port may used without risk of overflow.

$DX_{8-0}$ Auxiliary Data Input Port (9-bit two's complement format). Feeds one side of auxiliary adder. $DX_8$ is the MSB. Auxiliary inputs can be provided to the device for linear predictive coding (LPC) where pixel differences are transformed. In the FORWARD direction, inputs supplied to the DX port (and selected via ISEL) will be subtracted from pixel values input simultaneously on the DIN port. In the INVERSE direction, DX inputs will be added to outputs following the desired tranform operation. The DX inputs must be delayed so that they appear at the adder simultaneously with the corresponding pixel outputs.

### Data Outputs

$DOUT_{11-0}$ Data OUTput Port (12-bit, two's complement format). DOUT is the output port for both FORWARD and INVERSE transforms. $DOUT_{11}$ is the MSB. When CLIP=1, all data outputs are clipped to 9 bits, $DOUT_{8-0}$, with sign extension into the remaining MSBs. DOUT is forced into a high-impedance state when $\overline{OE}$=1.

### Output Flags

BOT Beginning Of Transform. Toggles LOW to denote the first result of each one-dimensional 8-point transform or the first result of each 8-point row or column of a two-dimensional transform. When FC=0, BOT will appear simultaneously with the corresponding result. When FC=1, BOT will appear one data I/O cycle earlier.

EOB End Of Block. Toggles LOW to signal the last result of the entire (8 or 64 point) transform field. When FC=0, EOB appears simultaneously with the last data result. When FC=1, EOB appears two cycles earlier.

### Clock

CLK Data Path Clock. The device operates with a clock of 0 to 30MHz. All internal operations are referenced to the rising edges of CLK; I/O operations except $CTRL_{7-0}$ read and write, to alternate rising edges of CLK.

### Power

$V_{DD}$, GND The TMC2311 operates from a single +5 Volt supply. All $V_{DD}$ and GND pins must be connected.

## Table 2. Data Formats and Bit Weighting

| | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input Data Format – Forward Transforms** | | | | | | | | | | | | |
| DIN | S | S | S | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| **Input Data Format – Inverse Transforms** | | | | | | | | | | | | |
| DX: | $-2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| | | | | $-2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| | $-2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| **Output Data Format – Forward Transforms** | | | | | | | | | | | | |
| DOUT: | $-2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| **Output Data Format – Inverse Transforms** | | | | | | | | | | | | |
| | S | S | S | $-2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

Notes. S = Sign Extension.
In forward transforms, system should feed two's complement sign bit to $DIN_{11\text{-}8}$ for 9-bit data size.
In inverse transforms, chip will output two's complement sign bit into pins $DOUT_{11\text{-}8}$.

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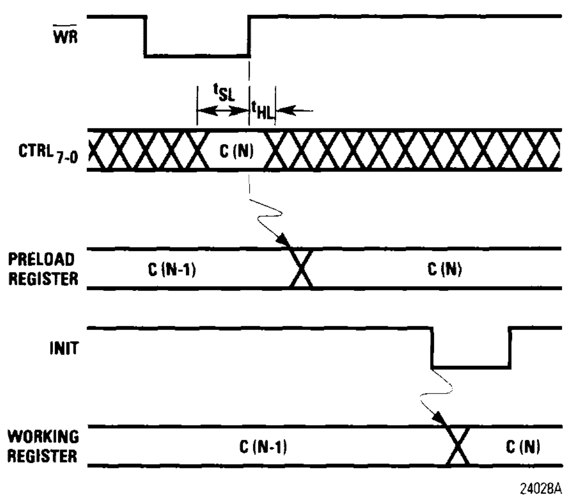
## Operation and Timing

### Initialization

### Control Word Preload Timing

The self-sequencing TMC2311 requires no cycle-to-cycle supervision by the host system. On the rising edge of $\overline{WR}$, the user loads an 8-bit control word ($CTRL_{7\text{-}0}$) which sets 5 device parameters: mode and direction of the transform, continuous (or non-continuous) device operation, format of output data and timing of the output flags. The control parameters preloaded via $CTRL_{7\text{-}0}$ are registered internally and updated by the INIT signal. Control load timing is displayed in *Figure 7*.

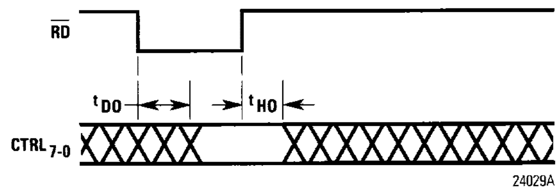
**Figure 7. Control Preload Timing**



## Control Word Read Timing

The TMC2311 also permits the user to read the preloaded control word value back through $CTRL_{7\text{-}0}$, a bidirectional port. When $\overline{RD}$=0, the $CTRL_{7\text{-}0}$ port outputs the control information stored in the device (*Figure 8*).

### Figure 8. Control Read Timing



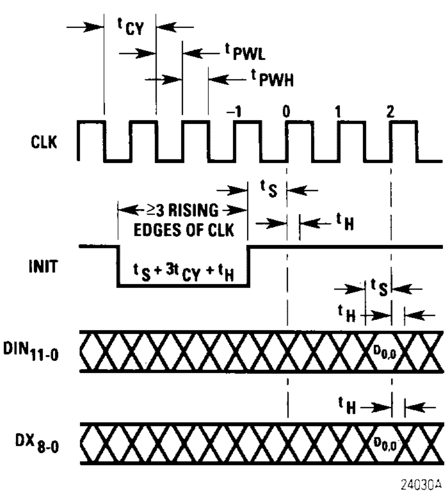

## Data Input Timing

After the TMC2311 is initialized, data are input to $DIN_{11\text{-}0}$ and $DX_{8\text{-}0}$ on alternate rising edges of the device system clock. When the device is set for forward DCTs with transpose, data inputs are accepted in row-major format, i.e., line-by-line through the 8x8 transform window. When the device performs inverse DCTs, inputs are accepted in column-major format. Following the rising edge of INIT command, data inputs can be continuously loaded into the device on alternate rising edges of the system clock (*Figure 9*).

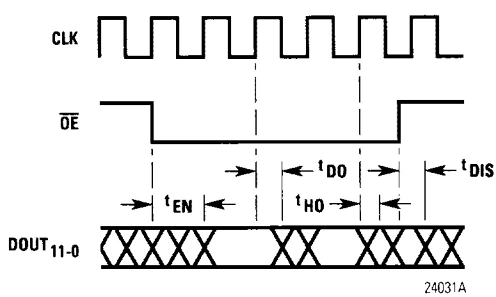
## Data Output Timing

Results are output at half the system clock rate. The initial result latency and the number of results depends on the device operation specified by $CTRL_{2\text{-}0}$. Once the first result reaches the output port, remaining results will appear continuously. When the TMC2311 is set to perform forward DCTs with transpose, output data are written in column-major format. In the inverse direction, data results are returned row-by-row (*Figure 10*).

### Figure 9. Data Input Timing




### Figure 10. Data Output Timing



## Overall Timing

The TMC2311 will expect data in groups of 8 or 64 points at regular intervals based on the mode of operation defined by $CTRL_{2-0}$. Results will be returned by the TMC2311 in similar groups following a predetermined initial latency. For applications that use the auxiliary adder ahead of the core of the device, corresponding DX and DIN inputs should be presented simultaneously to the device. Applications that use the adder after the DCT/memory core must account for the device's internal latency (*Table 3*). Each DX port input must be timed to appear at the adder one data cycle ahead of its corresponding output.

**Table 3. Data Output Latency**

| $CTRL_{2-0}$ | Operation | Latency* |
|---|---|---|
| 000 | 2-D Transform | 232 clocks |
| 001 | 2-D Transform | 232 |
| 010 | 1-D Transform, Transpose | 200 |
| 011 | Transpose, 1-D Transform | 200 |
| 100 | 1-D Transform | 56 |
| 101 | 1-D Transform | 56 |
| 110 | Transpose | 168 |
| 111 | Transpose | 168 |

*cycles after INIT goes high

If AUTOINIT ($CTRL_4$)=0, the device will operate continuously with no interruption between transforms. Otherwise the device will halt after the specified number of data points have been processed. When AUTOINIT=1, device operation will resume with the next INIT signal.

The TMC2311 also provides two output flags to differentiate between the rows/columns of the transform window and between individual transform blocks. The Beginning Of Transform (BOT) flag goes LOW with the first data result of each 8x1 transform row or column. A second flag, End Of Block, EOB, delineates transform blocks. EOB will go LOW when the last data point of each 8x1 (one dimensional mode) or 8x8 (two dimensional mode) transform is output. The user can program these flags to appear with their respective data (FC=0) or one data cycle earlier (FC=1). *Figure 11* shows the overall timing of a forward 2-D DCT with pre-subtraction and FC=0. *Figure 12* shows the overall timing of an inverse 2-D DCT with post addition and FC=1, demonstrating the timing for inputs to auxiliary port $DX_{8-0}$ and the shift in flag timing.

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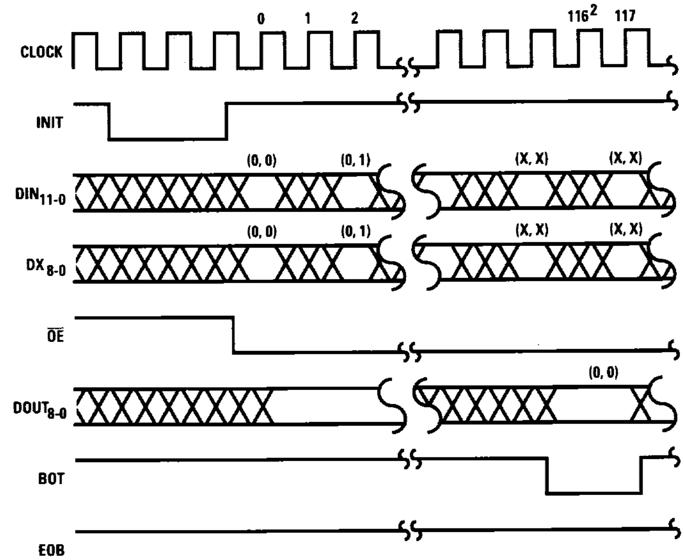
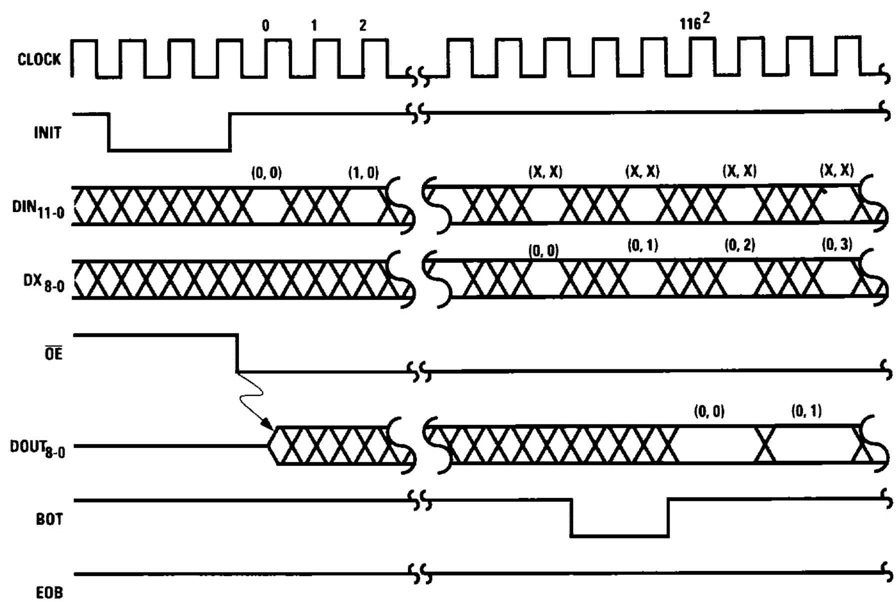
### Figure 11. Overall Timing - Forward Transform (Flag Control=0)

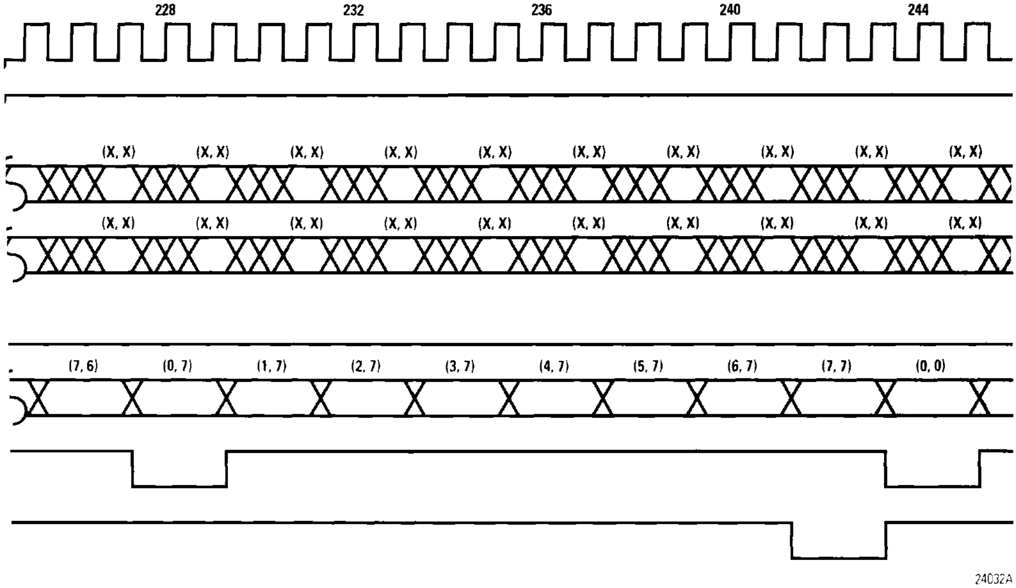



Notes: 1. $DIN_{11-0}$ (i,j) aligned with $DX_{8-0}$ (i,j), but alignment with $DOUT_{11-0}$ is mode-dependent..
2. $DOUT_{11-0}$ (0,0) is valid on CLK rising edge 116 in two-dimensional transfer modes only.

### Figure 12. Overall Timing - Inverse Transform (Flag Control=1)




Notes: 1. $DX_{8-0}$ (i,j) precedes $DOUT_{11-0}$ (i,j) by two CLK cycles, but alignment with $DIN_{11-0}$ is mode-dependent.
2. $DOUT_{11-0}$ (0,0) is valid on CLK rising edge 116 in two-dimensional transform modes only.


228
232
236
240
244
(X, X)
(7, 6)
(0, 7)
(1, 7)
(2, 7)
(3, 7)
(4, 7)
(5, 7)
(6, 7)
(7, 7)
(0, 0)
24032A

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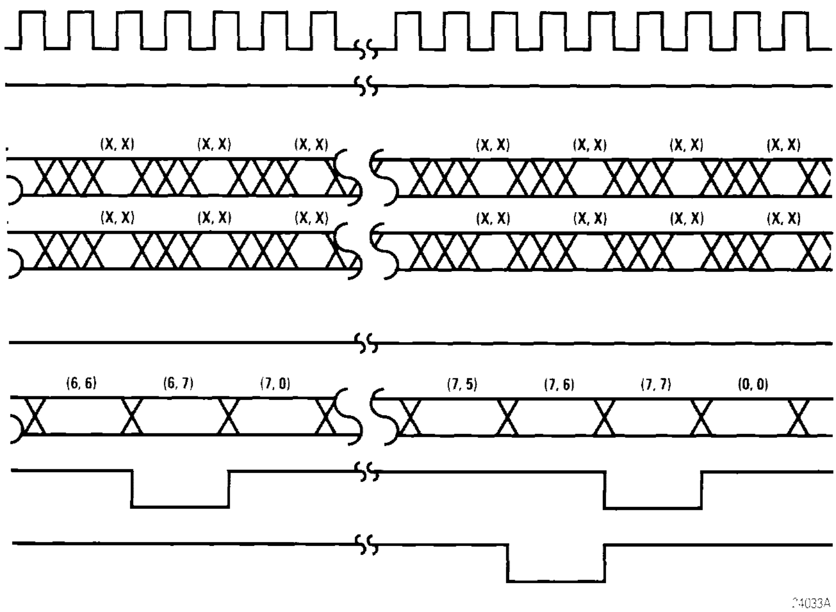

(X, X)
(6, 6)
(6, 7)
(7, 0)
(7, 5)
(7, 6)
(7, 7)
(0, 0)
24033A

## **Absolute maximum ratings** (beyond which the device may be damaged)[1]

| | |
|---|---|
| **Supply Voltage** | −0.5 to +7.0V |
| **Input Voltage**[2] | −0.5 to ($V_{DD}$ + 0.5)V |
| **Output** | |
| Applied Voltage[2] | −0.5 to ($V_{DD}$ + 0.5V) |
| Forced Current,[3,4] | −3.0 to +6.0mA |
| Short Circuit Duration (single output in HIGH state to ground) | 1 second |
| **Temperature** | |
| Operating, Case | −60 to +130°C |
| Junction | +175°C |
| Lead, Soldering (10 seconds) | +300°C |
| Storage. | −65 to +150°C |

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameter are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

## Operating conditions

| | | Temperature Range | | | |
|---|---|---|---|---|---|
| | | Standard | | | |
| **Parameter** | | **Min** | **Nom** | **Max** | **Units** |
| $V_{DD}$ | Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| $t_{CY}$ | Cycle Time | | | | |
| | TMC2311 | 37 | | | ns |
| | TMC2311-1 | 34.5 | | | ns |
| | TMC2311-2 | 28 | | | ns |
| $t_{PWL}$ | Clock Pulse Width, LOW | 8 | | | ns |
| $t_{PWH}$ | Clock Pulse Width, HIGH | 8 | | | ns |
| $t_S$ | Input Setup Time | 11 | | | ns |
| $t_H$ | Input Hold Time | 0 | | | ns |
| $V_{IL}$ | Input Voltage, Logic LOW | | | 0.8 | V |
| $V_{IH}$ | Input Voltage, Logic HIGH | 2.0 | | | V |
| $I_{OL}$ | Output Current, Logic LOW | | | 4.0 | mA |
| $I_{OH}$ | Output Current, Logic HIGH | | | −2.0 | mA |
| $T_A$ | Ambient Temperature, Still Air | 0 | | 70 | °C |
| $T_C$ | Case Temperature | | | | °C |

## Electrical characteristics within specified operating conditions[1]

| Parameter | | Test Conditions | Temperature Range Standard Min | Max | Units |
|---|---|---|---|---|---|
| $I_{DDQ}$ | Supply Current, Quiescent[2] | $V_{DD}$=Max, $V_{IN}$=0V, TS=5V | | 30 | mA |
| $I_{DDU}$ | Supply Current, Unloaded | $V_{DD}$=Max, f=30MHz, TS=5V | | 130 | mA |
| $I_{IL}$ | Input Current, Logic LOW | $V_{DD}$=Max, $V_{IN}$=0V | | −10 | µA |
| $I_{IH}$ | Input Current, Logic HIGH | $V_{DD}$=Max, $V_{IN}$=$V_{DD}$ | | +10 | µA |
| $V_{OL}$ | Output Voltage, Logic LOW | $V_{DD}$=Min, $I_{OL}$=Max | | 0.4 | V |
| $V_{OH}$ | Output Voltage, Logic HIGH | $V_{DD}$=Min, $I_{OH}$=Max | 2.4 | | V |
| $I_{OZL}$ | Hi-Z Output Leakage Current, | $V_{DD}$=Max, $V_{IN}$=0V Output LOW | | −40 | mA |
| $I_{OZH}$ | Hi-Z Output Leakage Current, | $V_{DD}$=Max, $V_{IN}$=0V Output HIGH | | +40 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{DD}$=Max, Output HIGH one pin to ground one second duration max. | | −45 | mA |
| $C_I$ | Input Capacitance | $T_A$=25°C, f=1MHz | | 10 | pF |
| $C_O$ | Output Capacitance | $T_A$=25°C, f=1MHz | | 10 | pF |

Note: 1. Actual test conditions may vary from those shown above, but guarantee operation as specified.

2. Following power-on, the TMC2311 must be clocked for at least 10 clock cycles before the clock is disabled.

F

## Switching characteristics within specified operating conditions[1]

| Parameter | | Test Conditions | Temperature Range Standard Min | Max | Units |
|---|---|---|---|---|---|
| $t_{DO}$ | Output Delay | $V_{DD}$=Min, $C_{Load}$=40pF | | 16 | ns |
| | TMC2311 | | | 16 | |
| | TMC2311-1 | | | 16 | |
| | TMC2311-2 | | | 12 | |
| $t_{HO}$ | Output Hold Time | $V_{DD}$=Max, $C_{Load}$=40pF | 4 | | ns |
| $t_{ENA}$ | Three-State Output Enable Delay | $V_{DD}$=Min, $C_{Load}$=40pF | | 16 | ns |
| | TMC2311 | | | 16 | |
| | TMC2311-1 | | | 16 | |
| | TMC2311-2 | | | 12 | |
| $t_{DIS}$ | Three-State Output Disable Delay | $V_{DD}$=Min, $C_{Load}$=40pF | | 22 | ns |

Note: 1. All transitions except for $t_{DIS}$ and $t_{ENA}$ are measured at a 1.5V level.

Figure 13. Equivalent Input Circuit

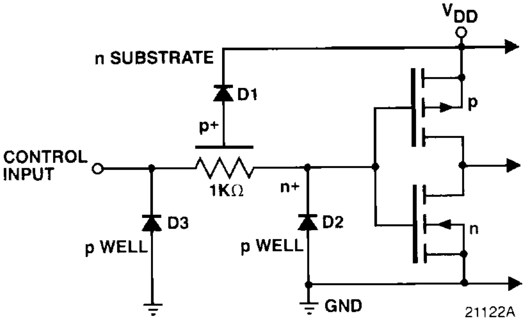
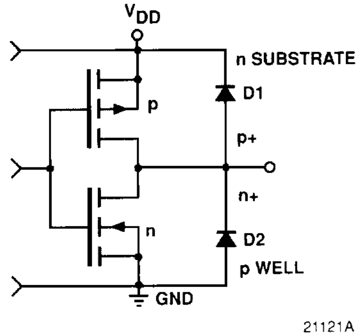



Figure 14. Equivalent Output Circuit




## Applications Discussions

### Frequency Domain Coding - Basic System

Frequency domain coding entails partitioning an image into (for example) 8x8 pixel blocks, then determining the two-dimensional spatial frequency spectrum of each block. In image compression, each component is then quantized by a frequency-specific factor, which tends to be smaller (more precise) for the dominant lower- frequency components and larger (coarser) for the less crucial higher-frequency components. Quantization effects compression by reducing the number of bits per frequency bin and by zeroing out high-frequency, low-energy bins. Following the quantizer, the scaled frequency data are then (arithmetic or Huffman) coded into a format that will allow them to be transmitted (or archived) even more economically. In particular, the JPEG modified Huffman coding represents each string of "zeroed out" bins with a compact code.

The transmitted images are reconstructed by reversing these operations. Coded information is received and restored to frequency information through a decoder. The received (or retrieved) data then pass through an inverse quantizer that restores the most important frequency components, albeit at somewhat grainier than original levels. Finally, the image is reconstructed by the inverse DCT. In practice, compression ratios of up to 20:1 can provide visually acceptable results with still images.

The basic compression circuit (*Figure 15*) shows a sample implementation of an intraframe compressor. The system contains an encoder comprising the TMC2311 DCT chip, a quantizer and a coder. Images are reconstructed in a complementary system with a decoder, a dequantizer, and a TMC2311 (inverse) DCT chip.

Figure 15. Basic System

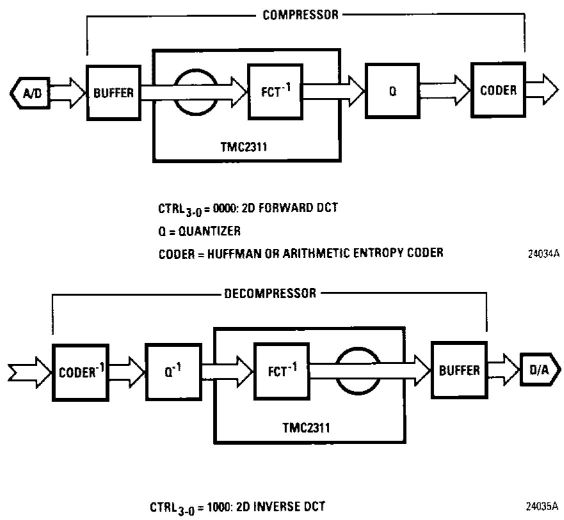
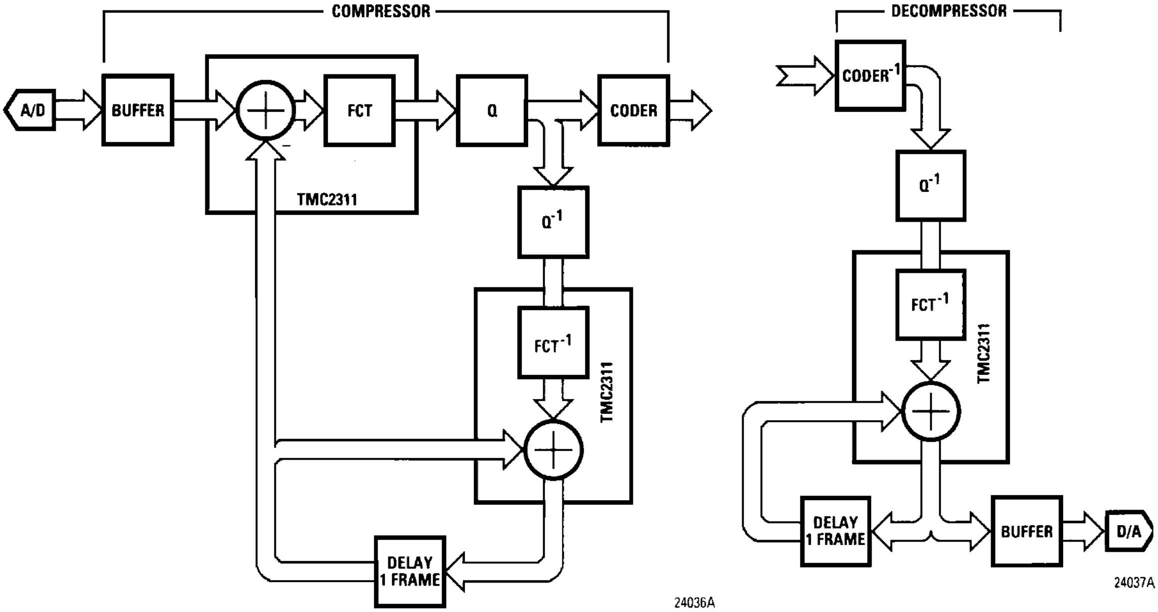


**Figure 16. Interframe Compression System**




## Interframe Compression

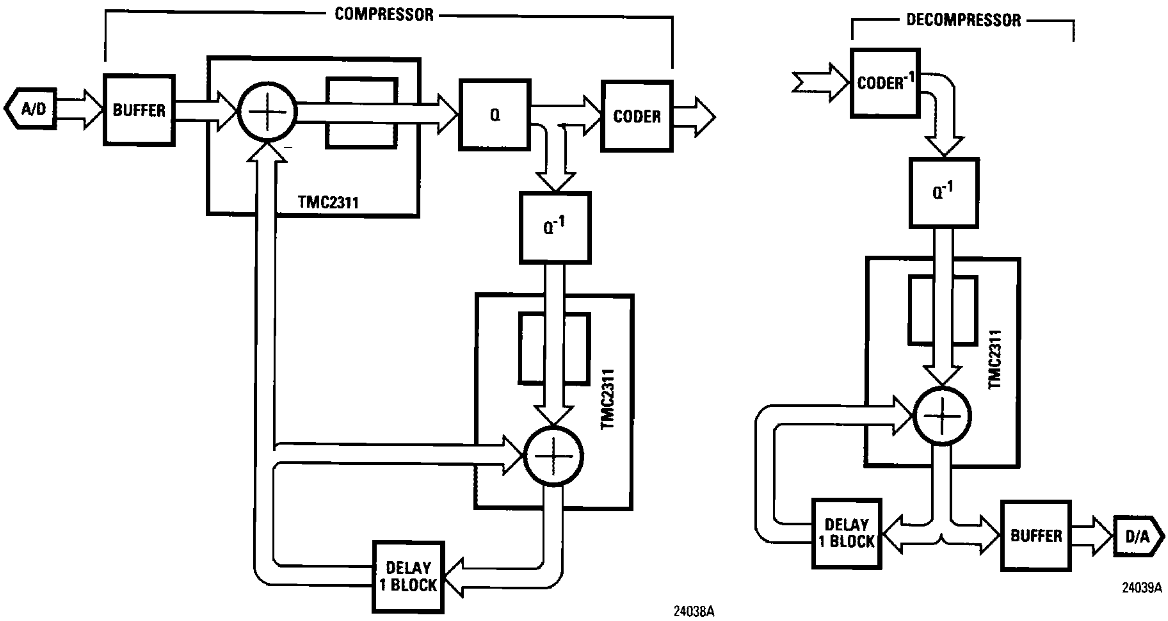
*Figure 16* shows a moving picture extension of frequency domain coding, which processes differences between the corresponding pixels of successive image frames. Interframe compression describes areas of change within a moving image by comparing each new frame against earlier frames. Prior to the DCT, a block from the new frame is subtracted from the corresponding block of the previous frame. The resulting differences are transformed, quantized, coded, and transmitted. The compressed data are then reconstructed by reversing the processing steps: decode, dequantize, inverse DCT, then accumulate differences from frame to frame. Transforming only these differences increases the achievable compression.

## Linear Predictive Coding System

Many critical biomedical and defense applications require that images be compressed and then restored "losslessly," i.e., without degradation. One technique, referred to as Linear Predictive Coding (LPC), has been very effective in speech compression. For image compression, LPC entails coding the differences between the current and previous pixel blocks of the same frame. This technique of intraframe compression can be used with or without the DCT. Much of the *Figure 16* interframe compression architecture can also be applied here, although the delay block now corresponds to delay within a single frame.

To obtain lossless compression, the user may code the differences between pixel blocks directly, without the DCT. This variety of intraframe compression, demonstrated in *Figure 17*, uses just the auxiliary adder of the TMC2311. In the forward direction, the differences are computed and transferred to the quantizer and coder circuitry where they are readied for transmission. In the inverse direction, the reconstruction process involves inverse coding and quantization, followed by cumulative addition of the image differences by the TMC2311's auxiliary adder.

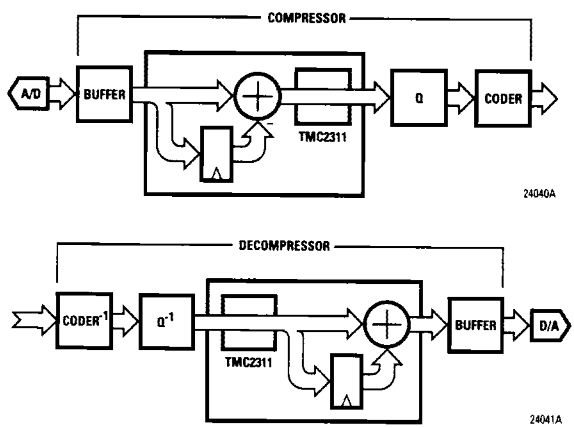
Figure 17. Linear Predictive Coding System (No Cosine Transform)




## Differential Pulse Code Modulation

Another linear prediction algorithm, differential pulse code modulation, (DPCM) uses the differences between individual pixels on each line of the image. These differences are quantized, coded and transmitted (or archived). This technique is also used where lossless compression is required. The system shown in *Figure 18* illustrates the use of the auxiliary adder circuit of the TMC2311. The device incorporates a special input delay path that allows a previous pixel value to be added or subtracted from the current input pixel value. The results are then either fed into the device core to perform a transpose function or output directly from the adder. In the forward direction the pixel differences are fed to the quantizer and coder blocks of the system and transmitted. In the inverse direction the coded information is reconstructed by inverse coding followed by inverse quantization and finally the accumulation of pixel differences in the TMC2311.

Figure 18. Differential Pulse Code Modulation System (No Cosine Transform)



## Package Interconnections

| Signal Type | Signal Name | Function | Value | R1 Package Pin |
|---|---|---|---|---|
| Power | $V_{DD}$ | Supply Voltage | +5.0V | 2 10 17 33 53 68 |
| | GND | Ground | 0.0V | 1 4 9 13 18 26 35 52 67 |
| Clock | CLK | System Clock | TTL | 65 |
| Inputs | $DIN_{11-0}$ | Data Inputs | TTL | 44 45 46 47 48 49 50 51 54 55 56 57 |
| | $DX_{8-0}$ | Aux Adder In | TTL | 34 36 37 38 39 40 41 42 43 |
| Outputs | $DOUT_{11-0}$ | Data Outputs | TTL | 5 6 7 8 11 12 14 15 16 19 20 21 |
| | BOT | Begin Transform | TTL | 22 |
| | EOB | End Of Block | TTL | 23 |
| Control | INIT | Initialize | TTL | 60 |
| | NOOP | No Operation | TTL | 61 |
| | $\overline{WR}$ | Control Preload | TTL | 66 |
| | $\overline{RD}$ | Read Control | TTL | 64 |
| | ISEL | Input Data Select | TTL | 59 |
| | OSEL | Output Select | TTL | 58 |
| | $\overline{OE}$ | Output Enable | TTL | 3 |
| | $\overline{FE}$ | Flag Enable | TTL | 62 |
| | $CTRL_{7-0}$ | Control Params | TTL | 32 31 30 29 28 27 25 24 |
| | DNR | Test Pin | — | 63 |
| Do Not Connect | | | | |

## Ordering Information

| Product Number | Data Rate MHz | Temperature Range | Screening | Package | Package Marking |
|---|---|---|---|---|---|
| TMC2311R1C | 13.5 | STD-$T_A$ = 0°C to 70°C | Commercial | 68 Pin PLCC | 2311R1C |
| TMC2311R1C1 | 14.5 | STD-$T_A$ = 0°C to 70°C | Commercial | 68 Pin PLCC | 2311R1C1 |
| TMC2311R1C2 | 17.8 | STD-$T_A$ = 0°C to 70°C | Commercial | 68 Pin PLCC | 2311R1C2 |

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