

040152

PRELIMINARY



HY61C68

4096x4-Bit CMOS Static RAM

OCTOBER 1986

DESCRIPTION

The HY61C68 is a high speed, low power, 4096-word by 4-bit static CMOS RAM fabricated using high-performance CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields access times of 25 ns maximum.

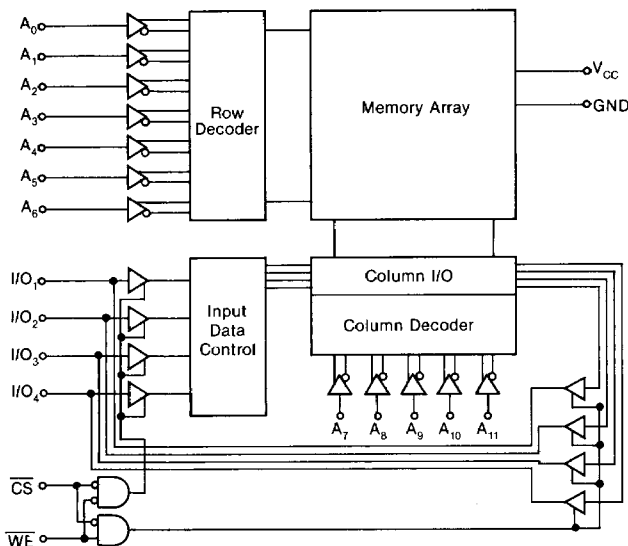
When chip select is brought high, the device assumes a standby mode in which the device power dissipation is reduced to 0.5 μ W (typically). The HY61C68L has a data retention mode that guarantees data will remain valid at a minimum power supply voltage of 2.0 volts.

Using CMOS technology, supply voltages from 2.0 to 5.5 volts have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY61C68 family.

FEATURES

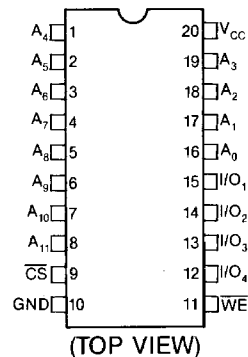
- ▲ Single +5V Operation ($\pm 10\%$)
- ▲ Fast Access Time—25/35/45/55/70ns
- ▲ Equal Access and cycle times
- ▲ Standard 20 pin 300 mil DIP
- ▲ Low Power Dissipation
 - Operating 150mW (typ.)
 - Stand-by 0.5 μ W (typ.)
- ▲ Capable of Battery Back-up Operation
 - 2 volt data retention (HY61C68L)
- ▲ Six transistor CMOS Memory Cell
- ▲ All inputs and output directly TTL-compatible
- ▲ Fully Static Operation
 - No clock or refresh required
- ▲ For extended temperature ranges, variation in access times, packages, power consumption and screening, call HYUNDAI.

BLOCK DIAGRAM



Part Number	POWER SUPPLY CURRENT			
	Access Time (ns, max)	Active (mA, max)	Standby (μ A, max)	Data Retention (μ A, max)
HY61C68-25	25	150	100	N/A
HY61C68-35	35	120	100	N/A
HY61C68-45	45	100	100	N/A
HY61C68-55	55	80	100	N/A
HY61C68-70	70	70	100	N/A
HY61C68L-25	25	120	2	2
HY61C68L-35	35	110	2	2
HY61C68L-45	45	90	2	2
HY61C68L-55	55	70	2	2
HY61C68L-70	70	60	2	2

PIN CONNECTIONS



HY61C68 Family High Performance Low Power 4096×4-Bit CMOS Static RAM

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5* to +7.0	V
T_{OPR}	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1.0	W

*-3.5V for 20ns pulse.

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

$T_A = 0$ to 70°C

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

(See Figure 1)

TRUTH TABLE

MODE	\overline{CS}	\overline{WE}	V_{CC} Current	I/O Pin	Ref. Cycle
Not selected	H	X	I_{SB} I_{SBI}	High-Z	
Read	L	H	I_{CC}	D_{OUT}	Read Cycle
Write	L	L	I_{CC}	D_{IN}	Write Cycle

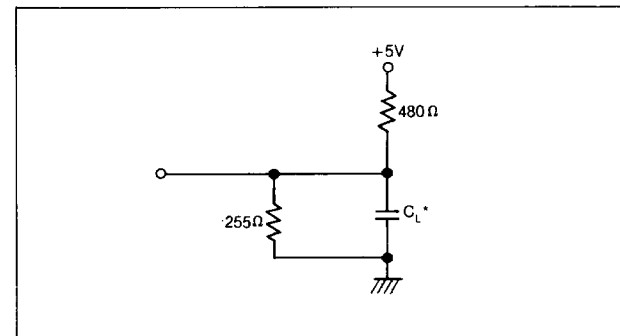
RECOMMENDED DC OPERATING CONDITIONS

$T_A = 0$ to 70°C

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5*	—	+0.8	V

*-3.5V for 20ns pulse.

OUTPUT LOAD



*Including scope and the jig

$C_L = 30$ pF standard output

$C_L = 5$ pF for t_{HZ} , t_{LZ} , t_{WZ} & t_{OW}

CAPACITANCE⁽¹⁾

$T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	3	4	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	4	6	pF

1. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{CC}=5V \pm 10\%$, $T_A=0$ to $70^\circ C$

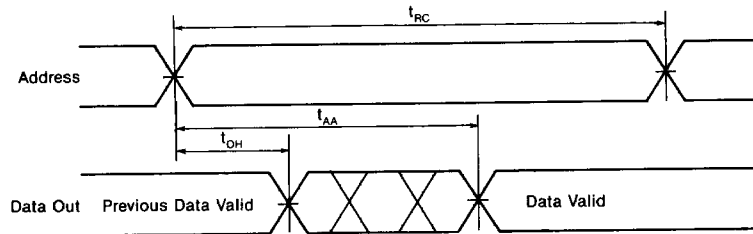
READ CYCLE

SYMBOL	PARAMETER	HY61C68-25		HY61C68-35		HY61C68-45		HY61C68-55		HY61C68-70		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle	25	—	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chips Select Access Time	—	25	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Adress Change	0	—	3	—	5	—	10	—	5	—	ns
t_{Lz}	Chip Selection to Output in Low z	0	—	3	—	5	—	10	—	15	—	ns
t_{HZ}	Chip Selection to Output in High z	0	15	0	15	0	20	0	20	0	20	ns
t_{PU}	Chip Selection to Power up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	25	—	25	—	30	—	30	—	30	ns

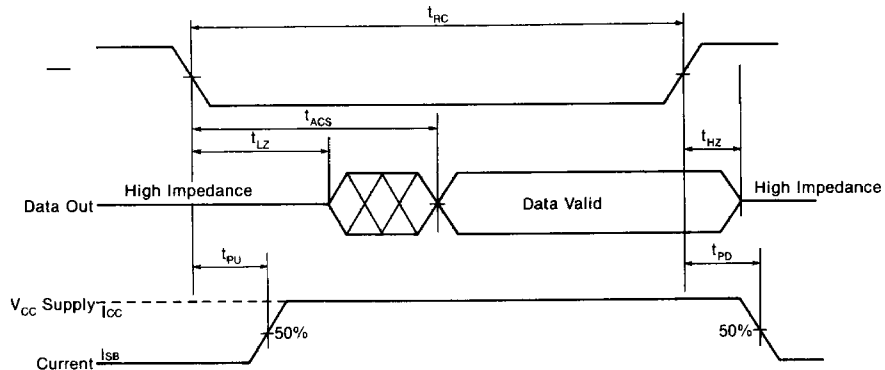
NOTES:

1. Test conditions: assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and load capacitance, as in Output Load.

TIMING WAVEFORMS OF READ CYCLE 1 (4.5)



TIMING WAVEFORMS OF READ CYCLE 2 (4.6)



NOTES:

1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{Lz} min. both for a given device and from device to device.
3. Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Load B.
4. \overline{WE} is High for read cycle.
5. Device is continuously selected. $\overline{CS}=I_{IL}$.
6. Addresses valid prior to or coincident with \overline{CS} transition low.
7. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS(1)

$V_{CC}=5V\pm 10\%$, $T_A=0$ to $70^\circ C$

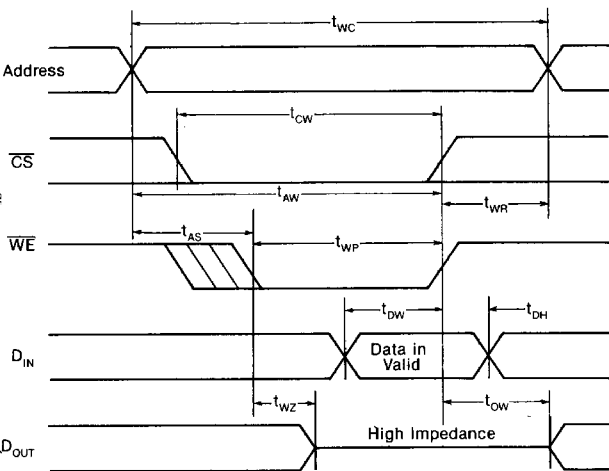
WRITE CYCLE

SYMBOL	PARAMETER	HY61C68-25		HY61C68-35		HY61C68-45		HY61C68-55		HY61C68-70		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
t_{CW}	Chip Selection to End of Write	25	—	30	—	40	—	50	—	65	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	40	—	50	—	65	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	5	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	5	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	25	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z	—	5	—	15	—	20	—	20	—	25	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

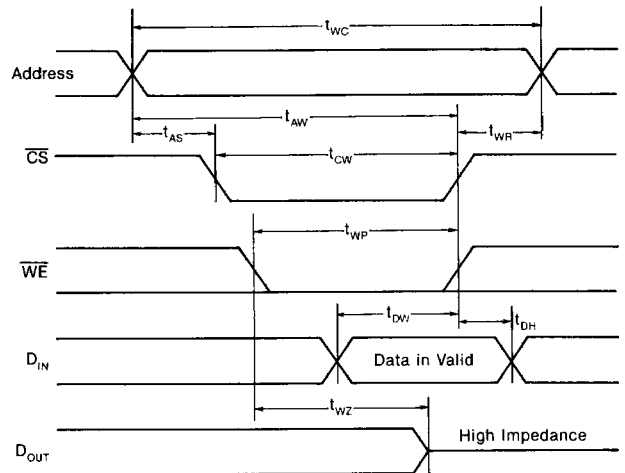
NOTES:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, an in Output Load.

WRITE CYCLE 1 (\overline{WE} Controlled)



WRITE CYCLE 2 (\overline{CS} Controlled)



NOTES:

1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . (t_{WP}).
2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
3. During the period, I/O pins are in the output state. Input signals of opposite phase to the outputs must not be applied.
4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output buffer buffers remain in a high impedance state.
5. If \overline{CS} is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied.
6. Transition is measured $\pm 500mV$ from steady state voltage specified loading in Load B.
7. This parameter is sampled and not 100% tested.

DC and Operating Characteristics

($V_{CC}=5V \pm 10\%$, $T_a=0$ to $70^\circ C$)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input Leakage Current	$ I_{Li} $	$V_{CC}=5.5V$, $V_{IN}=0V$ to V_{CC}	—	—	2	μA	
Output Leakage Current	$ I_{Lo} $	$\overline{CS}=V_{IH}$, $V_{OUT}=0V$ to V_{CC}	—	—	2	μA	
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	30	60	mA	
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$ <i>TTL</i>	—	2	5	mA	
	I_{SB1} <i>CMOS</i>	$\overline{CS}=V_{CC}-0.2V$	HY61C68	—	4	100	μA
		$V_{IN}=0V$ to V_{CC}	HY61C68L	—	0.1	2	
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.4	V	
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V	

NOTE:

Typical values are at $V_{CC}=5.0V$, $T_a=25^\circ C$ and specified loading.

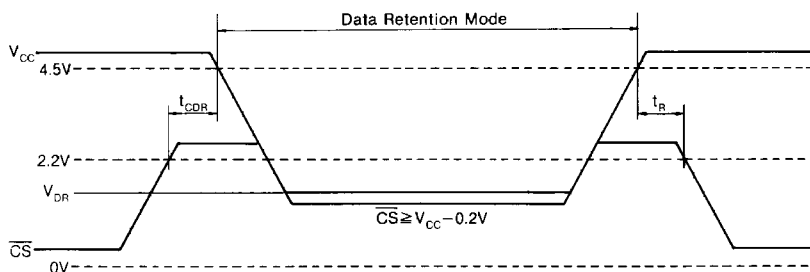
LOW V_{CC} DATA RETENTION CHARACTERISTICS

($T_a=0^\circ C$ to $70^\circ C$)

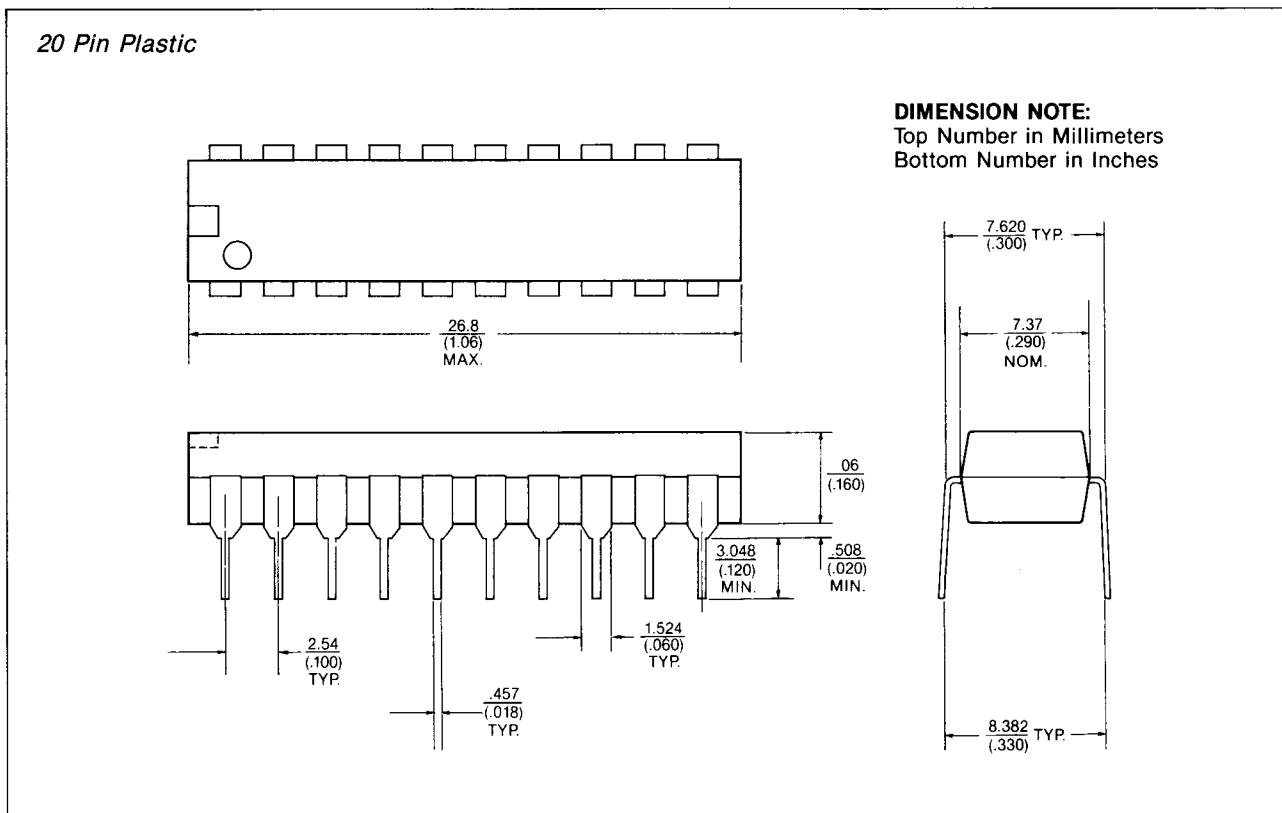
PARAMETER	SYMBOL	TEST CONDITIONS	HY61C68L-25/35/45/55/70			Unit
			Min.	Typ.	Max.	
V_{CC} for Data Retention	V_{DR}		2.0	—	5.5	V
Data Retention Current	I_{CCDR}	$\overline{CS} \geq V_{CC}-0.2V$		0.05	2	μA
Chip Deselect to Data Retention Time	t_{CDR}	$V_{IN}=0V$ to V_{CC}	0	—	—	ns
Operation Recovery Time	t_R	$V_{CC}=2V$	t_{RC}^*	—	—	ns

* t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



PACKAGE OUTLINE



ORDERING INFORMATION

HY61C68 X X XX

OPERATING TEMPERATURE RANGE

STANDARD TYPE & 0°C TO +70°C NO MARK
 LOW POWER TYPE & 0°C TO +70°C L

SPEED

25: 25ns
 35: 35ns
 45: 45ns
 55: 55ns
 70: 70ns

PACKAGE TYPE

PLASTIC DIP 300MIL
 PLCC J-FORM
 SOIC
 CERDIP DIP 300MIL
 CERAMIC S/B 300MIL
 PGA
 LCC

S
 F
 J
 K
 T
 G
 N