

SN10KHT5565, SN100KT5565
OCTAL TTL/ECL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
 T-52-11
 D3541, JUNE 1990

- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} , V_{EE} , and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

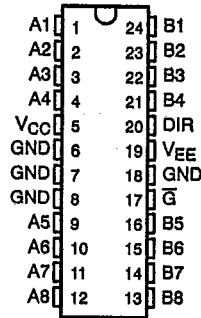
The SN10KHT5565 and SN100KT5565 are noninverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50- Ω load terminated to -2 V.

When the output-enable input \bar{G} is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. When \bar{G} is high, both buses are in the high-impedance state. Both \bar{G} and DIR are ECL-compatible.

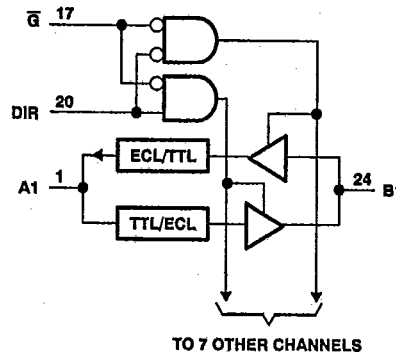
The SN10KHT5565 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5565 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

DW OR NT PACKAGE
 (TOP VIEW)



logic diagram (positive logic)



PRODUCT PREVIEW

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.