



**Advanced
Micro
Devices**

Am386™DX

High-Performance 32-Bit Microprocessor

DISTINCTIVE CHARACTERISTICS

- Compatible with 386DX systems and software
- 40-, 33-, 25-, and 20-MHz clock speeds
- 32-bit microprocessor for personal computers and embedded systems
- 32-bit address and data bus for high performance
 - 4-Gb physical address space
 - 64-tb virtual address space
 - 4-Gb maximum segment size
- Supports 387DX-compatible math coprocessor
- AMD advanced 0.8 micron CMOS technology
- 132-lead ceramic PGA package or optional 132-lead plastic quad flat pack (PQFP) package

GENERAL DESCRIPTION

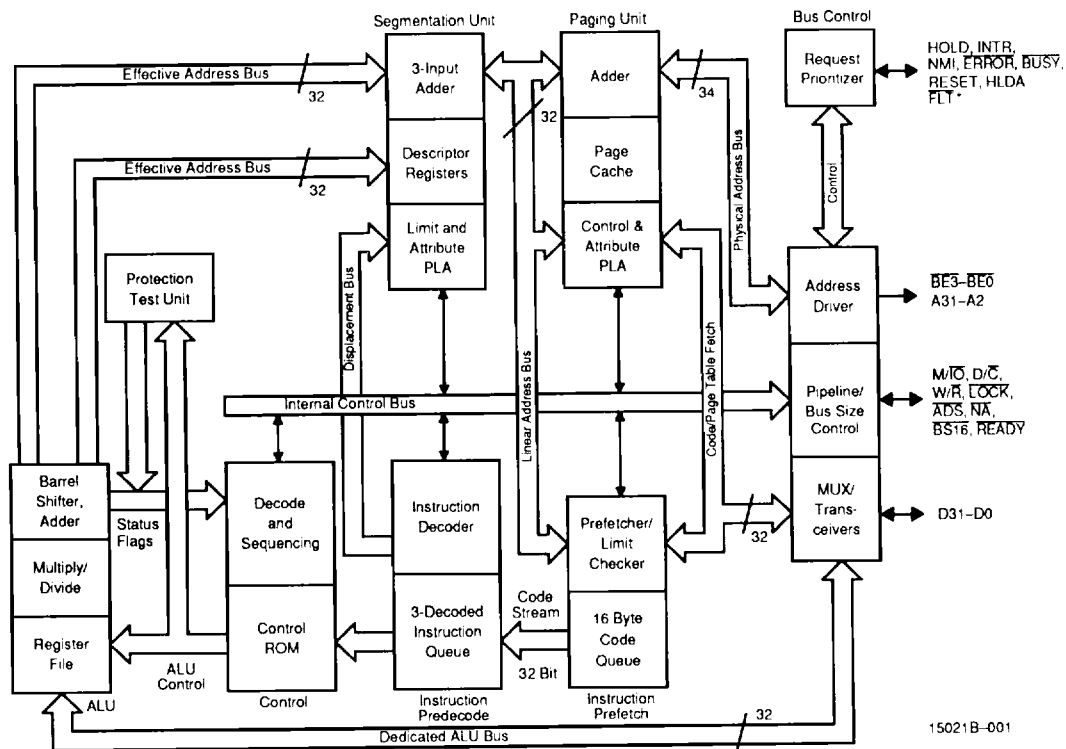
The Am386DX microprocessor is a compatible implementation of the Intel i386DX. It is engineered to meet strict requirements for compatibility. It is compatible with 386DX-based hardware, and is in fact a plug-in replacement for the Intel i386DX. It is also compatible with operating systems written for the 386 and the wide variety of commercially available software applications.

The Am386DX device is an advanced 32-bit microprocessor designed for applications needing very high performance. This device offers a 21% increase in performance from 33 to 40 MHz. The 32-bit registers and data paths support 32-bit addresses and data types. The processor addresses up to 4 Gb of physical

memory and 64 tb of virtual memory. The integrated memory management and protection architecture allow high-performance execution of operating systems including DOS, Windows, OS/2, and UNIX.

The device is manufactured using the AMD advanced 0.8 micron CMOS process and is packaged in a standard 132-lead ceramic pin grid array (PGA) package. Additionally, the Am386DX microprocessor will be available in a small footprint 132-pin plastic quad flat pack (PQFP) package. This surface-mount package is 40% smaller than PGA allowing smaller, lower cost board designs without the need for a socket.

BLOCK DIAGRAM



*Float feature available in Rev. C0 and later, PQFP only.

INTRODUCTION

AMD is proud to provide the Am386DX microprocessor at a time when the personal computer market requires alternatives. Alternate source manufacturers traditionally increase availability, add features, and broaden the market. AMD has focused significant engineering resources to bring you these benefits.

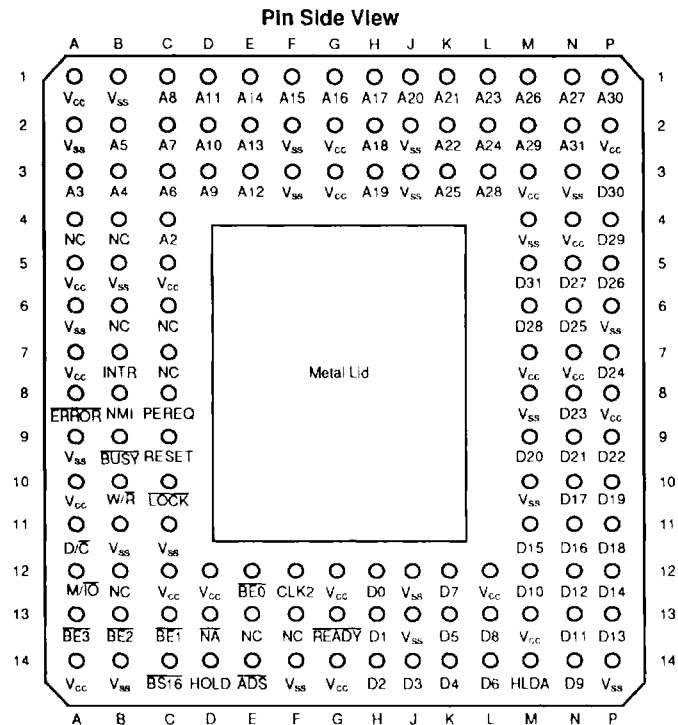
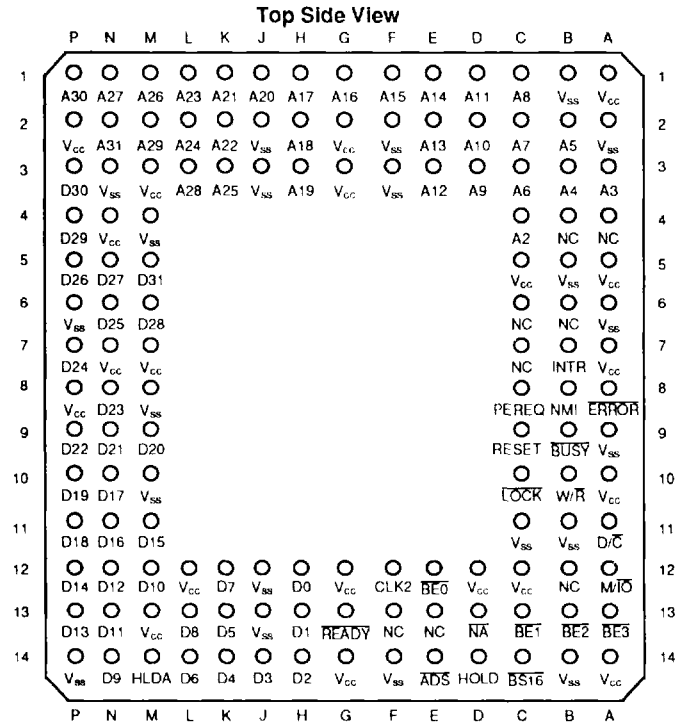
AMD's track record with the 80286 shows that we were first to raise the performance of the 80286 from 8 MHz to 10, 12, and 16 MHz. We were first to offer new packaging technology with a smaller, lower cost PLCC. Today, over 90% of all 80286s sold use PLCC packaging. AMD is committed to similar advances with the Am386DX microprocessor.

Another member of the family is the Am386DXL microprocessor. This device offers several enhancements including operating speeds up to 40 MHz, true static compatibility, and a small footprint cost-saving PQFP package. The Am386DXL microprocessor provides higher speeds and lower heat dissipation for desktop PCs, allowing the use of a smaller, or even, no cooling fan. For portables, its true static design allows for longer battery life with low power consumption and standby mode. (See Am386DXL CPU Data Sheet for more information—order #15484.)

AMD has engineered the Am386DX microprocessor to insure compatibility with the installed base of hardware and software for 386-based personal computers. The Am386DX microprocessor is your solution to meet the demand for high-performance, 32-bit personal computers.

CONNECTION DIAGRAMS

132-Lead Ceramic Pin Grid Array (PGA) Package



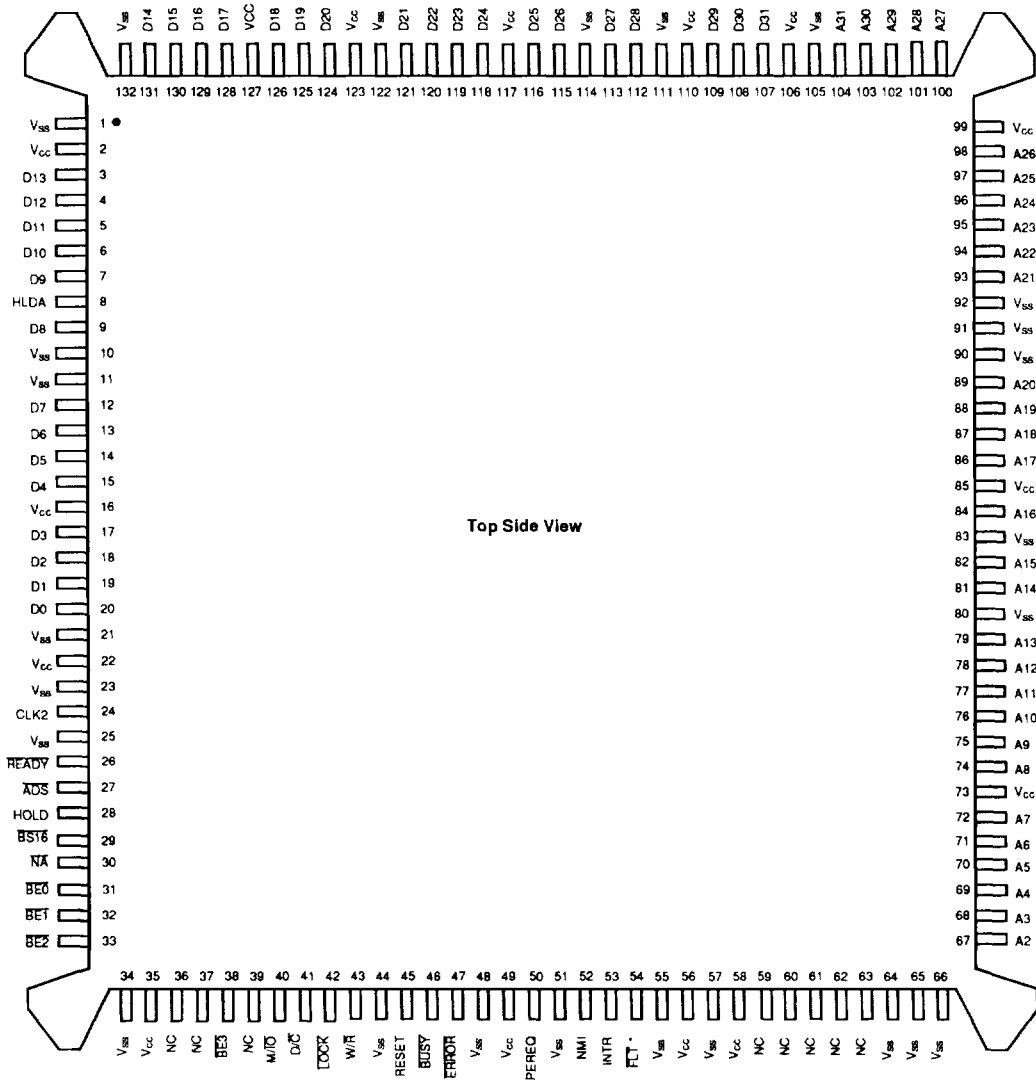
PGA Pin Designations (Functional Grouping)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A2	C4	A24	L2	D6	L14	D28	M6	V _{cc}	C12	V _{ss}	F2
A3	A3	A25	K3	D7	K12	D29	P4		D12		F3
A4	B3	A26	M1	D8	L13	D30	P3		G2		F14
A5	B2	A27	N1	D9	N14	D31	M5		G3		J2
A6	C3	A28	L3	D10	M12	D/C	A11		G12		J3
A7	C2	A29	M2	D11	N13	ERROR	A8		G14		J12
A8	C1	A30	P1	D12	N12	HLDA	M14		L12		J13
A9	D3	A31	N2	D13	P13	HOLD	D14		M3		M4
A10	D2	ADS	E14	D14	P12	INTR	B7		M7		M8
A11	D1	BE0	E12	D15	M11	LOCK	C10		M13		M10
A12	E3	BE1	C13	D16	N11	M/I _O	A12		N4		N3
A13	E2	BE2	B13	D17	N10	NA	D13		N7		P6
A14	E1	BE3	A13	D18	P11	NMI	B8		P2		P14
A15	F1	BS16	C14	D19	P10	PEREQ	C8		P8	W/R	B10
A16	G1	BUSY	B9	D20	M9	READY	G13	V _{ss}	A2	NC	A4
A17	H1	CLK2	F12	D21	N9	RESET	C9		A6		B4
A18	H2	D0	H12	D22	P9	V _{cc}	A1		A9		B6
A19	H3	D1	H13	D23	N8		A5		B1		B12
A20	J1	D2	H14	D24	P7		A7		B5		C6
A21	K1	D3	J14	D25	N6		A10		B11		C7
A22	K2	D4	K14	D26	P5		A14		B14		E13
A23	L1	D5	K13	D27	N5		C5		C11		F13

PGA Pin Designations (Sorted by Pin No.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	V _{cc}	B9	BUSY	D3	A9	H1	A17	L13	D8	N7	V _{cc}
A2	V _{ss}	B10	W/R	D12	V _{cc}	H2	A18	L14	D6	N8	D23
A3	A3	B11	V _{ss}	D13	NA	H3	A19	M1	A26	N9	D21
A4	NC	B12	NC	D14	HOLD	H12	D0	M2	A29	N10	D17
A5	V _{cc}	B13	BE2	E1	A14	H13	D1	M3	V _{cc}	N11	D16
A6	V _{ss}	B14	V _{ss}	E2	A13	H14	D2	M4	V _{ss}	N12	D12
A7	V _{cc}	C1	A8	E3	A12	J1	A20	M5	D31	N13	D11
A8	ERROR	C2	A7	E12	BE0	J2	V _{ss}	M6	D28	N14	D9
A9	V _{ss}	C3	A6	E13	NC	J3	V _{ss}	M7	V _{cc}	P1	A30
A10	V _{cc}	C4	A2	E14	ADS	J12	V _{ss}	M8	V _{ss}	P2	V _{cc}
A11	D/C	C5	V _{cc}	F1	A15	J13	V _{ss}	M9	D20	P3	D30
A12	M/I _O	C6	NC	F2	V _{ss}	J14	D3	M10	V _{ss}	P4	D29
A13	BE3	C7	NC	F3	V _{ss}	K1	A21	M11	D15	P5	D26
A14	V _{cc}	C8	PEREQ	F12	CLK2	K2	A22	M12	D10	P6	V _{ss}
B1	V _{ss}	C9	RESET	F13	NC	K3	A25	M13	V _{cc}	P7	D24
B2	A5	C10	LOCK	F14	V _{ss}	K12	D7	M14	HLDA	P8	V _{cc}
B3	A4	C11	V _{ss}	G1	A16	K13	D5	N1	A27	P9	D22
B4	NC	C12	V _{cc}	G2	V _{cc}	K14	D4	N2	A31	P10	D19
B5	V _{ss}	C13	BE1	G3	V _{cc}	L1	A23	N3	V _{ss}	P11	D18
B6	NC	C14	BS16	G12	V _{cc}	L2	A24	N4	V _{cc}	P12	D14
B7	INTR	D1	A11	G13	READY	L3	A28	N5	D27	P13	D13
B8	NMI	D2	A10	G14	V _{cc}	L12	V _{cc}	N6	D25	P14	V _{ss}

CONNECTION DIAGRAMS (continued) 132-Lead Plastic Quad Flat Pack (PQFP) Package



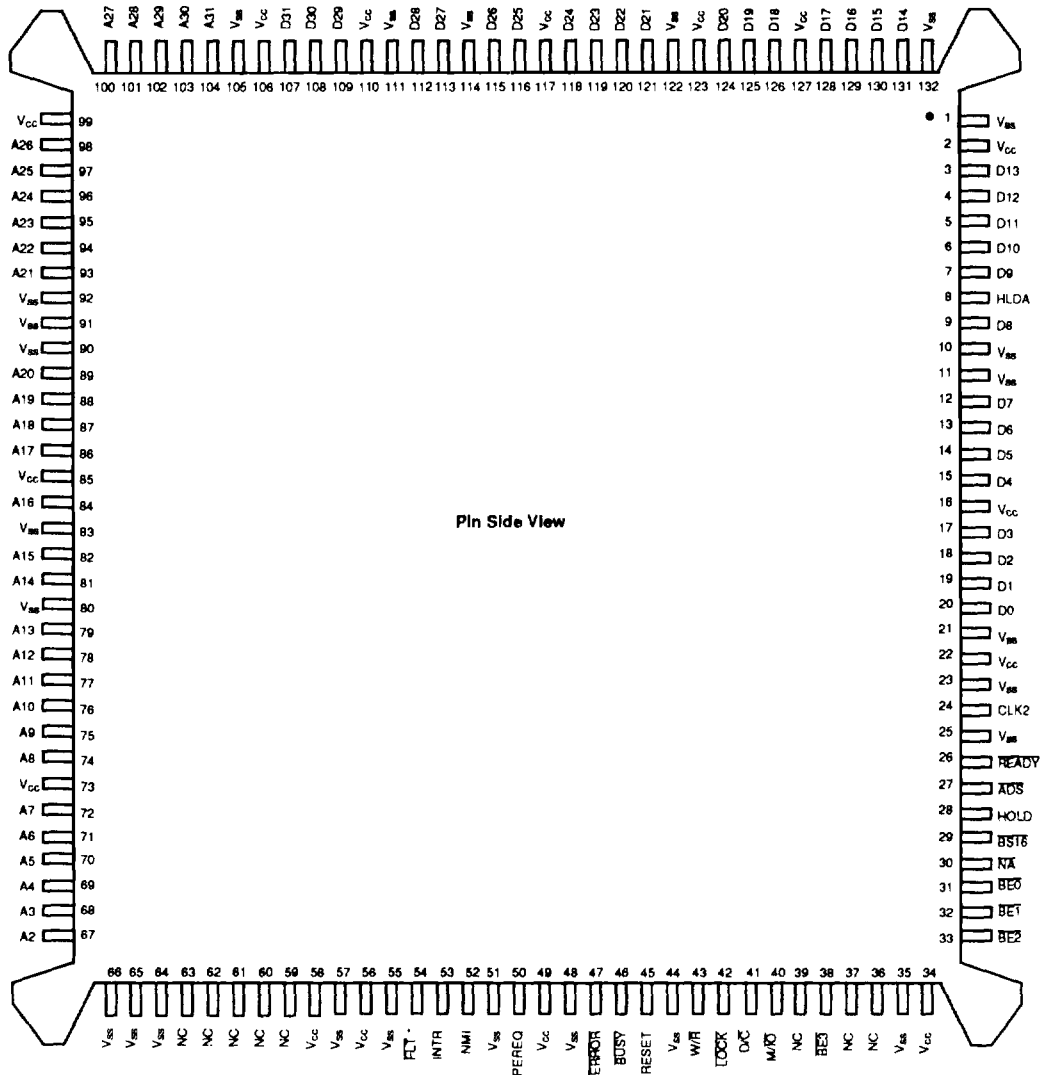
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Notes: Pin 1 is marked for orientation.

*Float feature available in Rev. C0 and later, PQFP only.

CONNECTION DIAGRAMS (continued)

132-Lead Plastic Quad Flat Pack (PQFP) Package



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Notes: Pin 1 is marked for orientation.

*Float feature available in Rev. C0 and later, PQFP only.

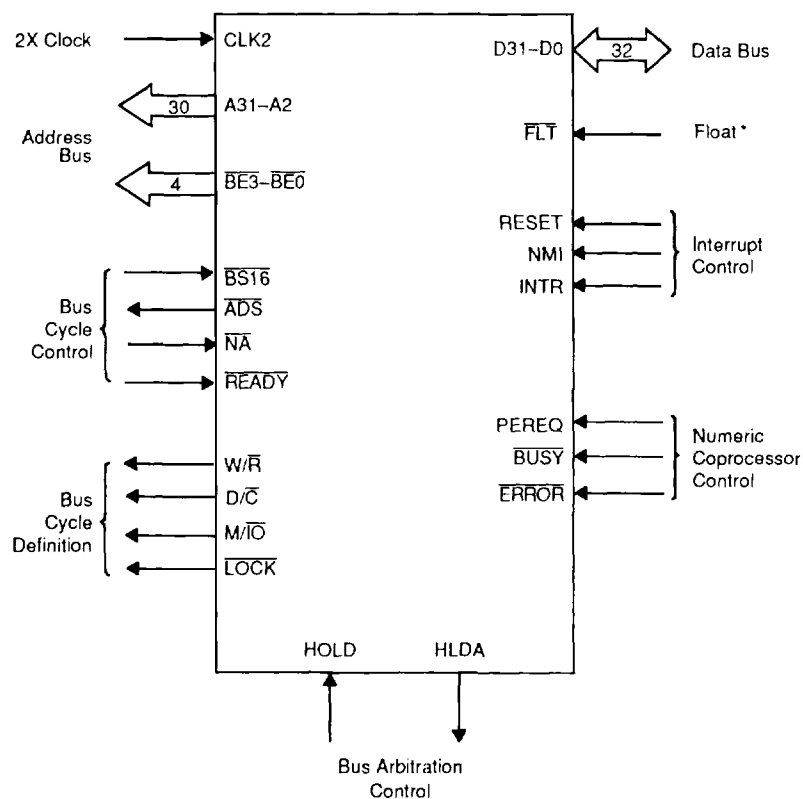
PQFP Pin Designation (Functional Grouping)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A2	67	A24	96	D6	13	D28	112	V _{CC}	56	V _{SS}	64
A3	68	A25	97	D7	12	D29	109		58		65
A4	69	A26	98	D8	9	D30	108		73		66
A5	70	A27	100	D9	7	D31	107		85		80
A6	71	A28	101	D10	6	D/C	41		99		83
A7	72	A29	102	D11	5	ERROR	47		106		90
A8	74	A30	103	D12	4	HLDA	8		110		91
A9	75	A31	104	D13	3	HOLD	28		117		92
A10	76	ADS	27	D14	131	INTR	53		123		105
A11	77	BE0	31	D15	130	LOCK	42		127		111
A12	78	BE1	32	D16	129	M/IO	40	V _{SS}	1		114
A13	79	BE2	33	D17	128	NA	30		10		122
A14	81	BE3	38	D18	126	NMI	52		11		132
A15	82	BS16	29	D19	125	PEREQ	50		21	W/R	43
A16	84	BUSY	46	D20	124	READY	26		23	NC	36
A17	86	CLK2	24	D21	121	RESET	45		25		37
A18	87	D0	20	D22	120	V _{CC}	2		35		39
A19	88	D1	19	D23	119		16		44		59
A20	89	D2	18	D24	118		22		48		60
A21	93	D3	17	D25	116		34		51		61
A22	94	D4	15	D26	115		49		55		62
A23	95	D5	14	D27	113	FLT*	54		57		63

PQFP Pin Designation (Sorted by Pin No.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	23	V _{SS}	45	RESET	67	A2	89	A20	111	V _{SS}
2	V _{CC}	24	CLK2	46	BUSY	68	A3	90	V _{SS}	112	D28
3	D13	25	V _{SS}	47	ERROR	69	A4	91	V _{SS}	113	D27
4	D12	26	READY	48	V _{SS}	70	A5	92	V _{SS}	114	VSS
5	D11	27	ADS	49	V _{CC}	71	A6	93	A21	115	D26
6	D10	28	HOLD	50	PEREQ	72	A7	94	A22	116	D25
7	D9	29	BS16	51	V _{SS}	73	V _{CC}	95	A23	117	V _{CC}
8	HLDA	30	NA	52	NMI	74	A8	96	A24	118	D24
9	D8	31	BE0	53	INTR	75	A9	97	A25	119	D23
10	V _{SS}	32	BE1	54	FLT*	76	A10	98	A26	120	D22
11	V _{SS}	33	BE2	55	V _{SS}	77	A11	99	V _{CC}	121	D21
12	D7	34	V _{CC}	56	V _{CC}	78	A12	100	A27	122	V _{SS}
13	D6	35	V _{SS}	57	V _{SS}	79	A13	101	A28	123	V _{CC}
14	A5	36	NC	58	V _{CC}	80	V _{SS}	102	A29	124	D20
15	D4	37	NC	59	NC	81	A14	103	A30	125	D19
16	V _{CC}	38	BE3	60	NC	82	A15	104	A31	126	D18
17	D3	39	NC	61	NC	83	V _{SS}	105	V _{SS}	127	V _{CC}
18	D2	40	M/IO	62	NC	84	A16	106	V _{CC}	128	D17
19	D1	41	D/C	63	NC	85	V _{CC}	107	D31	129	D16
20	D0	42	LOCK	64	V _{SS}	86	A17	108	D30	130	D15
21	V _{SS}	43	W/R	65	V _{SS}	87	A18	109	D29	131	D14
22	V _{CC}	44	V _{SS}	66	V _{SS}	88	A19	110	V _{CC}	132	V _{SS}

*Float feature available in Rev. C0 and later, PQFP only.



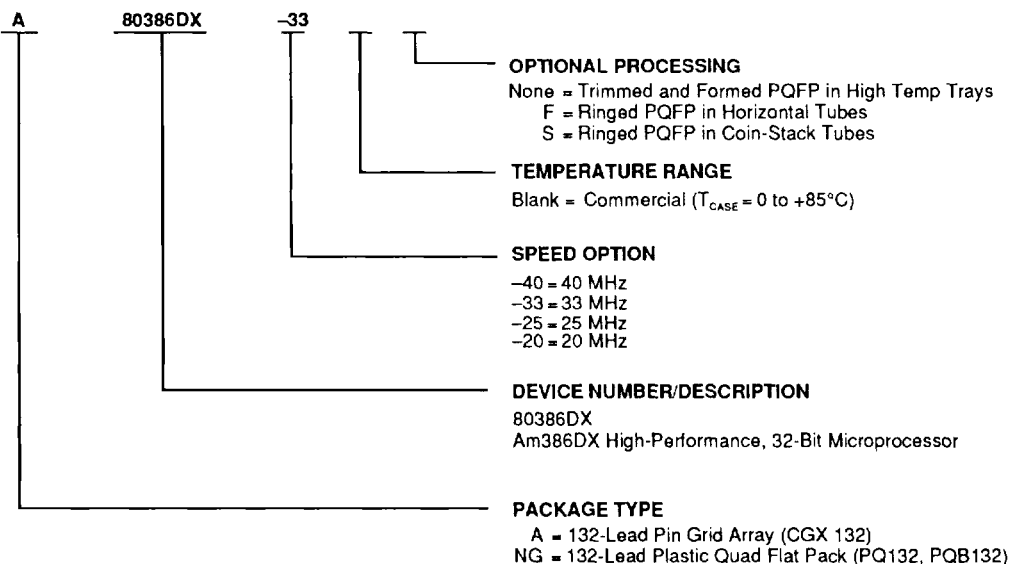
*Float feature available in Rev. C0 and later, PQFP only.

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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
A	80386DX	-40 -33 -25 -20
NG	80386DX	-40F, -40S -33F, -33S -25F, -25S -20F, -20S

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

A31–A2

Address Bus (Outputs)

Outputs physical memory or port I/O addresses.

$\overline{ADS}$

Address Status (Active Low; Output)

Indicates that a valid bus cycle definition and address ($\overline{W/R}$, $\overline{D/C}$, $\overline{M/I/O}$, $\overline{BE0}$, $\overline{BE1}$, $\overline{BE2}$, $\overline{BE3}$, and A31–A2) are being driven at the Am386DX microprocessor pins.

$\overline{BE3}–\overline{BE0}$

Byte Enables (Active Low; Outputs)

Indicate which data bytes of the data bus take part in a bus cycle.

$\overline{BS16}$

Bus Size 16 (Active Low; Input)

Allows direct connection of 32-bit and 16-bit data buses.

$\overline{BUSY}$

Busy (Active Low; Input)

Signals a busy condition from a processor extension.

CLK2

Clock (Input)

Provides the fundamental timing for the Am386DX microprocessor.

D31–D0

Data Bus (Inputs/Outputs)

Inputs data during memory, I/O, and interrupt acknowledge read cycles and outputs data during memory and I/O write cycles.

$\overline{D/C}$

Data/Control (Output)

A bus cycle definition pin that distinguishes data cycles, either memory or I/O from control cycles which are: interrupt acknowledge, halt, and instruction fetching.

$\overline{ERROR}$

Error (Active Low; Input)

Signals an error condition from a processor extension.

$\overline{FLT}^*$

Float (Active Low; Input)

An input signal which forces all bi-directional and output signals, including HLDA, to the three-state condition.

$\overline{FLT}$ has an internal pull-up resistor, and if it is not used it should be unconnected.

HLDA

Bus Hold Acknowledge (Active High; Output)

Indicates that the Am386DX microprocessor surrendered control of its local bus to another bus master.

HOLD

Bus Hold Request (Active High; Input)

Allows another bus master to request control of the local bus.

INTR

Interrupt Request (Active High; Input)

A maskable input that signals the Am386DX microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

$\overline{LOCK}$

Bus Lock (Active Low; Output)

A bus cycle definition pin that indicates that other system bus masters are denied access to the system bus while it is active.

$\overline{M/I/O}$

Memory I/O (Output)

A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

$\overline{NA}$

Next Address (Active Low; Input)

Used to request address pipelining.

NC

No Connect

Should always remain unconnected. Connection of a NC pin may cause the processor to malfunction or be incompatible with future steppings of the Am386DX microprocessor.

NMI

Non-Maskable Interrupt Request (Active High; Input)

A non-maskable input that signals the Am386DX microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

PEREQ

Processor Extension Request (Active High; Input)

Indicates that the processor extension has data to be transferred by the Am386DX microprocessor.

$\overline{READY}$

Bus Ready (Active Low; Input)

Terminates the bus cycle.

RESET

Reset (Active High; Input)

Suspends any operation in progress and places the Am386DX microprocessor in a known reset state.

V_{cc}

System Power (Active High; Input)

Provides the +5 V nominal DC supply input.

V_{ss}

System Ground (Input)

System ground provides 0 V connection from which all inputs and outputs are measured.

$\overline{W/R}$

Write/Read (Output)

A bus cycle definition pin that distinguishes write cycles from read cycles.

*Float feature available in Rev C0 and later, PQFP only.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature Under Bias . . -65°C to $+125^{\circ}\text{C}$
 Supply Voltage with Respect
 to V_{SS} -0.5 V to $+7\text{ V}$
 Voltage on Other Pins -0.5 V to $V_{CC} + 0.5\text{ V}$

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

DC CHARACTERISTICS over COMMERCIAL operating ranges

$V_{CC} = 5\text{ V} \pm 5\%$; $T_{CASE} = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (PGA)
 $V_{CC} = 5\text{ V} \pm 10\%$; $T_{CASE} = 0^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ (PQFP)

Symbol	Parameter Description	Notes	Min	Max	Unit
V_{IL}	Input Low Voltage	(Note 1)	-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	$V_{CC} + 0.3$	V
V_{ILC}	CLK2 Input Low Voltage	(Note 1)	-0.3	0.8	V
V_{IHC}	CLK2 Input High Voltage 20 MHz		$V_{CC} - 0.8$	$V_{CC} + 0.3$	V
			3.7	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage $I_{OL} = 4\text{ mA}$: A31–A2, D31–D0 $I_{OL} = 5\text{ mA}$: $\overline{BE3}$ – $\overline{BE0}$, $\overline{W/\overline{R}}$, D/ $\overline{C}$, M/ $\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA			0.45	V
				0.45	V
V_{OH}	Output High Voltage $I_{OH} = 1\text{ mA}$: A31–A2, D31–D0 $I_{OH} = 0.9\text{ mA}$: $\overline{BE3}$ – $\overline{BE0}$, $\overline{W/\overline{R}}$, D/ $\overline{C}$, M/ $\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA		2.4		V
			2.4		V
I_U	Input Leakage Current (All pins except $\overline{BST6}$, PEREQ, $\overline{BUSY}$, $\overline{FLT}^*$, and $\overline{ERROR}$)	$0\text{ V} \leq V_{IN} \leq V_{CC}$		± 15	μA
I_{IH}	Input Leakage Current (PEREQ Pin)	$V_{IH} = 2.4\text{ V}$ (Note 2)		200	μA
I_{IL}	Input Leakage Current ($\overline{BST6}$, $\overline{BUSY}$, $\overline{FLT}^*$, and $\overline{ERROR}$)	$V_{IL} = 0.45$ (Note 3)		-400	μA
I_{LO}	Output Leakage Current	$0.45\text{ V} \leq V_{OUT} \leq V_{CC}$		± 15	μA
I_{CC}	Supply Current CLK2 = 40 MHz: with -20	$I_{CC}\text{ Typ} \approx 350$		500	mA
	CLK2 = 50 MHz: with -25	$I_{CC}\text{ Typ} \approx 375$		550	mA
	CLK2 = 66 MHz: with -33	$I_{CC}\text{ Typ} \approx 400$		550	mA
	CLK2 = 80 MHz: with -40	$I_{CC}\text{ Typ} \approx 400$		550	mA
C_{IN}	Input or I/O Capacitance	$F_C = 1\text{ MHz}$ (Note 4)		10	pF
C_{OUT}	Output Capacitance	$F_C = 1\text{ MHz}$ (Note 4)		12	pF
C_{CLK}	CLK2 Capacitance	$F_C = 1\text{ MHz}$ (Note 4)		20	pF

- Notes: 1. The Min value, -0.3 , is not 100% tested.
 2. PEREQ input has an internal pulldown resistor.
 3. $\overline{BST6}$, $\overline{BUSY}$, $\overline{FLT}^*$, and $\overline{ERROR}$ inputs each have an internal pullup resistor.
 4. Not 100% tested.
 *Float feature available in Rev. Co and later, PQFP only.

SWITCHING CHARACTERISTIC over operating range

$V_{CC} = 5\text{ V} \pm 5\%$; $T_{CASE} = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

No.	Parameter Description	Notes	Ref Figure	40 MHz Min	40 MHz Max	Unit
	Operating Frequency	Half of CLK2 Freq		8	40	MHz
1	CLK2 Period		3	12.5	62.5	ns
2a	CLK2 High Time	at 2 V	3	5		ns
2b	CLK2 High Time	at 3.7 V	3	3.25		ns
3a	CLK2 Low Time	at 2 V	3	5		ns
3b	CLK2 Low Time	at 0.8 V	3	3.25		ns
4	CLK2 Fall Time	3.7 V to 0.8 V (Note 3)	3		4	ns
5	CLK2 Rise Time	0.8 V to 3.7 V (Note 3)	3		4	ns
6	A31–A2 Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	13	ns
7	A31–A2 Float Delay	(Note 1)	13	4	20	ns
8	BE3–BE0, LOCK Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	13	ns
9	BE3–BE0, LOCK Float Delay	(Note 1)	13	4	20	ns
10	W/R, M/I $\bar{O}$, D/ $\bar{C}$ Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	13	ns
10a	ADS Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	13	ns
11	W/R, M/I $\bar{O}$, D/ $\bar{C}$, ADS Float Delay	(Note 1)	13	4	20	ns
12	D31–D0 Write Data Valid Delay	$C_L = 50\text{ pF}$ (Note 4)	2, 6, 13	7	18	ns
12a	D31–D0 Write Data Hold Time	$C_L = 50\text{ pF}$	2, 7	2		ns
13	D31–D0 Float Delay	(Note 1)	13	4	17	ns
14	HLDA Valid Delay	$C_L = 50\text{ pF}$	2, 13	4	17	ns
15	NA Setup Time		4	5		ns
16	NA Hold Time		4	2		ns
17	BS16 Setup Time		4	5		ns
18	BS16 Hold Time		4	2		ns
19	READY Setup Time		4	7		ns
20	READY Hold Time		4	4		ns
21	D31–D0 Read Setup Time		4	4		ns
22	D31–D0 Read Hold Time		4	3		ns
23	HOLD Setup Time		4	4		ns
24	HOLD Hold Time		4	2		ns
25	RESET Setup Time		14	4		ns
26	RESET Hold Time		14	2		ns
27	NMI, INTR Setup Time	(Note 2)	14	5		ns
28	NMI, INTR Hold Time	(Note 2)	14	5		ns
29	PEREQ, ERROR, BUSY Setup Time	(Note 2)	4	5		ns
30	PEREQ, ERROR, BUSY Hold Time	(Note 2)	4	4		ns

- Notes: 1. Float condition occurs when maximum output current becomes less than I_{OL} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific clock period.
3. Rise and fall times are not tested.
4. Min time not 100% tested.

SWITCHING CHARACTERISTIC over operating range $V_{CC} = 5\text{ V} \pm 5\%$; $T_{CASE} = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

No.	Parameter Description	Notes	Ref Figures	33 MHz Min	33 MHz Max	Unit
	Operating Frequency	Half of CLK2 Freq		8	33.3	MHz
1	CLK2 Period		3	15.0	62.5	ns
2a	CLK2 High Time	at 2 V	3	6.25		ns
2b	CLK2 High Time	at 3.7 V	3	4.5		ns
3a	CLK2 Low Time	at 2 V	3	6.25		ns
3b	CLK2 Low Time	at 0.8 V	3	4.5		ns
4	CLK2 Fall Time	3.7 V to 0.8 V (Note 3)	3		4	ns
5	CLK2 Rise Time	0.8 V to 3.7 V (Note 3)	3		4	ns
6	A31–A2 Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	15	ns
7	A31–A2 Float Delay	(Note 1)	13	4	20	ns
8	BE3–BE0, LOCK Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	15	ns
9	BE3–BE0, LOCK Float Delay	(Note 1)	13	4	20	ns
10	W/R, M/I $\bar{O}$, D/C Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	15	ns
10a	ADS Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	14.5	ns
11	W/R, M/I $\bar{O}$, D/C, $\bar{A}\bar{D}\bar{S}$ Float Delay	(Note 1)	13	4	20	ns
12	D31–D0 Write Data Valid Delay	$C_L = 50\text{ pF}$ (Note 4)	2, 6, 13	7	24	ns
12a	D31–D0 Write Data Hold Time	$C_L = 50\text{ pF}$	2, 7	2		ns
13	D31–D0 Float Delay	(Note 1)	13	4	17	ns
14	HLDA Valid Delay	$C_L = 50\text{ pF}$	2, 13	4	20	ns
15	NA Setup Time		4	5		ns
16	NA Hold Time		4	2		ns
17	BS16 Setup Time		4	5		ns
18	BS16 Hold Time		4	2		ns
19	READY Setup Time		4	7		ns
20	READY Hold Time		4	4		ns
21	D31–D0 Read Setup Time		4	5		ns
22	D31–D0 Read Hold Time		4	3		ns
23	HOLD Setup Time		4	11		ns
24	HOLD Hold Time		4	2		ns
25	RESET Setup Time		14	5		ns
26	RESET Hold Time		14	2		ns
27	NMI, INTR Setup Time	(Note 2)	4	5		ns
28	NMI, INTR Hold Time	(Note 2)	4	5		ns
29	PEREQ, ERROR, BUSY Setup Time	(Note 2)	4	5		ns
30	PEREQ, ERROR, BUSY Hold Time	(Note 2)	4	4		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.

2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.

3. Rise and fall times are not tested.

4. Min time not 100% tested.

SWITCHING CHARACTERISTIC over operating range

$V_{CC} = 5\text{ V} \pm 5\%$; $T_{CASE} = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (PGA)

$V_{CC} = 5\text{ V} \pm 10\%$; $T_{CASE} = 0^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ (PQFP)

No.	Parameter Description	Notes	Ref Figures	25 MHz Min	25 MHz Max	Unit
	Operating Frequency	Half of CLK2 Freq		4	25	MHz
1	CLK2 Period		3	20	125	ns
2a	CLK2 High Time	at 2 V	3	7		ns
2b	CLK2 High Time	at 3.7 V	3	4		ns
3a	CLK2 Low Time	at 2 V	3	7		ns
3b	CLK2 Low Time	at 0.8 V	3	5		ns
4	CLK2 Fall Time	3.7 V to 0.8 V (Note 3)	3		7	ns
5	CLK2 Rise Time	0.8 V to 3.7 V (Note 3)	3		7	ns
6	A31–A2 Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	21	ns
7	A31–A2 Float Delay	(Note 1)	13	4	30	ns
8	BE3–BE0 Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	24	ns
8a	LOCK Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	21	ns
9	BE3–BE0, LOCK Float Delay	(Note 1)	13	4	30	ns
10	W/R, M/I $\bar{O}$, D/ $\bar{C}$, ADS Valid Delay	$C_L = 50\text{ pF}$	2, 5, 13	4	21	ns
11	W/R, M/I $\bar{O}$, D/ $\bar{C}$, ADS Float Delay	(Note 1)	13	4	30	ns
12	D31–D0 Write Data Valid Delay	$C_L = 50\text{ pF}$	2, 6, 13	7	27	ns
12a	D31–D0 Write Data Hold Time	$C_L = 50\text{ pF}$	2, 7	2		ns
13	D31–D0 Float Delay	(Note 1)	13	4	22	ns
14	HLDA Valid Delay	$C_L = 50\text{ pF}$	2, 13	4	22	ns
15	$\bar{N}\bar{A}$ Setup Time		4	7		ns
16	$\bar{N}\bar{A}$ Hold Time		4	3		ns
17	BS16 Setup Time		4	7		ns
18	BS16 Hold Time		4	3		ns
19	READY Setup Time		4	9		ns
20	READY Hold Time		4	4		ns
21	D31–D0 Read Setup Time		4	7		ns
22	D31–D0 Read Hold Time		4	5		ns
23	HOLD Setup Time		4	15		ns
24	HOLD Hold Time		4	3		ns
25	RESET Setup Time		14	10		ns
26	RESET Hold Time		14	3		ns
27	NMI, INTR Setup Time	(Note 2)	4	6		ns
28	NMI, INTR Hold Time	(Note 2)	4	6		ns
29	PEREQ, ERROR, BUSY, FLT* Setup Time	(Note 2)	4	6		ns
30	PEREQ, ERROR, BUSY, FLT* Hold Time	(Note 2)	4	5		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} magnitude. Float delay is not 100% tested.

2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.

3. Rise and fall times are not tested.

*Float feature available in Rev C0 and later, PQFP only.

SWITCHING CHARACTERISTIC over operating range

$V_{CC} = 5\text{ V} \pm 5\%$; $T_{CASE} = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (PGA)

$V_{CC} = 5\text{ V} \pm 10\%$; $T_{CASE} = 0^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ (PQFP)

No.	Parameter Description	Notes	Ref Figures	20 MHz Min	20 MHz Max	Unit
	Operating Frequency	Half of CLK2 Freq		4	20	MHz
1	CLK2 Period		3	25	125	ns
2a	CLK2 High Time	at 2 V	3	8		ns
2b	CLK2 High Time	at ($V_{CC} - 0.8\text{ V}$)	3	5		ns
3a	CLK2 Low Time	at 2 V	3	8		ns
3b	CLK2 Low Time	at 0.8 V	3	6		ns
4	CLK2 Fall Time	($V_{CC} - 0.8\text{ V}$) to 0.8 V (Note 3)	3		8	ns
5	CLK2 Rise Time	0.8 V to ($V_{CC} - 0.8\text{ V}$) (Note 3)	3		8	ns
6	A31–A2 Valid Delay	$C_L = 120\text{ pF}$	2, 5, 13	4	30	ns
7	A31–A2 Float Delay	(Note 1)	13	4	32	ns
8	BE3–BE0, LOCK Valid Delay	$C_L = 75\text{ pF}$	2, 5, 13	4	30	ns
9	BE3–BE0, LOCK Float Delay	(Note 1)	13	4	32	ns
10	W/R, M/I $\bar{O}$, D/C, ADS Valid Delay	$C_L = 75\text{ pF}$	2, 5, 13	4	28	ns
11	W/R, M/I $\bar{O}$, D/C, ADS Float Delay	(Note 1)	13	4	30	ns
12	D31–D0 Write Data Valid Delay	$C_L = 120\text{ pF}$	2, 8, 13	4	38	ns
13	D31–D0 Float Delay	(Note 1)	13	4	27	ns
14	HLDA Valid Delay	$C_L = 75\text{ pF}$	2, 13	6	28	ns
15	NA Setup Time		4	9		ns
16	NA Hold Time		4	14		ns
17	BS16 Setup Time		4	13		ns
18	BS16 Hold Time		4	21		ns
19	READY Setup Time		4	12		ns
20	READY Hold Time		4	4		ns
21	D31–D0 Read Setup Time		4	11		ns
22	D31–D0 Read Hold Time		4	6		ns
23	HOLD Setup Time		4	17		ns
24	HOLD Hold Time		4	5		ns
25	RESET Setup Time		14	12		ns
26	RESET Hold Time		14	4		ns
27	NMI, INTR Setup Time	(Note 2)	4	16		ns
28	NMI, INTR Hold Time	(Note 2)	4	16		ns
29	PEREQ, ERROR, BUSY, FLT* Setup Time	(Note 2)	4	14		ns
30	PEREQ, ERROR, BUSY, FLT* Hold Time	(Note 2)	4	5		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} magnitude. Float delay is not 100% tested.

2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.

3. Rise and fall times are not tested.

*Float feature available in Rev. C0 and later, PQFP only.

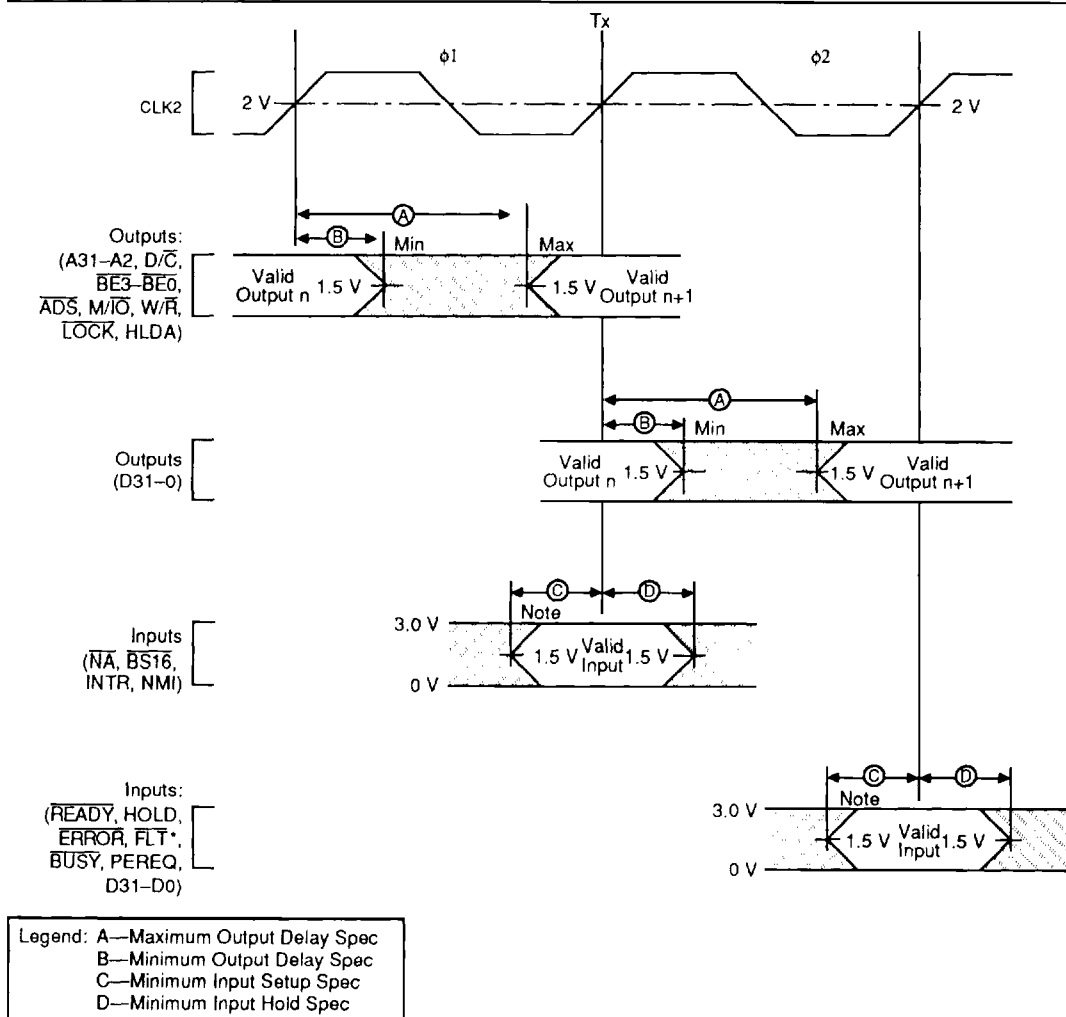
SWITCHING WAVEFORMS

The switching characteristics consist of output delays, input setup requirements, and input hold requirements. All characteristics are relative to the CLK2 rising edge crossing the 2.0 V level.

Switching characteristic measurement is defined in Figure 1. Inputs must be driven to the voltage levels indicated by this diagram. Am386DX microprocessor output delays are specified with minimum and maximum limits, measured as shown. The minimum Am386DX microprocessor delay times are hold times provided to external circuitry. Am386DX microprocessor input setup and hold time are specified as minimums, defining

the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct Am386DX microprocessor operation.

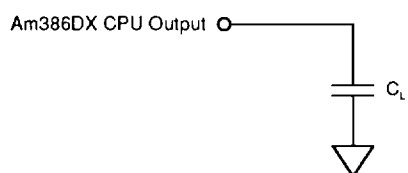
Outputs $\overline{ADS}$, $W/\overline{R}$, $D/\overline{C}$, $M/\overline{IO}$, $\overline{LOCK}$, $BE3-BE0$, $A31-A2$, and $HLDA$ only change at the beginning of phase one. $D31-D0$ (write cycles) only change at the beginning of phase two. The $\overline{READY}$, $\overline{HOLD}$, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{PEREQ}$, $\overline{FLT}^*$, and $D31-D0$ (read cycles) inputs are sampled at the beginning of phase one. The $\overline{NA}$, $\overline{BS16}$, $\overline{INTR}$, and $\overline{NMI}$ inputs are sampled at the beginning of phase two.



Note: Input waveforms have $t_r \leq 2.0$ ns from 0.8 V to 2.0 V.
 *Float feature available in Rev. Co and later, PQFP only.

15021B-071

Figure 1. Drive Levels and Measurement Points



C_L includes all parasitic capacitances.

Figure 2. AC Test Loads

15021B-072

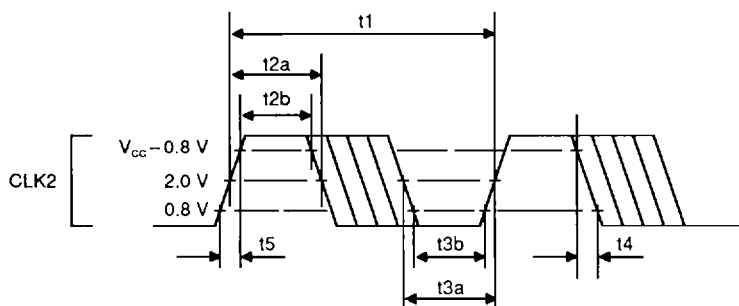
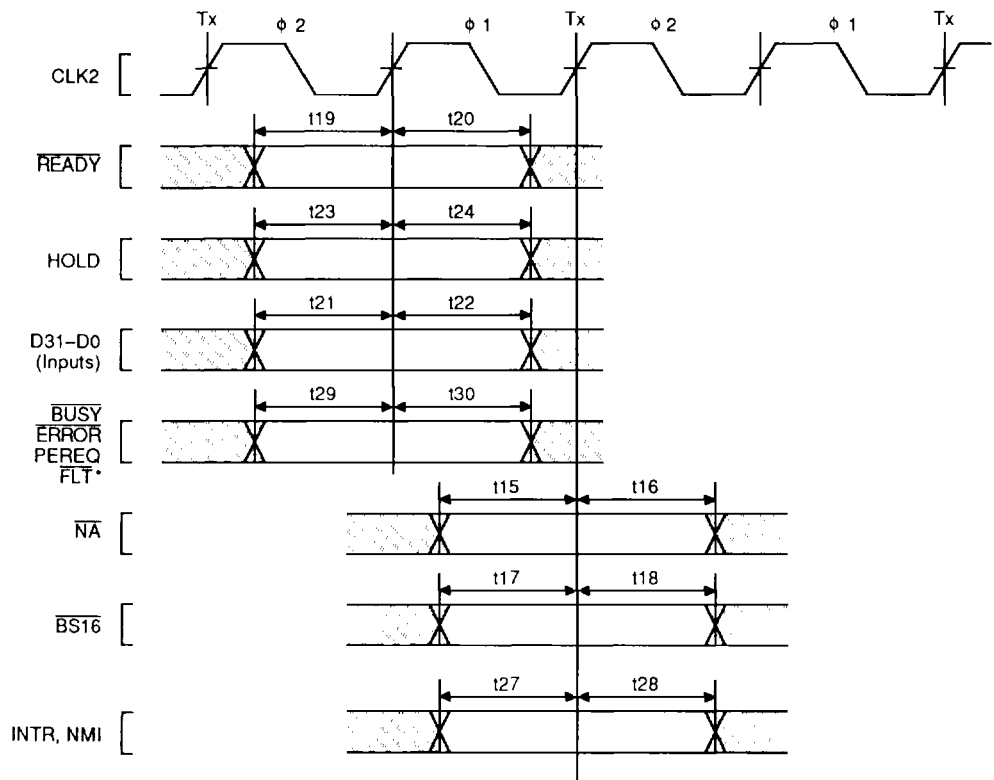


Figure 3. CLK2 Timing

15021B-073



*Float feature available in Rev. C0 and later, PQFP only.

Figure 4. Input Setup and Hold Timing

15021B-074

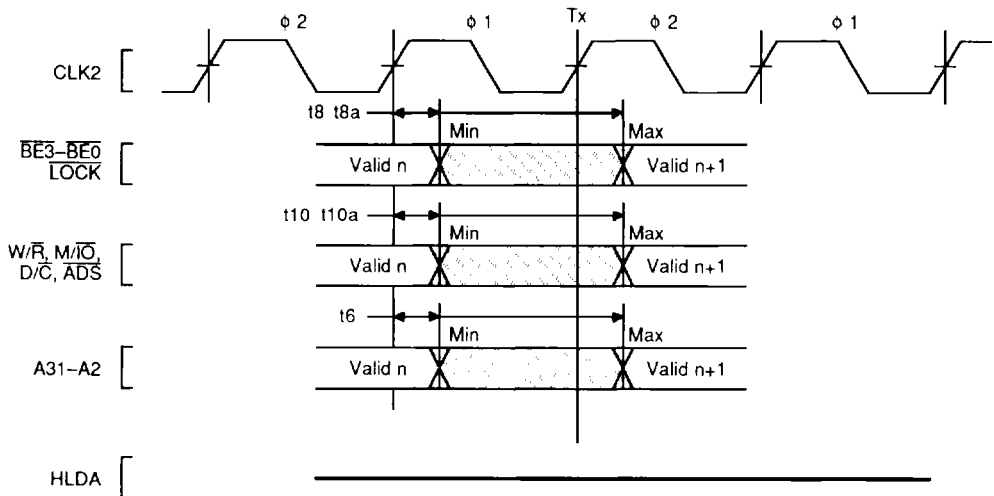
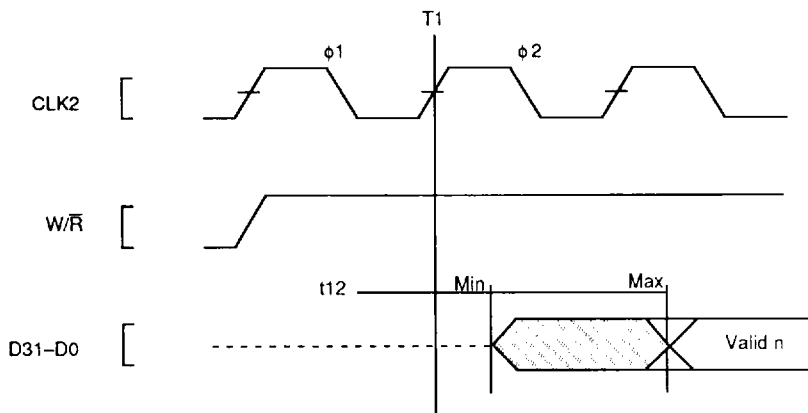


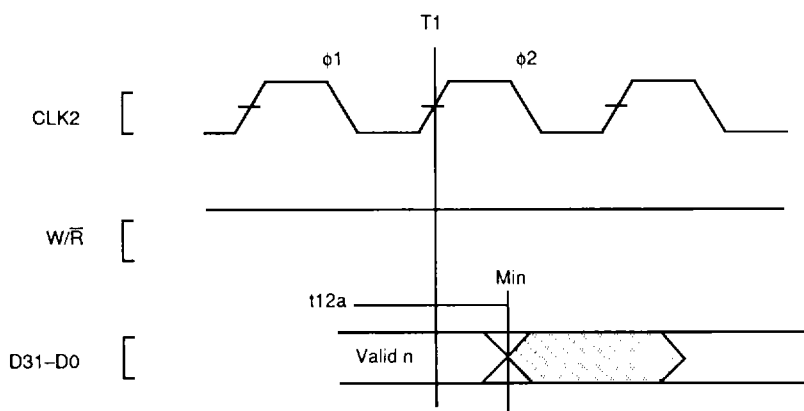
Figure 5. Output Valid Delay Timing

15021B-075



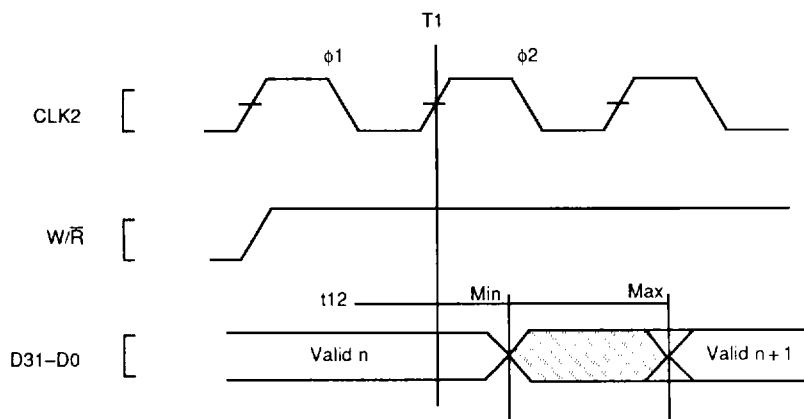
15021B-076

Figure 6. Write Data Valid Delay Timing (25, 33, and 40 MHz)



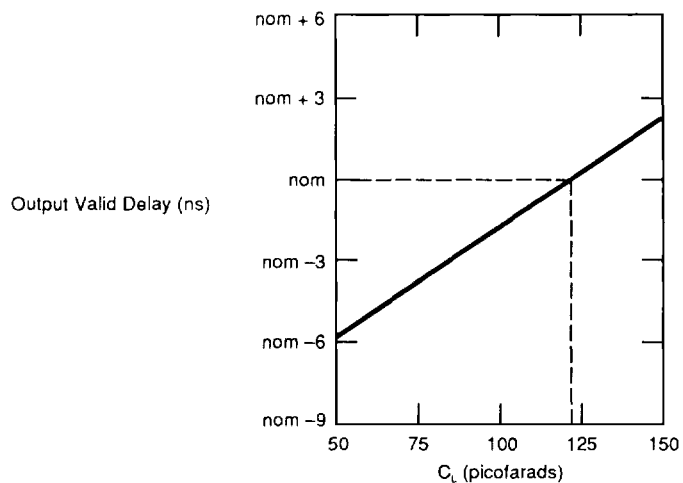
15021B-077

Figure 7. Write Data Hold Timing (25, 33, and 40 MHz)



15021B-078

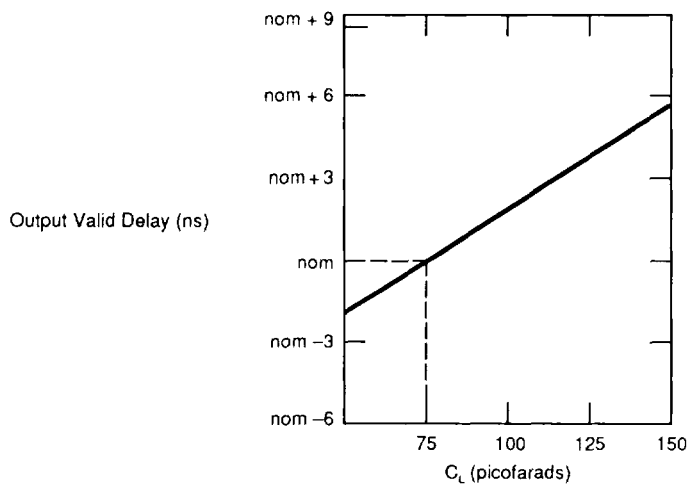
Figure 8. Write Data Valid Delay Timing (20 MHz)



Note: This graph will not be linear outside of the C_L range shown.

15021B-079

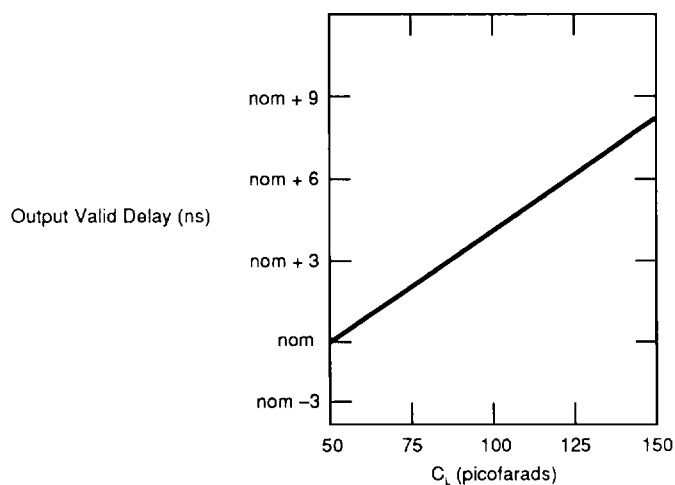
Figure 9. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L = 120$ pF)



Note: This graph will not be linear outside of the C_L range shown.

15021B-080

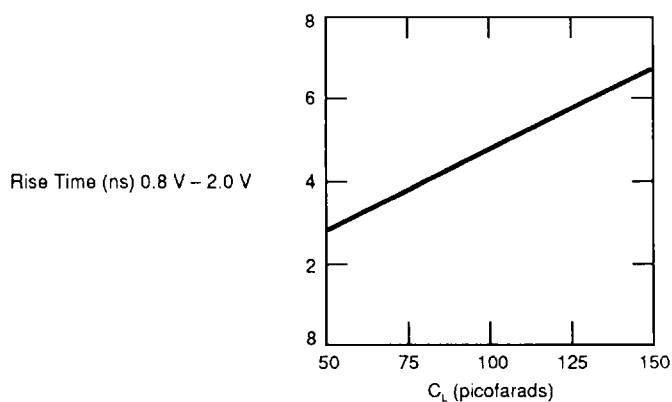
Figure 10. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L = 75$ pF)



Note: This graph will not be linear outside of the C_L range shown.

15021B-081

Figure 11. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature ($C_L = 50$ pF)



Note: This graph will not be linear outside of the C_L range shown.

15021B-082

Figure 12. Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature

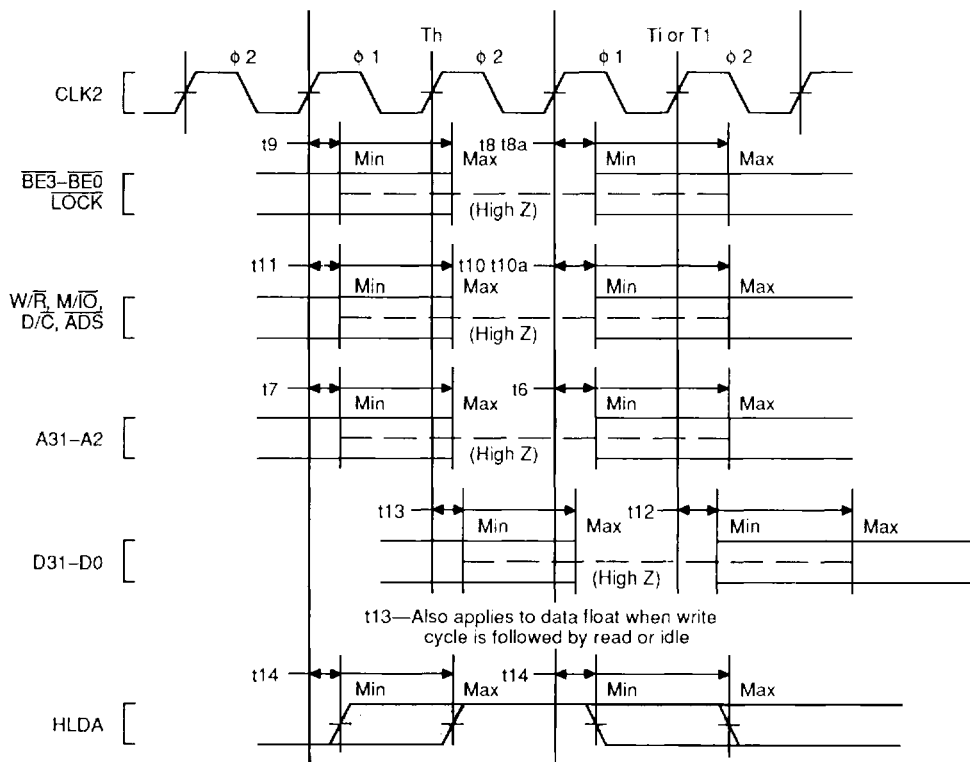
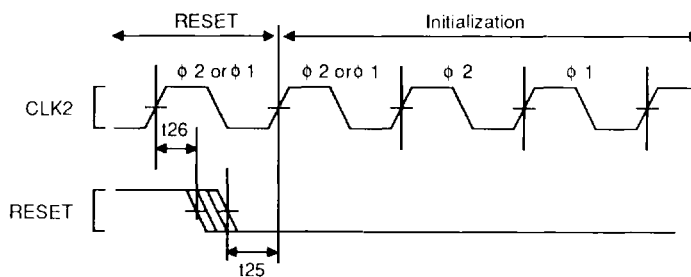


Figure 13. Output Float Delay and HLDA Valid Delay Timing

15021B-083



The second internal processor phase following RESET High to Low transition (provided t_{25} and t_{26} are met) is $\phi 2$.

Figure 14. RESET Setup and Hold Timing and Internal Phase

15021B-084