

74AC899 • 54ACT/74ACT899 9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

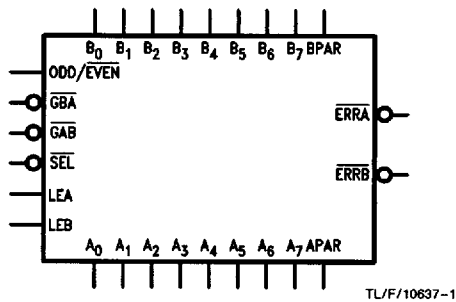
The 'AC/'ACT899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. The 'AC/'ACT899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

Features

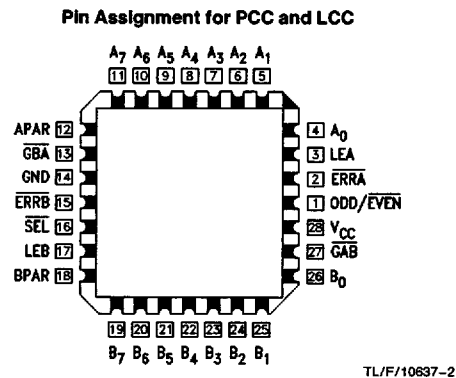
- Latchable transceiver with output sink of 24 mA
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enable for A-to-B and B-to-A directions
- Select pin for ODD/EVEN parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in system applications in place of the '280
- May be used in system applications in place of the '657 and '373 (no need to change T/ $\overline{\text{R}}$ to check parity)
- 4 kV minimum ESD immunity

74AC899 • 54ACT/74ACT899
9-Bit Latchable Transceiver with Parity Generator/Checker

Logic Symbol



Connection Diagram



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FACT™ is a trademark of National Semiconductor Corporation.

Pin Names	Description
A ₀ -A ₇ B ₀ -B ₇ APAR, BPAR ODD/EVEN	A Bus Data Inputs/Data Outputs B Bus Data Inputs/Data Outputs A and B Bus Parity Inputs ODD/EVEN Parity Select, Active LOW for EVEN Parity
\overline{GBA} , \overline{GAB}	Output Enables for A or B Bus, Active LOW
\overline{SEL}	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
\overline{ERRA} , \overline{ERRB}	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The 'AC/ACT899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

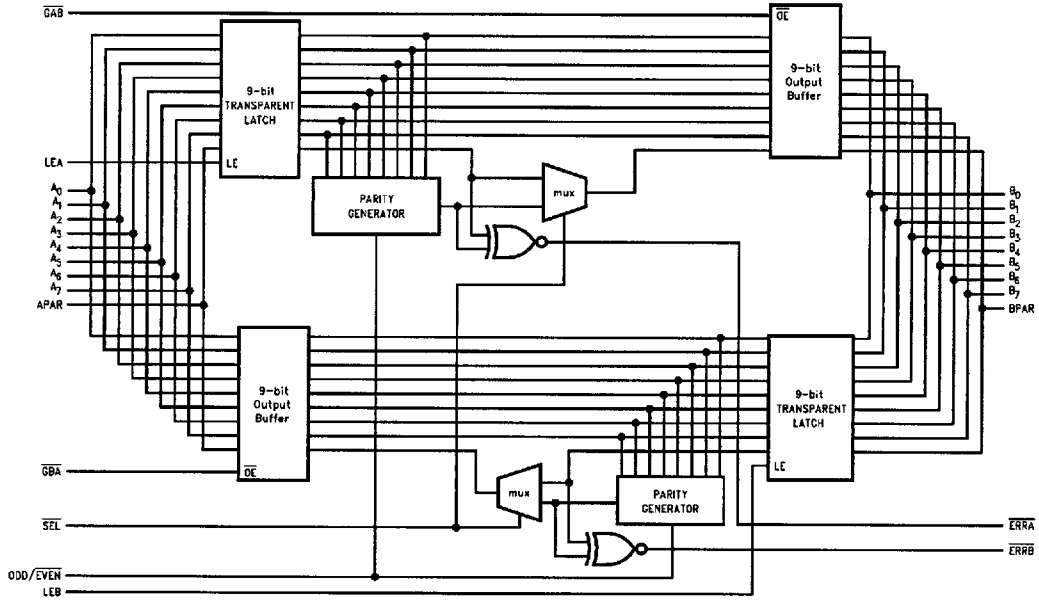
- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select (\overline{SEL}) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by \overline{ERRB} (\overline{ERRA}).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if \overline{SEL} is HIGH. Parity is still generated and checked as \overline{ERRA} and \overline{ERRB} in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

Function Table

Inputs					Operation
\overline{GAB}	\overline{GBA}	\overline{SEL}	LEA	LEB	
H	H	X	X	X	Busses A and B are TRI-STATE®.
H	L	L	L	H	Generates parity from B[0:7] based on O/\overline{E} (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as \overline{ERRB} .
H	L	L	H	H	Generates parity from B[0:7] based on O/\overline{E} . Generated parity → APAR. Generated parity checked against BPAR and output as \overline{ERRB} . Generated parity also fed back through the A latch for generate/check as \overline{ERRA} .
H	L	L	X	L	Generates parity from B latch data based on O/\overline{E} . Generated parity → APAR. Generated parity checked against latched BPAR and output as \overline{ERRB} .
H	L	H	X	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as \overline{ERRB} .
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as \overline{ERRB} . Generated parity also fed back through the A latch for generate/check as \overline{ERRA} .
L	H	L	H	L	Generates parity for A[0:7] based on O/\overline{E} . Generated parity → BPAR. Generated parity checked against APAR and output as \overline{ERRA} .
L	H	L	H	H	Generates parity from A[0:7] based on O/\overline{E} . Generated parity → BPAR. Generated parity checked against APAR and output as \overline{ERRA} . Generated parity also fed back through the B latch for generate/check as \overline{ERRB} .
L	H	L	L	X	Generates parity from A latch data based on O/\overline{E} . Generated parity → BPAR. Generated parity checked against latched APAR and output as \overline{ERRA} .
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as \overline{ERRA} .
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as \overline{ERRA} . Generated parity also fed back through the B latch for generate/check as \overline{ERRB} .

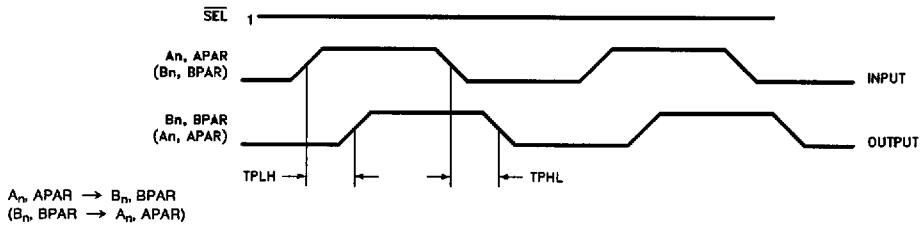
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Note 1: O/\overline{E} = ODD/EVEN

Functional Block Diagram



TL/F/10637-3

AC Path



TL/F/10637-4

FIGURE 1

AC Path (Continued)

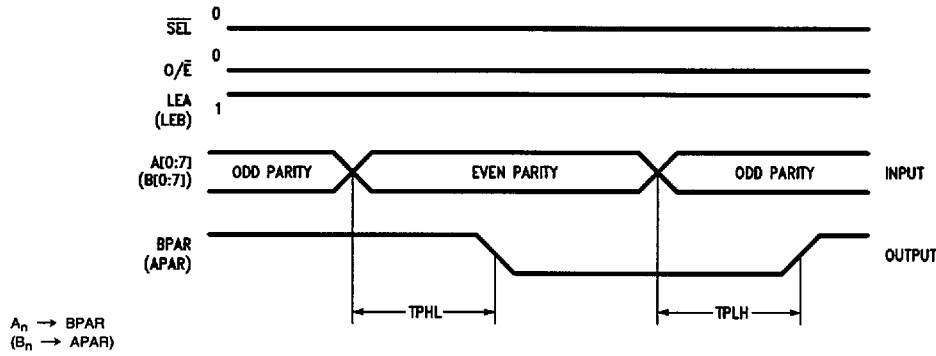


FIGURE 2

TL/F/10637-5

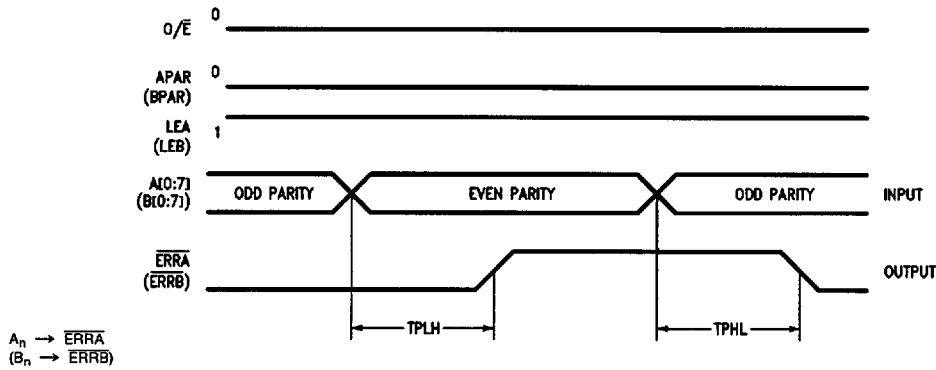


FIGURE 3

TL/F/10637-6

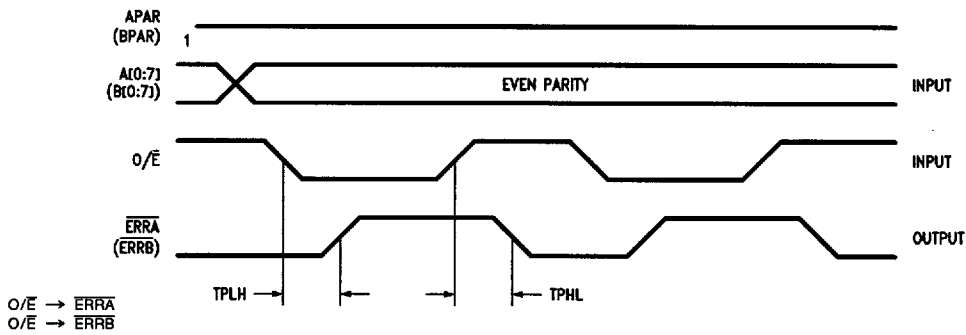


FIGURE 4

TL/F/10637-7

AC Path (Continued)

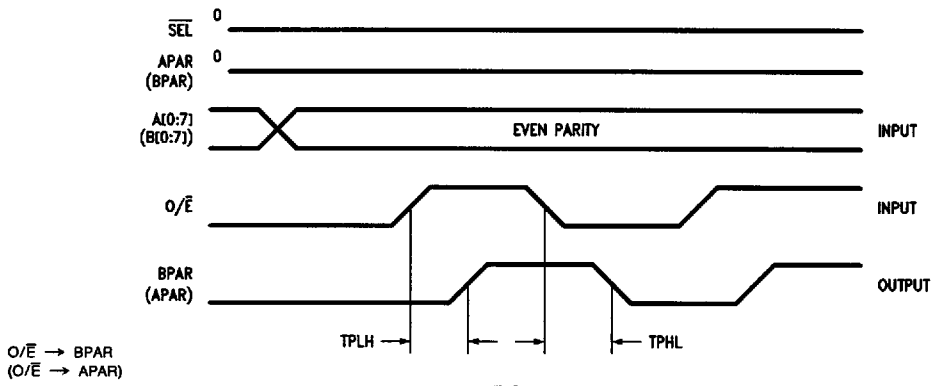


FIGURE 5

TL/F/10637-8

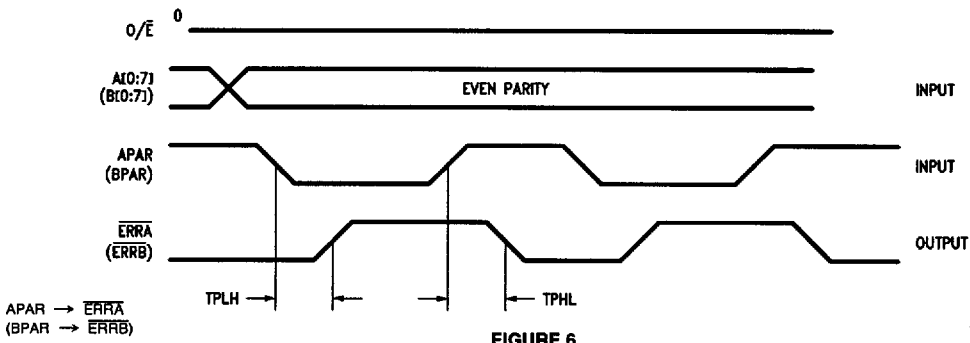
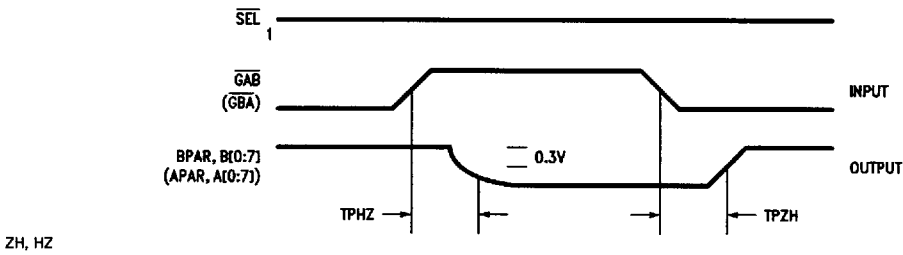


FIGURE 6

TL/F/10637-9

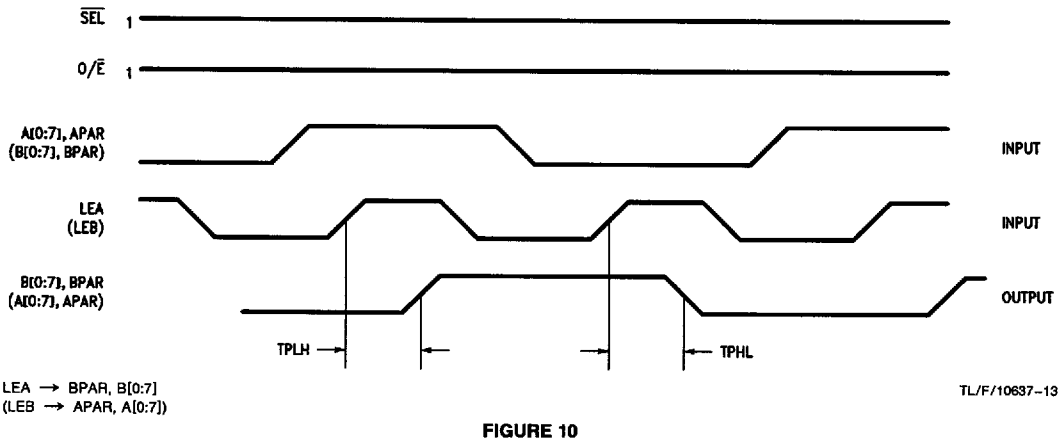
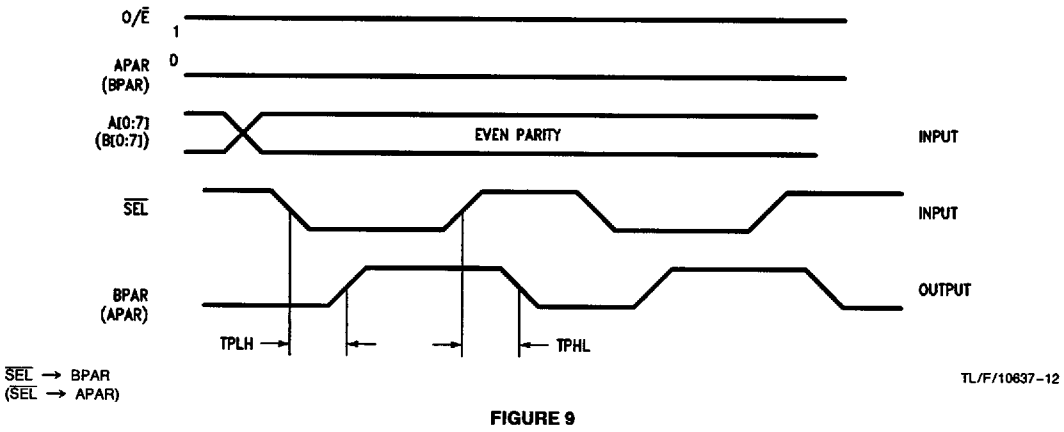
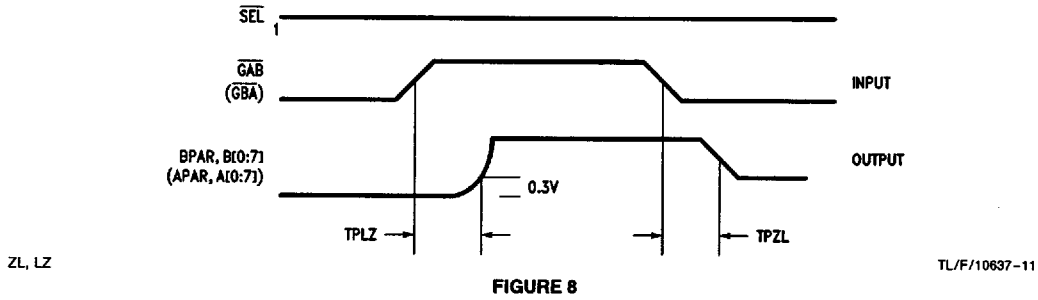


ZH, HZ

FIGURE 7

TL/F/10637-10

AC Path (Continued)



AC Path (Continued)

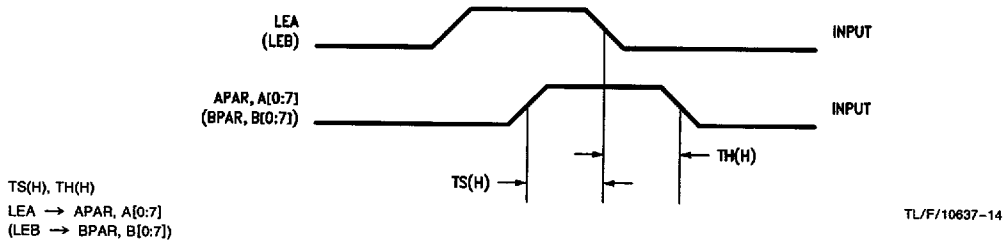


FIGURE 11

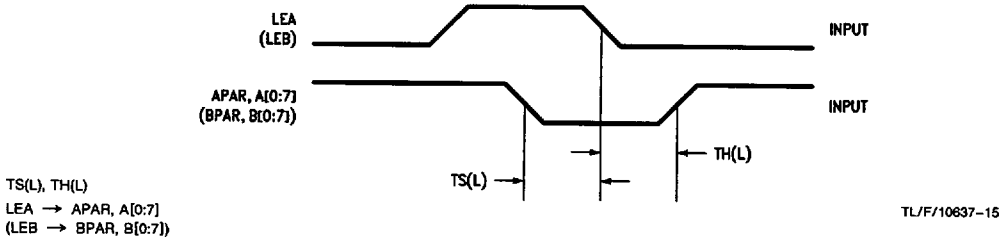


FIGURE 12

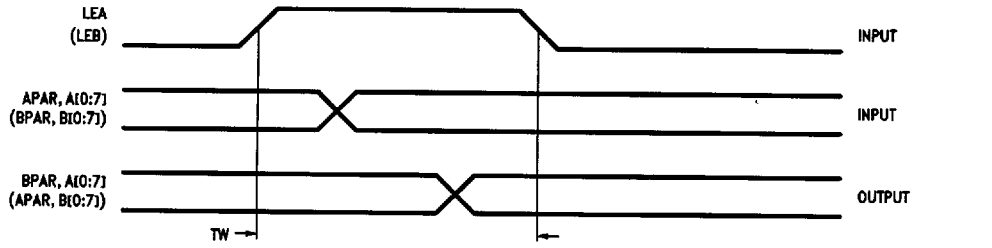


FIGURE 13

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTM circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})		2.0V to 6.0V
'AC		4.5V to 5.5V
'ACT		
Input Voltage (V_I)		0V to V_{CC}
Output Voltage (V_O)		0V to V_{CC}
Operating Temperature (T_A)		
74AC/ACT		-40°C to +85°C
54ACT		-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$		
'AC Devices		
V_{IN} from 30% to 70% of V_{CC}		
V_{CC} @ 3.0V, 4.5V, 5.5V		125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$		
'ACT Devices		
V_{IN} from 0.8V to 2.0V		
V_{CC} @ 4.5V, 5.5V		125 mV/ns

Note: PLCC packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

DC Electrical Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC		74AC		Units	Conditions
			$T_A = +25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$			
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	* $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	* $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}, GND$ (Note)	

*Maximum of 9 outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	5.5				75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5				-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0		80.0	μA	V _{IN} = V _{CC} or GND (Note)
I _{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5		±5.0	μA	V _{I(OE)} = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits						
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	2.0	2.0	2.0	2.0	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	0.8	0.8	0.8	0.8	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	4.4	4.4	V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	3.76	3.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA -24 mA
		5.5		4.86	4.70	4.76	4.76	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	0.44	0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA 24 mA
		5.5		0.36	0.50	0.44	0.44	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	±5.0	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND	
I _{CC1}	Maximum I _{CC} /Input	5.5	0.6		1.6	1.5	1.5	mA	V _I = V _{CC} - 2.1V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75	75	mA	V _{OLD} = 1.65V Max	
I _{OHD}		5.5			-50	-75	-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	80.0	μA	V _{IN} = V _{CC} or GND (Note)	

*Maximum of 9 outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay A _n , B _n to B _n , A _n	3.3 5.0	2.5 1.5	12.0 7.0	15.0 10.0	2.5 1.5	15.5 10.5	ns	1
t _{PLH} t _{PHL}	Propagation Delay APAR, BPAR to BPAR, APAR	3.3 5.0	2.5 1.5	9.5 5.5	12.0 8.0	2.5 1.5	12.5 8.5	ns	1
t _{PLH} t _{PHL}	Propagation Delay A _n , B _n to BPAR, APAR	3.3 5.0	3.0 2.0	13.5 8.0	16.5 11.0	3.0 2.0	17.0 11.5	ns	2
t _{PLH} t _{PHL}	Propagation Delay A _n , B _n to <u>ERRA</u> , <u>ERRB</u>	3.3 5.0	2.5 1.5	12.5 7.5	15.5 10.5	2.5 1.5	16.5 11.0	ns	3
t _{PLH} t _{PHL}	Propagation Delay ODD/EVEN to <u>ERRA</u> , <u>ERRB</u>	3.3 5.0	2.5 1.5	12.5 7.5	15.5 10.5	2.5 1.5	16.5 11.0	ns	4
t _{PLH} t _{PHL}	Propagation Delay ODD/EVEN to APAR, BPAR	3.3 5.0	3.0 2.0	12.5 7.5	15.5 10.5	3.0 2.0	16.5 11.0	ns	5
t _{PLH} t _{PHL}	Propagation Delay APAR, BPAR to <u>ERRA</u> , <u>ERRB</u>	3.3 5.0	2.0 1.5	12.5 7.5	15.5 10.5	2.0 1.5	16.5 11.0	ns	6
t _{PLH} t _{PHL}	Propagation Delay <u>SEL</u> to APAR, BPAR	3.3 5.0	2.0 1.5	10.0 6.0	12.5 8.5	2.0 1.5	13.5 9.0	ns	9
t _{PLH} t _{PHL}	Propagation Delay LEB, LEA to A _n , B _n	3.3 5.0	4.0 2.5	12.0 7.0	15.5 10.5	4.0 2.5	16.5 11.0	ns	10, 11
t _{PLH} t _{PHL}	Propagation Delay LEB, LEA to APAR, BPAR	3.3 5.0	3.0 2.0	13.5 8.0	17.0 11.5	3.0 2.0	18.0 12.0	ns	10, 11
t _{PLH} t _{PHL}	Propagation Delay LEB, LEA to <u>ERRA</u> , <u>ERRB</u>	3.3 5.0	4.0 2.5	13.5 8.0	17.0 11.5	4.0 2.5	18.0 12.0	ns	12
t _{PZH} t _{PZL}	Output Enable Time <u>GBA</u> , <u>GAB</u> to A _n , B _n	3.3 5.0	3.0 2.0	12.5 7.5	15.5 10.5	3.0 2.0	16.5 11.0	ns	7, 8
t _{PZH} t _{PZL}	Output Enable Time <u>GBA</u> , <u>GAB</u> to APAR, BPAR	3.3 5.0	2.5 1.5	10.5 6.0	13.5 9.0	2.5 1.5	14.0 9.5	ns	7, 8
t _{PHZ} t _{PLZ}	Output Disable Time GBA, GAB to A _n , B _n	3.3 5.0	1.5 1.0	11.0 6.5	14.0 9.5	1.5 1.0	14.0 9.5	ns	7, 8
t _{PHZ} t _{PHL}	Output Disable Time <u>GBA</u> , <u>GAB</u> to APAR, BPAR	3.3 5.0	1.5 1.0	11.0 6.5	14.0 9.5	1.5 1.0	14.0 9.5	ns	7, 8

*Voltage Range 5.0 is 5.0V ± 0.5V.
Voltage Range 3.3 is 3.3V ± 0.3V.

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74AC		Units	Fig. No.		
			T _A = +25°C C _L = 50 pF				74AC T _A = -40°C to +85°C C _L = 50 pF	
			Guaranteed Minimum					
t _s	Setup Time, HIGH or LOW A _n , B _n , PAR to LEA, LEB	3.3	3.0		ns	11, 12		
		5.0	3.0					
t _h	Hold Time, HIGH or LOW A _n , B _n , PAR to LEA, LEB	3.3	2.0		ns	11, 12		
		5.0	1.5					
t _w	Pulse Width for LEA, LEB	3.3	4.0		ns	13		
		5.0	4.0					

*Voltage Range 5.0 is 5.0V ± 0.5V.

Voltage Range 3.3 is 3.3V ± 0.3V.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay A _n , B _n to B _n , A _n	5.0	2.5	7.5	11.5	1.5	13.5	2.5	12.0	ns	1
t _{PLH} t _{PHL}	Propagation Delay APAR, BPAR to BPAR, APAR	5.0	1.5	6.0	8.5	1.5	11.0	1.5	9.0	ns	1
t _{PLH} t _{PHL}	Propagation Delay A _n , B _n to BPAR, APAR	5.0	2.5	8.5	12.0	1.5	16.0	2.5	12.5	ns	2
t _{PLH} t _{PHL}	Propagation Delay A _n , B _n to \overline{ERRA} , \overline{ERRB}	5.0	2.0	8.0	11.5	1.5	16.0	2.0	12.0	ns	3
t _{PLH} t _{PHL}	Propagation Delay ODD/EVEN to \overline{ERRA} , \overline{ERRB}	5.0	2.0	8.0	11.5	1.5	16.0	2.0	12.0	ns	4
t _{PLH} t _{PHL}	Propagation Delay ODD/EVEN to APAR, BPAR	5.0	2.5	8.0	11.5	1.5	14.5	2.5	12.0	ns	5
t _{PLH} t _{PHL}	Propagation Delay APAR, BPAR to \overline{ERRA} , \overline{ERRB}	5.0	1.5	7.5	10.5	1.5	11.5	1.5	11.5	ns	6
t _{PLH} t _{PHL}	Propagation Delay \overline{SEL} to APAR, BPAR	5.0	1.5	6.5	9.0	1.5	12.5	1.5	9.5	ns	9
t _{PLH} t _{PHL}	Propagation Delay LEB to A _n , B _n	5.0	2.5	7.0	10.5	1.5	13.5	2.5	11.0	ns	10, 11
t _{PLH} t _{PHL}	Propagation Delay LEA to APAR, BPAR	5.0	2.0	8.0	11.5	1.5	16.0	2.0	12.0	ns	10, 11
t _{PLH} t _{PHL}	Propagation Delay LEA, LEB to \overline{ERRA} , \overline{ERRB}	5.0	2.5	8.0	11.5	1.5	16.0	2.5	12.0	ns	12
t _{PZH} t _{PZL}	Output Enable Time \overline{GBA} or \overline{GAB} to A _n , B _n	5.0	2.5	7.0	10.5	1.5	16.0	2.5	11.0	ns	7, 8
t _{PZH} t _{PZL}	Output Enable Time \overline{GBA} or \overline{GAB} to BPAR or APAR	5.0	1.5	6.0	9.0	1.5	11.0	1.5	9.5	ns	7, 8
t _{PHZ} t _{PHL}	Output Disable Time \overline{GBA} or \overline{GAB} to A _n , B _n	5.0	1.5	6.5	9.5	1.5	11.0	1.5	9.5	ns	7, 8
t _{PHZ} t _{PLZ}	Output Disable Time \overline{GBA} or \overline{GAB} to BPAR, APAR	5.0	1.5	6.5	9.5	1.5	11.0	1.5	9.5	ns	7, 8

*Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74ACT	54ACT	74ACT	Units	Fig. No.
			T _A = +25°C C _L = 50 pF	T _A = -55°C to +125°C C _L = 50 pF	T _A = -40°C to +85°C C _L = 50 pF		
			Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW A _n , B _n , PAR to LEA, LEB	5.0	3.0	3.0	3.0	ns	11, 12
t _h	Hold Time, HIGH or LOW A _n , B _n , PAR to LEA, LEB	5.0	1.5	3.0	1.5	ns	11, 12
t _w	Pulse Width for LEB, LEA	5.0	4.0	4.0	4.0	ns	13

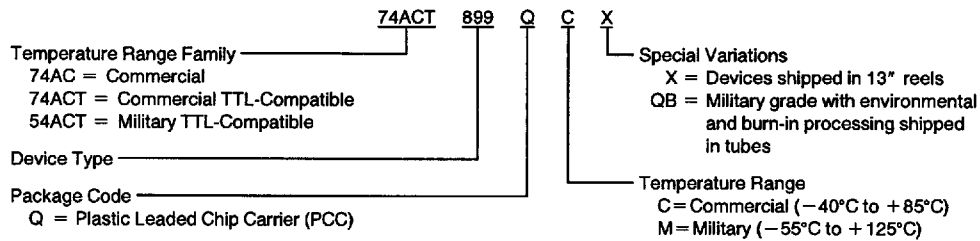
*Voltage Range 5.0 = 5.0V ±0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	210	pF	V _{CC} = 5.0V

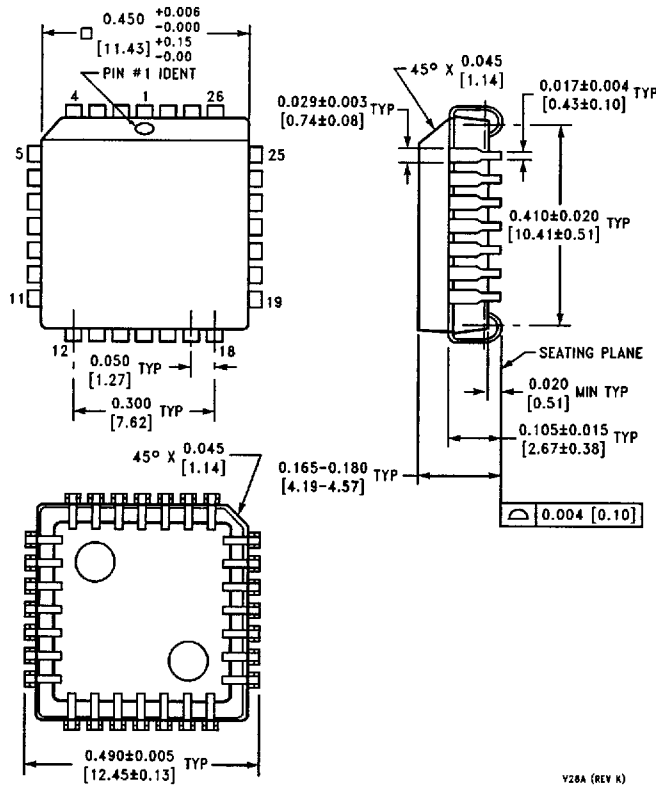
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

Lit. # 115200



28-Lead Plastic Chip Carrier (Q)
 NS Package Number V28A

V28A (REV K)

LIFE SUPPORT POLICY

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